APV Readout and Experiment Trigger

The OLYMPUS experiment

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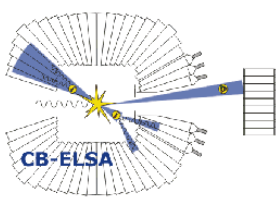

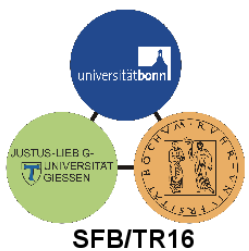

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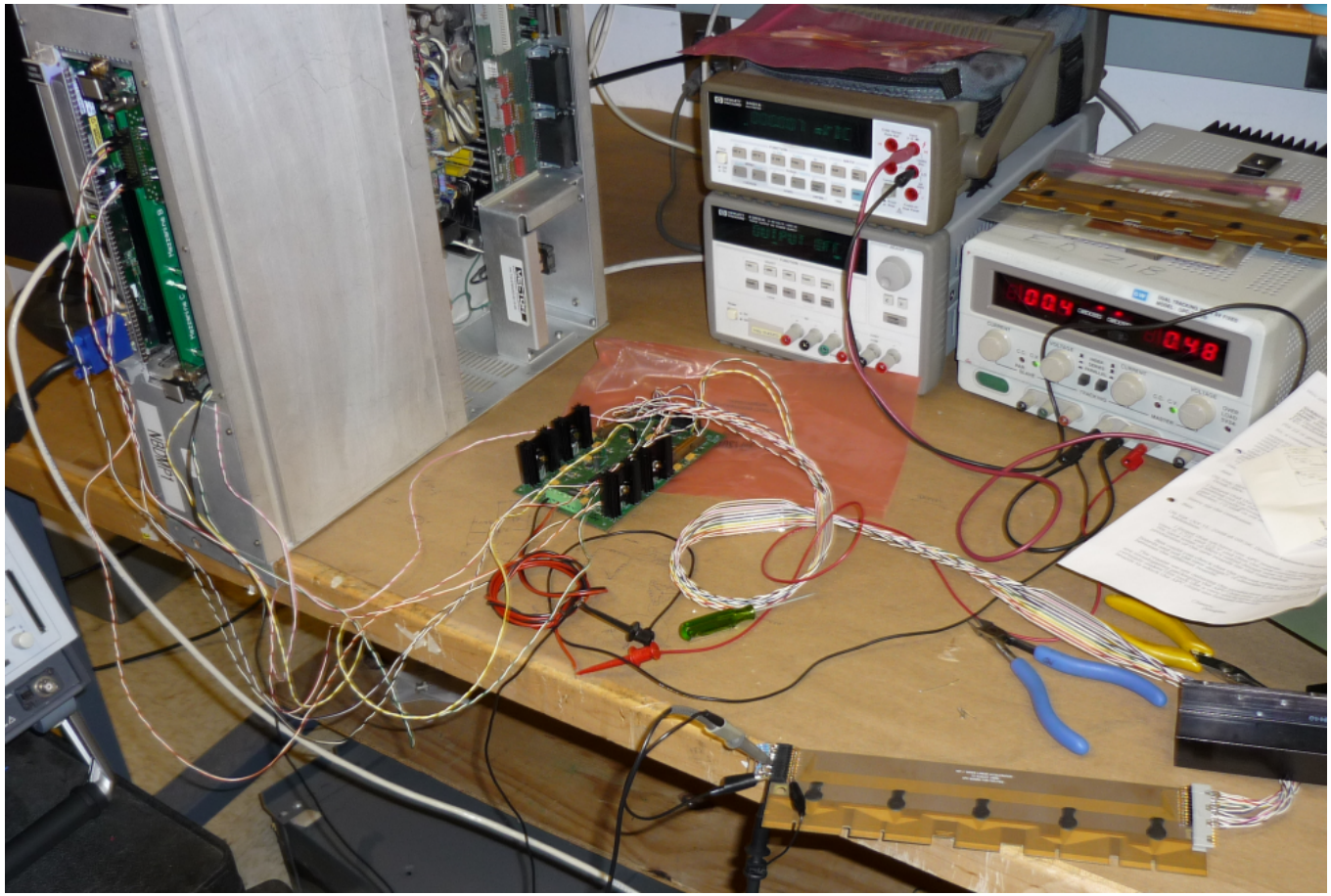
APV readout system



3 stage readout electronics (ADC, supply board, APV board)

Tests at Bates

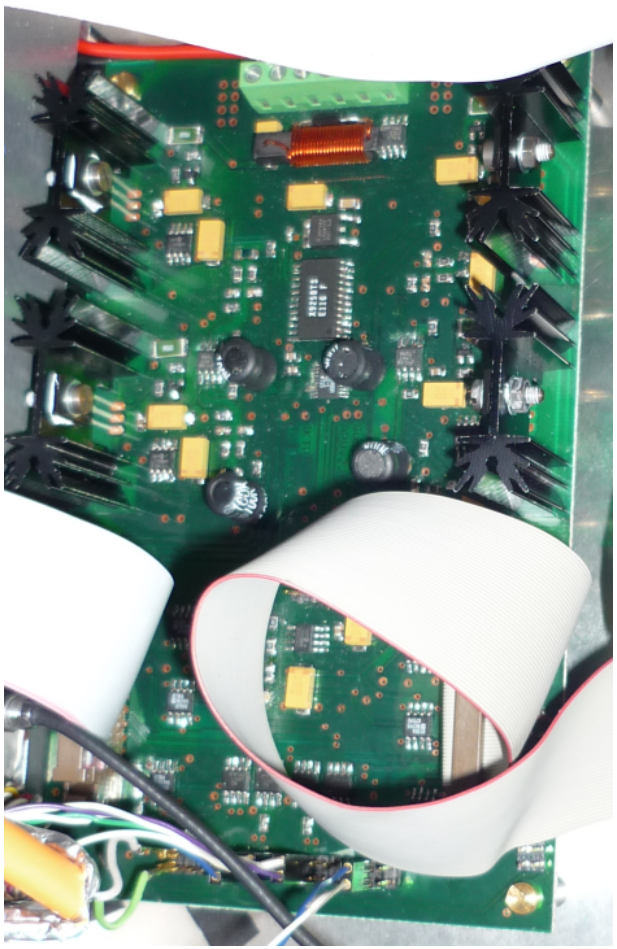
Goals for testing

- Demonstrate the readout system
- Check interfacing between readout system and MIT APV boards
- Testing qualitatively the noise
- Identify weak points in the systems
- ☺ *Test the customs in Cologne and Boston with a CARNET ATA*

MIT APV board

- 5 APVs per board
- MIT (Miro) design
- Edge connectors for detector

Supply board



Specifications

- Generate voltages for APVs
- I^2C level translators
- Differential line driver
- Tested cable length to APVs $\lesssim 5\,\mathrm{m}$

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ADC module

Specifications

- FPGA based VME module
- 3 ADC mezzanine cards
  - 4 APVs per card
  - 12 bit resolution
  - Up to 65 MSPS/s
  - Variable clock source and frequency
- Firmware
  - Base line determination and subtraction
  - Zero suppression
  - (1d cluster)

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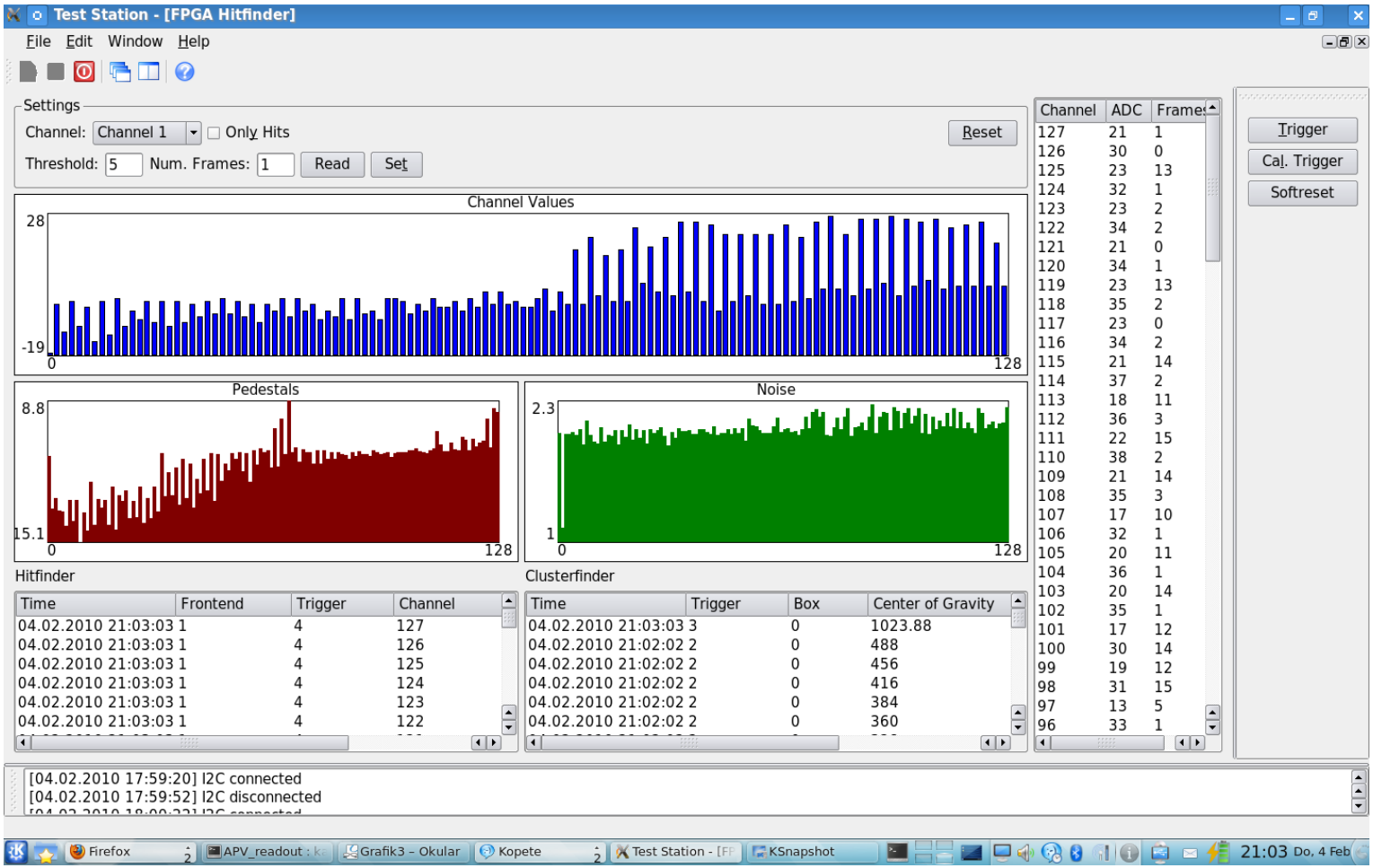
Test results



- APVs configured via I^2C
- Data and heart beat observing, pedestal determination

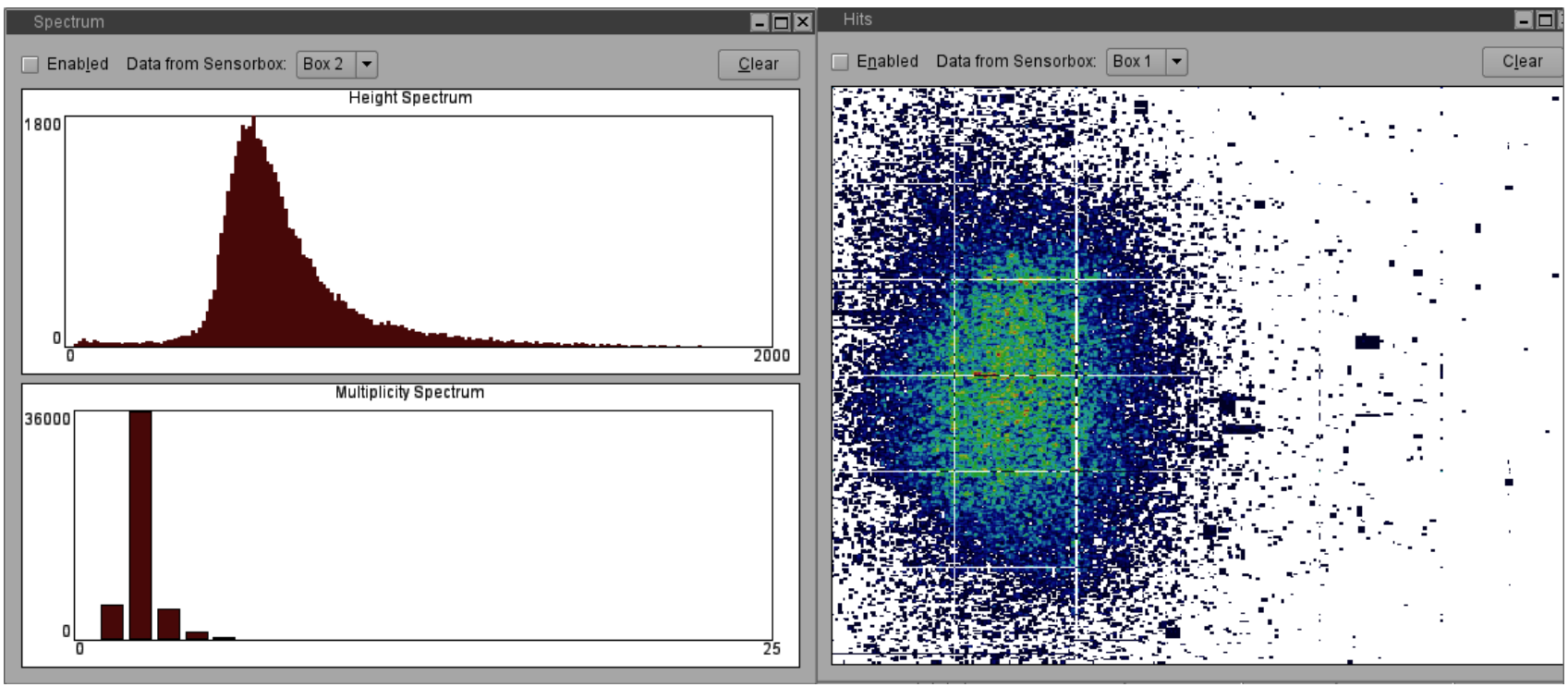
Improvements of APV board

Suggestions for APV boards

- 100 Ω resistor between GND2 and VDD direct at APV chip
- Numerous decoupling capacitors for supply voltages
- Connection of SDATA in and SDATA out on APV board
- Termination of clk, trigger on APV board
- Pull-up resistors for I2C lines on APV board
- APV addresses should be configured via soldering connections

Further activities

- Integration of readout system into Olympus DAQ
- Successful beam tests with 24 APVs (silicon strip detectors) in proton beam at COSY



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Trigger for OLYMPUS

Specifications

- FPGA based VME module
- I/O Mezzanine cards (NIM/LVDS/ECL)
- VHDL firmware
- Fully configurable via VME

  Simulated and tested ✓

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OLYMPUS Trigger

Trigger features

- Synchronized to 10 MHz DORIS clock
- 8 parallel trigger conditions
  - Trigger and veto pattern
  - Event ID / priority
  - 24 bit pre-scaler
- Scaler events (Δt : 10 ns .. 42 s)
- Latching 32 bit scaler for
  - All trigger conditions
  - Event and system reset
  - Lifetime and spilltime
- Adjustable trigger re-arm procedure

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