OLYMPUS Collaboration
DESY 28/June/2010

# Rome group activity since last meeting (3)


Salvatore Frullani / INFN-Rome Sanità Group

# Outline

- MWPC electronics
  - Request , what will be provided
  - Safe working conditions for electronics
- Monitor GEM electronics
  - INFN design for GEM readout plane (40x50 $cm^2$) sent, upon request, to M. Kohl
  - GEM performances at PREX, simulation studies
  - GEM electronics
  - Request for GEM Monitor electronics
  - Test beam plans in July

# MWPC readout PCOS4 system LeCroy-ISS design for HERMES

- Monitor MWP Chambers: 400 channels each -> 25 PCOS4 cards + 2 backplanes 14 slots + ½ VME module
- For 6 chambers: 2400 channels -> 150 fec + 12 backplanes + 3 VME modules + 1 VME controller + 1 fanout module
- Readout electronics and some spare
- Electronics needed for RICH SBS then we must guarantee a use in safe condition
- Conditions used for HERMES MWPC and RICH must be reproduced: temperature control, switches and relays for low voltage power supply, patch panels and all other services

THE HERMES MAGNET CHAMBERS, READOUT and ELECTRONICS

E. Cisbani from a first idea of M. Iodice

last revision December 2000

http://www.iss.infn.it/webg3/hermes/mc.zip

**Contents**

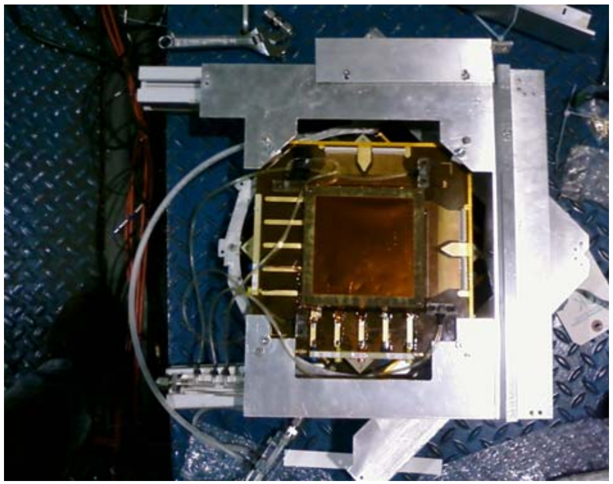
- All software prepared by our group for HERMES is available:
  - Setting
  - Acquisition
  - Checking
  - Debugging
- Electronics is not radiation hard:
  - Check radiation field in installation place near beam pipe (see Axel Schmidt talks): exposure rate (Gray/h) and integrated exposure for all the working period
  - If the case the electronics must be tested after being exposed in a Gamma exposition cell

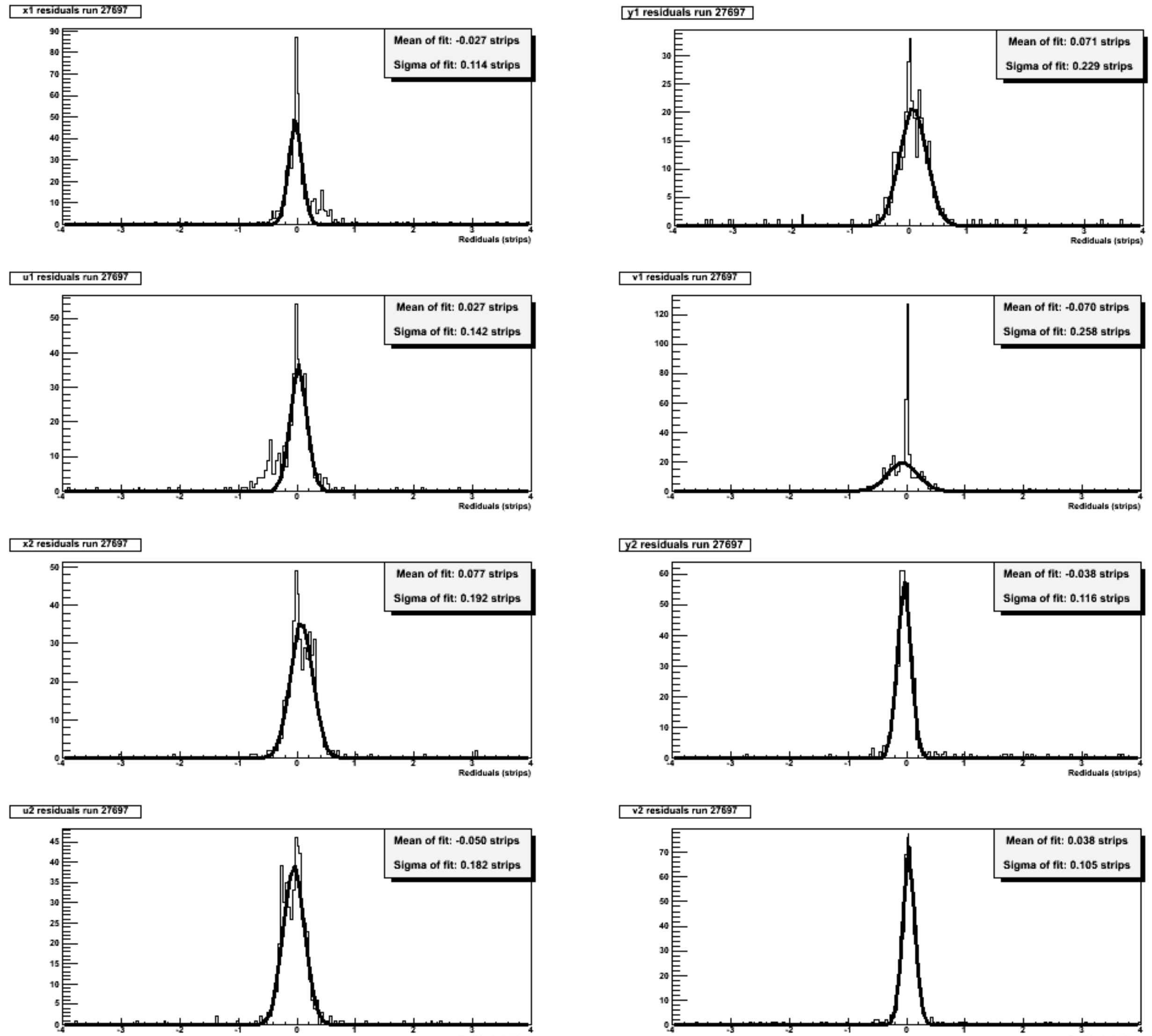
# GEM: PREX gaining experience

- Useful to introduce people in data reduction and analysis (help from Rome group – Guido Maria Urciuoli – and JLab group)
- Confirmed GEM performances : 100 μm resolution for a 400 μm pitch

# Test PREX

- Spatial resolution on 2D readout with 0.4 mm pitch





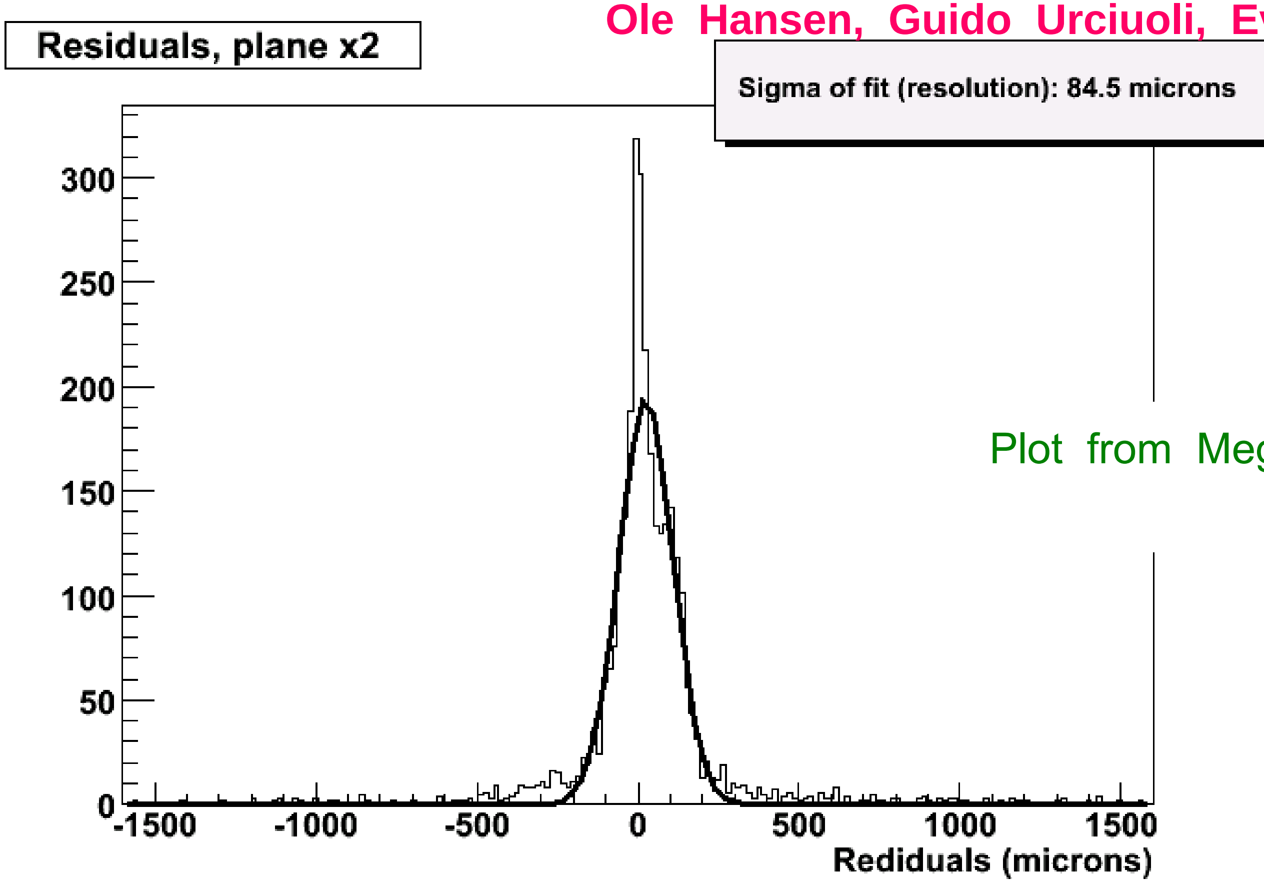

Results from Megan Friend

# New GEM Detectors

High-rate tracking (issue for $Q^2$ )

4 Chambers on L-HRS are working.

**Nilanga Liyanage, Seamus Riordan, Kiadtisak Saenboonruang, Alexandre Camsonne, Ole Hansen, Guido Urciuoli, Evaristo Cisbani**



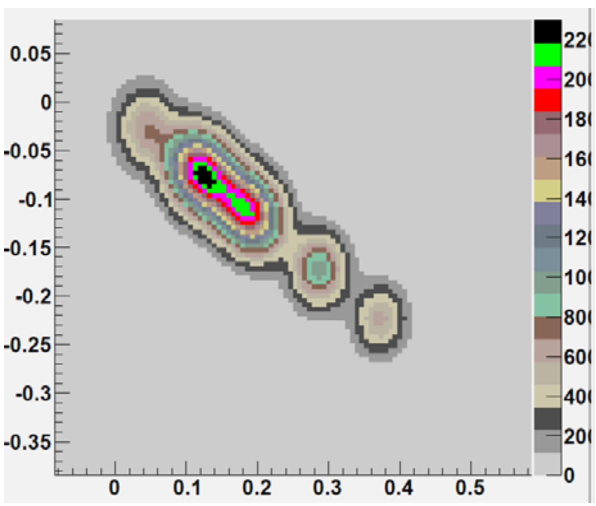

Plot from Megan Friend

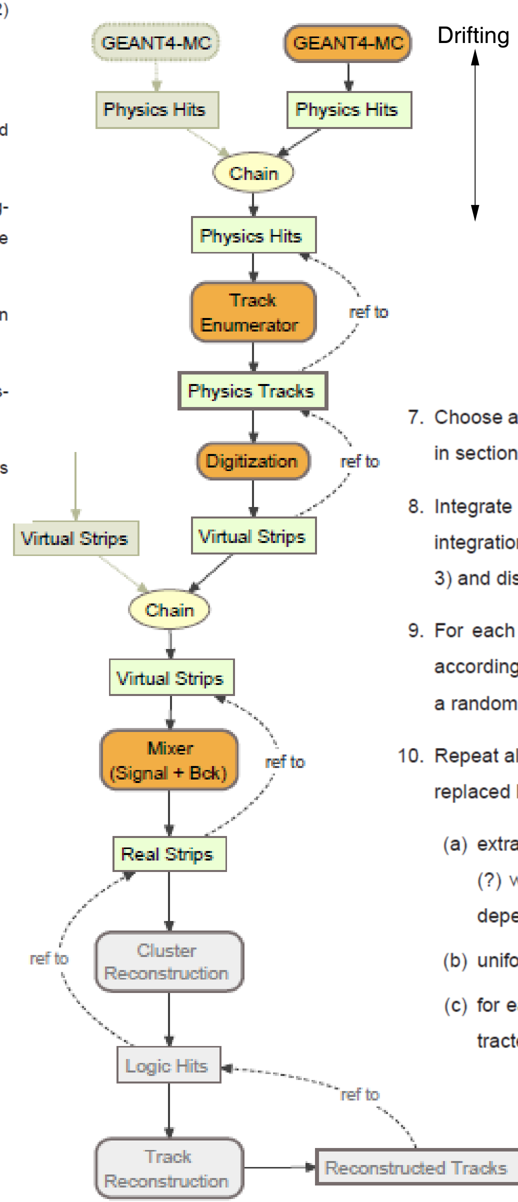
# GEM digitization (implemented under ROOT)

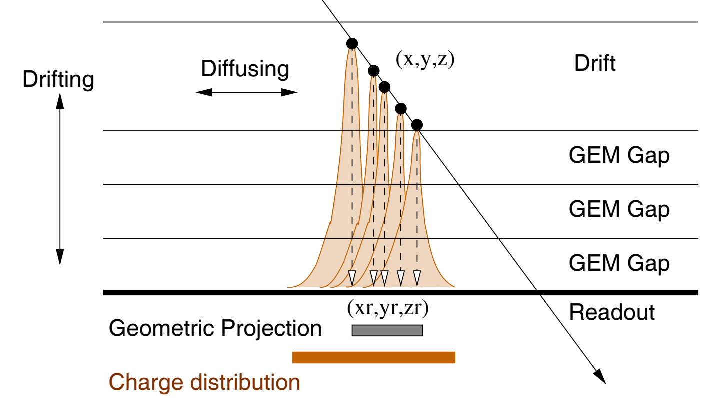
### 5.1 Digitization algorithm

The digitization algorithm uses the output of the GEANT4 MonteCarlo (see table 1) as input as well as geometry parameters and physics parameters of the chamber (see 2) and produces a 'friend' output (see table 3).

1. Project the track segment in the drift gap to the readout plane.
2. Assume $n_{ion}$ $(x_i^r, y_i^r)$ points Poisson distributed with mean $\overline{n}_{ion}$, in the projected segment.
3. Such points are assumed to be spatially uniformly distributed (along the segment); (implementation: extract $n_{ion}$ values of length from 0 to $L_s$, being $L_s$ the length of the projected segment).
4. Each point is the center of a 2D gaussian with $\sigma_x = \sigma_y = \sigma_s$ (see above equation 1).
5. The integral (total charge for each secondary) of the gaussian is given by $G$ distributed according to a gaussian function with mean $\overline{G}$ and $\sigma_G$ given by 2.
6. Sum up all gaussian centered in the projection of the primary ionization pairs points.



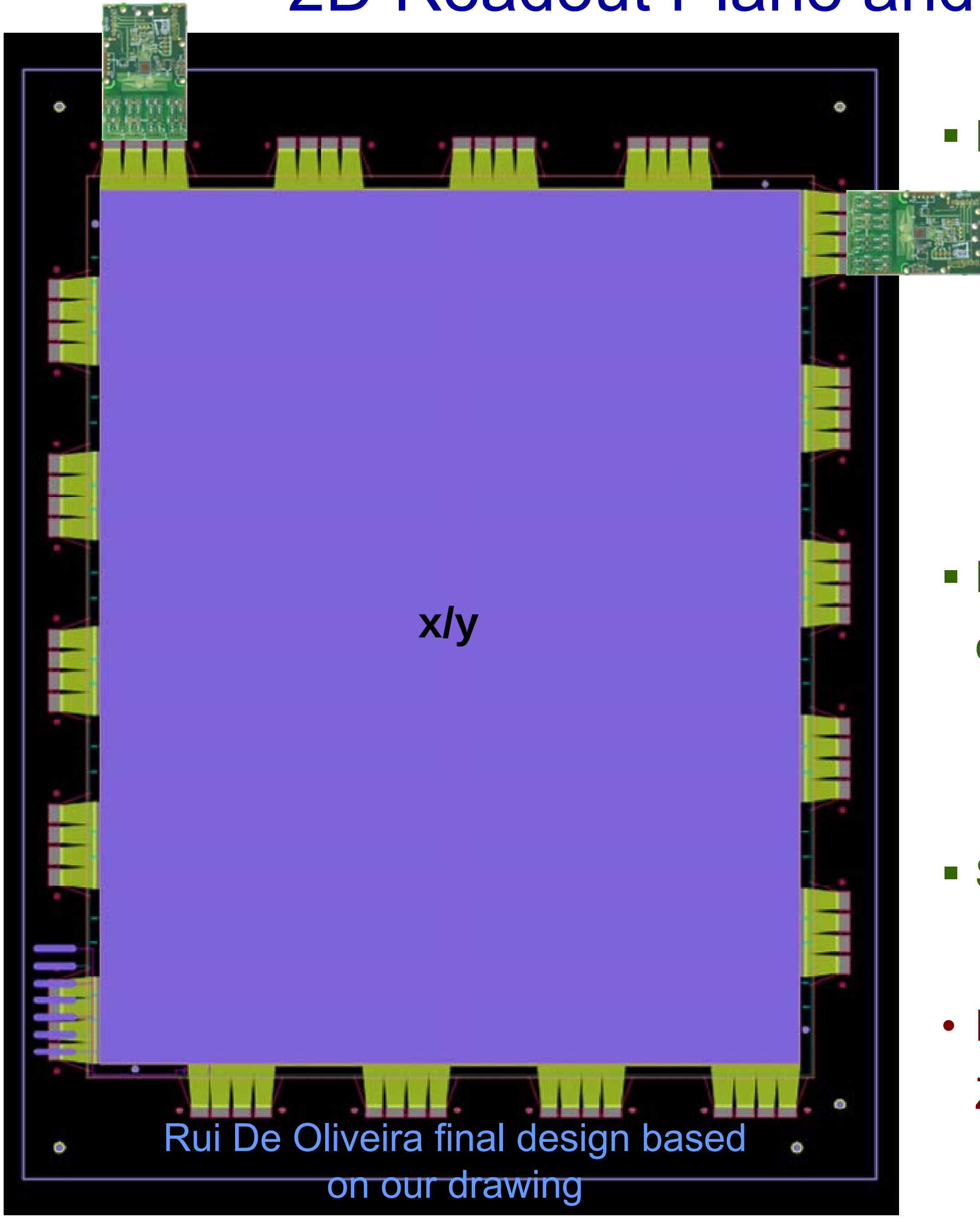




7. Choose a rectangular window around the projected segment as suggested above in section 4.
8. Integrate the window pixels to get the charge of each strip in $x$ and $y$ (note that integration along one axis is continuous, while along the other is in steps, see fig 3) and discussion above.
9. For each strip in the window take 3 consecutive 25 ns samples of the signal according to eq. 4.1 starting at fixed time (or point in the signal, possibly adding a random jitter TO BE DEFINED).
10. Repeat all the above steps for the background hits, except step 9, which shall be replaced by:
    (a) extract the number of background hits $n_{bck}$ according to a Poisson distribution (?) with mean $r_{bck} \cdot \Delta t$ where $r_{bck}$ is the background rate (in principle space dependent!) and $\Delta t$ the effective time window (see 4.1).
    (b) uniformly extract $n_{bck}$ times $tr^i_{bck}$ between $-t_{signal}$ and $n_{sample} \cdot t_{sample}$
    (c) for each strip take 3 consecutive samples starting at the random points extracted in the previous item, relative to the "0" of the GEM signal

# Monitor GEM project

- Upon request from Michael Kohl, sent design of our 40x50 $cm^2$ module for SBS GEM in Gerbv files in order to be of help for the design of 10x10 $cm^2$ (1/20 area) OLYMPUS GEM Monitor
- Same solution to interface electronic FEC adopted (positive solution)

# 2D Readout Plane and ZIF extension

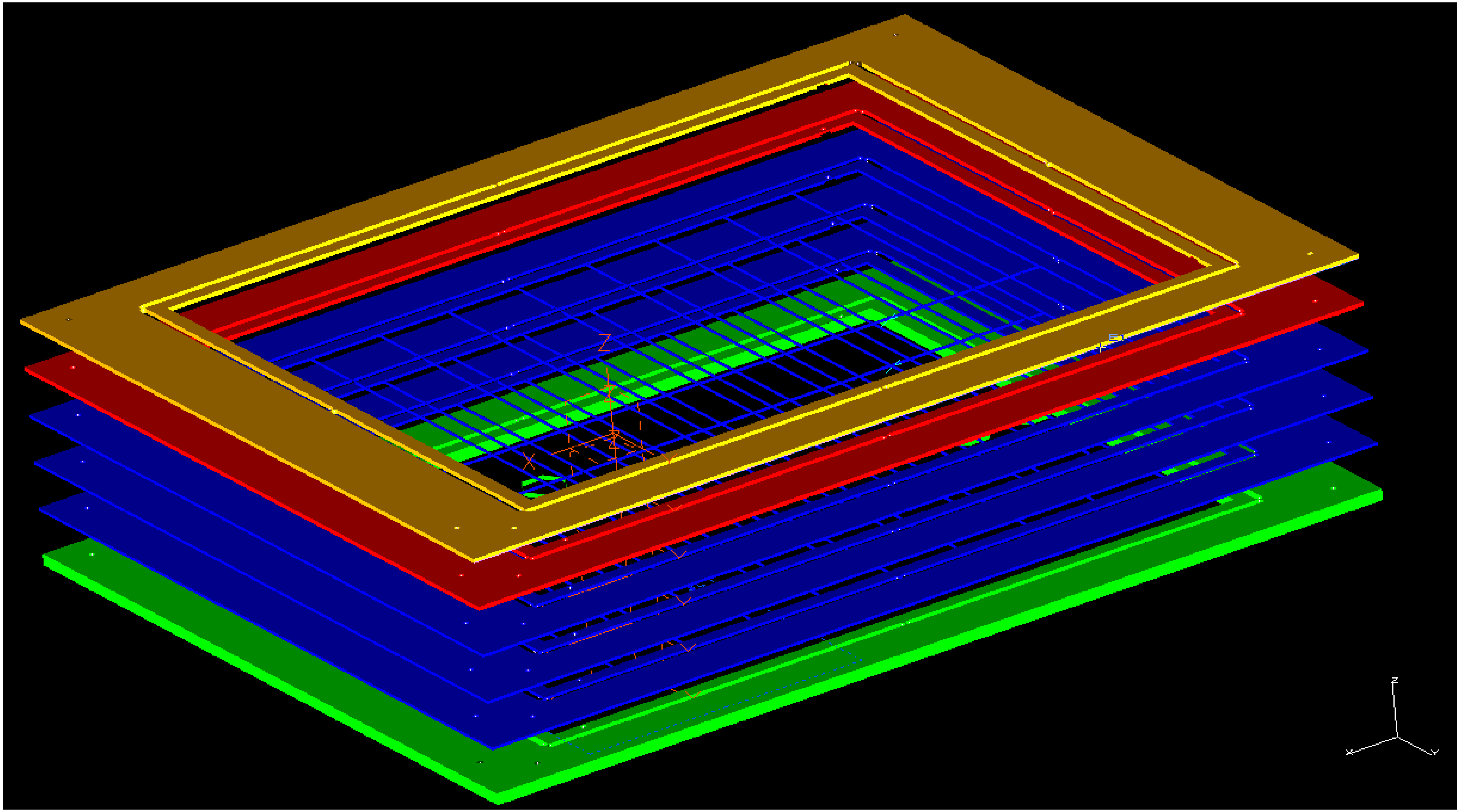



- Readout along all sides
  - not strictly required in x/y unless additional segmentation of the readout plane
  - weight balance
  - unavoidable in diagonal u/v
- Extension feeds into ZIF connectors:
  - no soldering on the readout foil
  - permit safer bending
- Small frame width (8 mm); minimize dead area
- Require precise cutting around the ZIF terminals

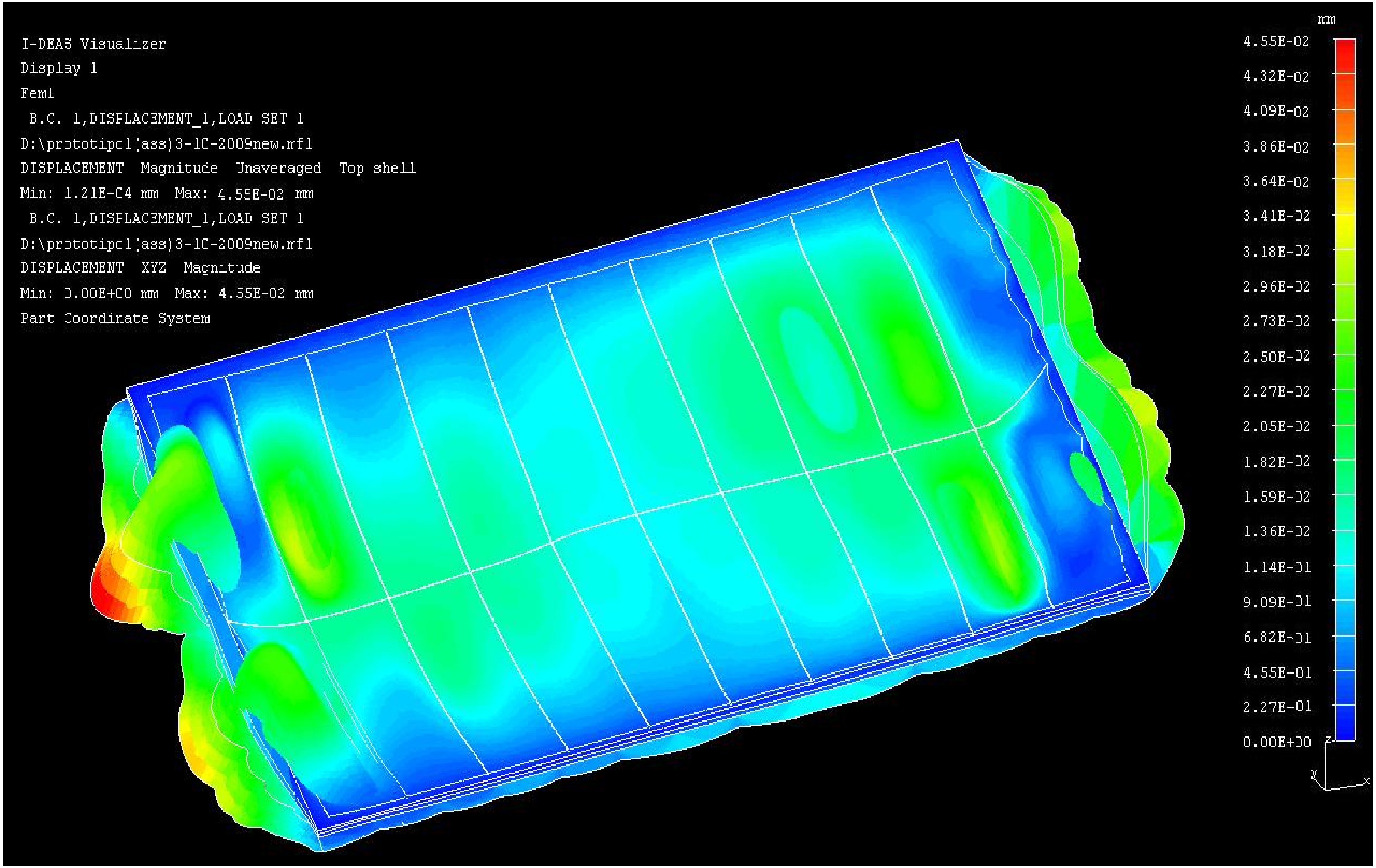
**Under delivery!**

# SIMULAZIONE FRAME

ESPLOSO DELLA CAMERA GEM

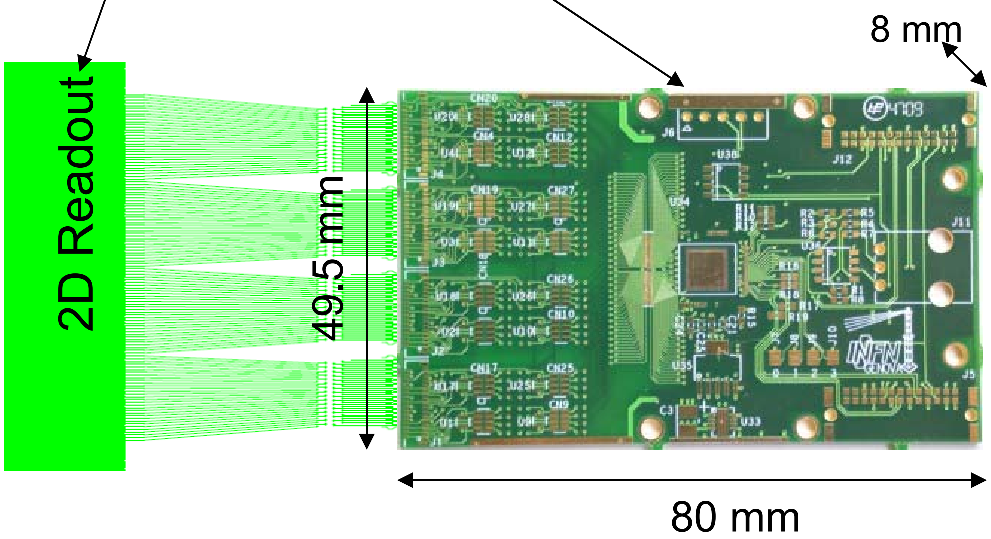


# SIMULAZIONE FRAME



# Electronics Components

## GEM ⇒ FEC ⇒ ADC+VME Controller ⇒ DAQ




**Up to 16 FEC**

**Up to 10 m or + ?**

Main features:

- Use analog readout APV25 chips (wire-bonded on standard PCB, no ceramics): proven to work in COMPASS
- ZIF connector on the GEM side (no soldering on readout foil)
- Minimum electronics components (front-end + VME custom module)
- Copper connection between front-end and VME

# Front End Card (Proto 0)

## GEM ⇒ FEC ⇒ ADC+VME Controller ⇒ DAQ

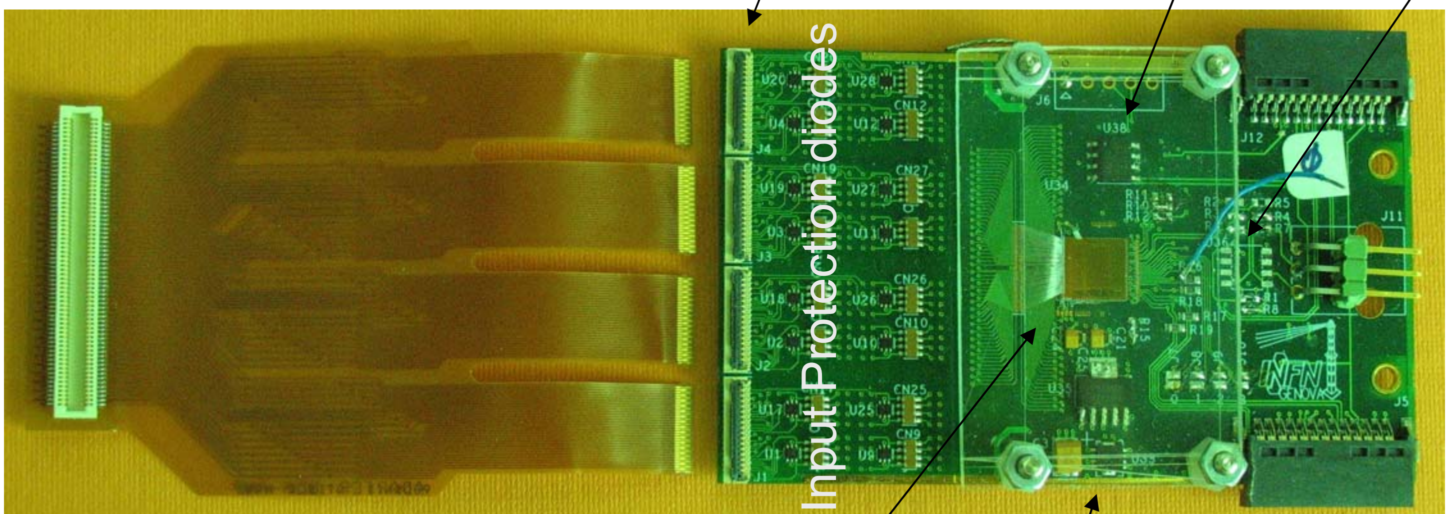
Front End card based on the APV25 chip

1 FE = 1 APV25 = 128 chs

Panasonic FPC connectors

Thermometer

Analog Driver




Analog Output

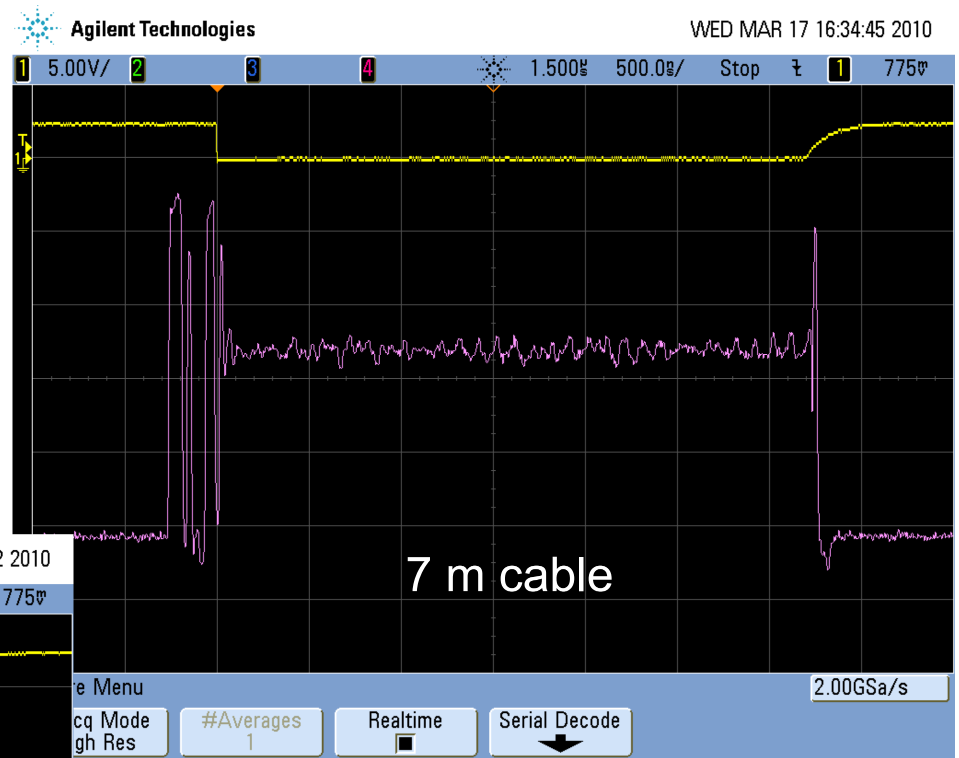
Digital IN
Power Line
I2C

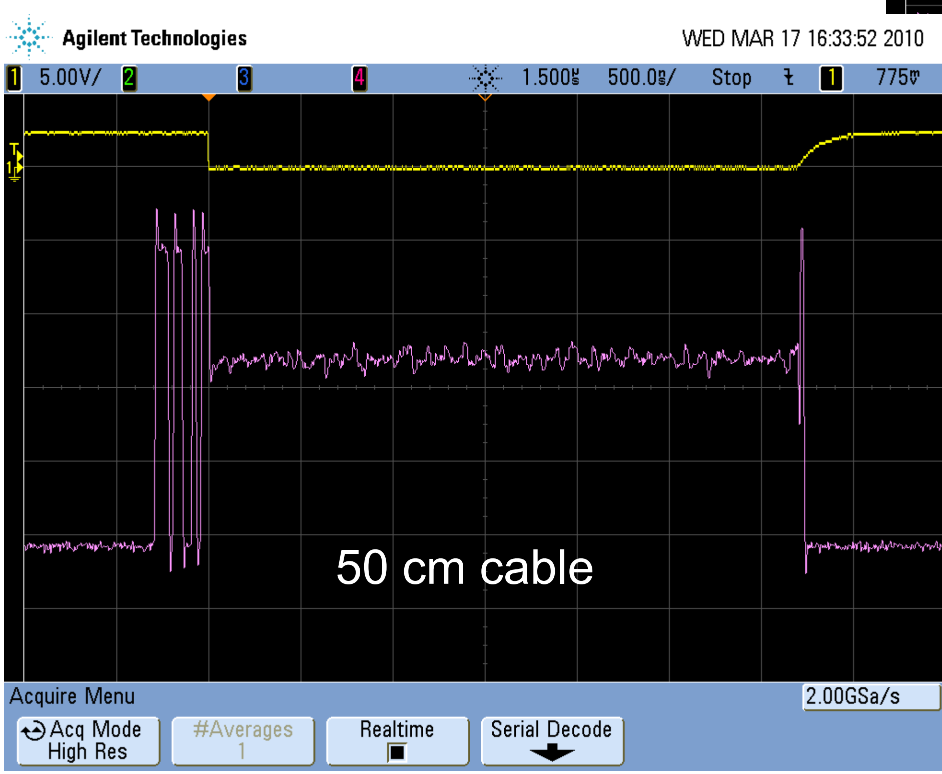
APV25 bonding on PCB

Voltage regulators

# Front-end prototypes tests

- Front-end card under control
- First tests on analog cable length positive
- No analog driver

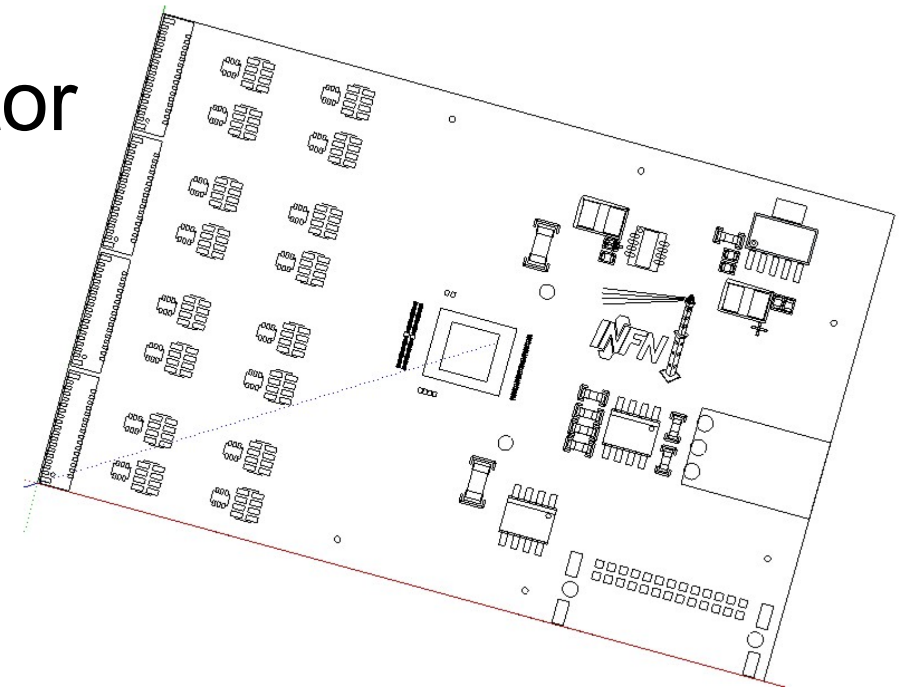



Work is in progress

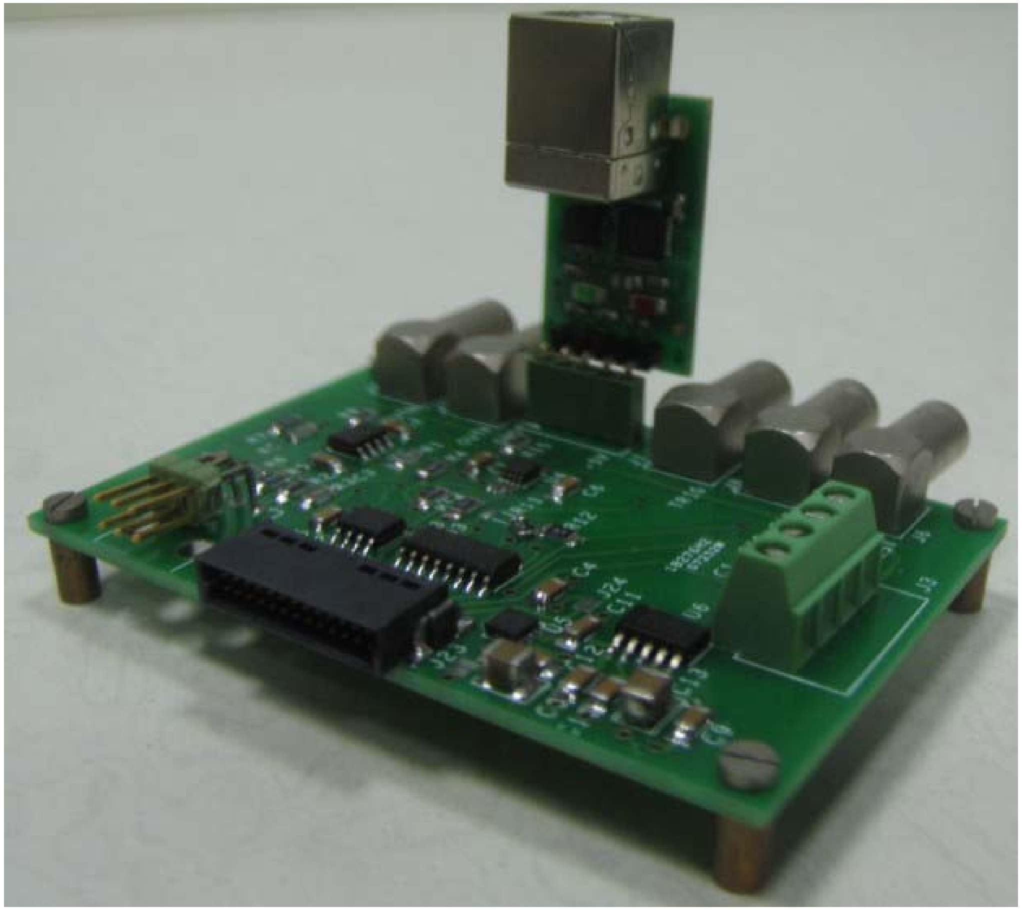
# Front-End new version (Proto 1)

- Bug fixing of previous version
- Denser Bonding: 50 um pad, 100 um pitch
- Backplane connector (back side)
- 5 mm shorter
- Arrived June 14

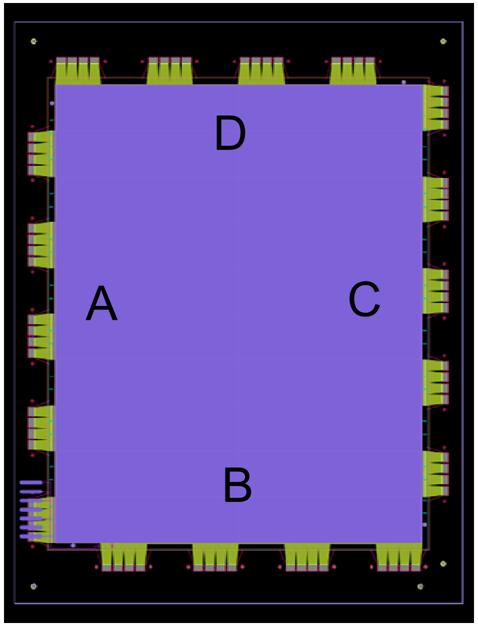


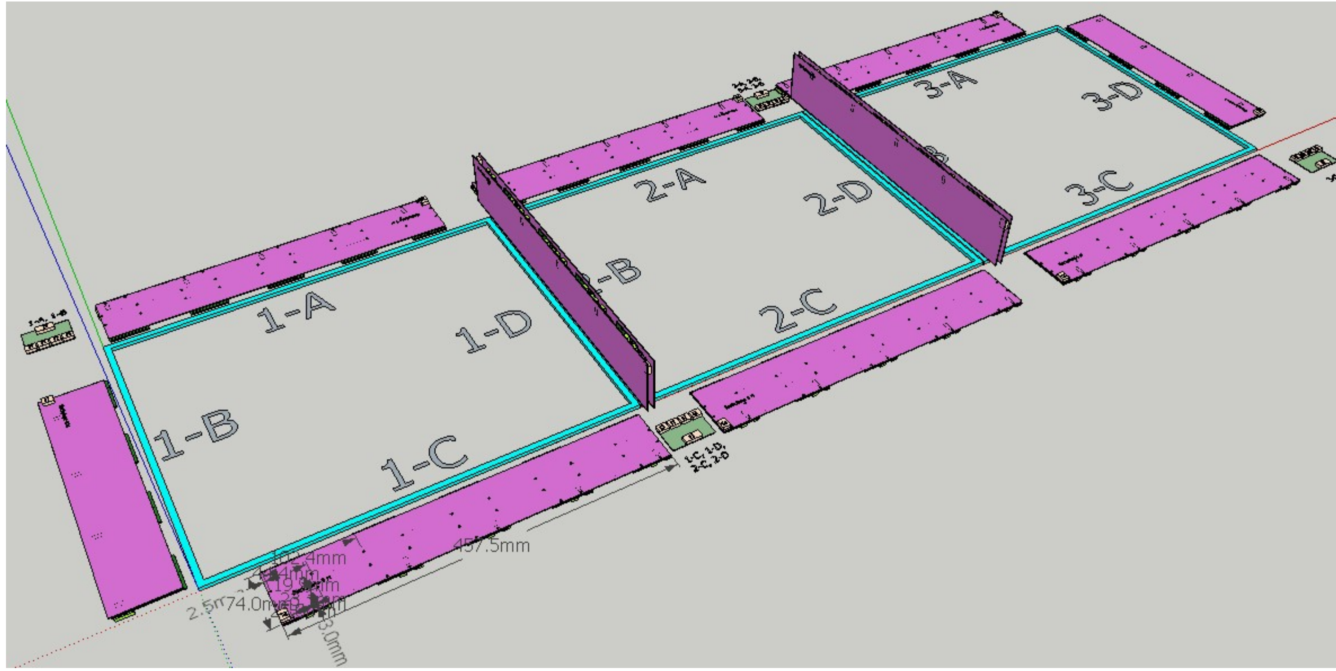
# Front-End adapter card (for testing)

- LEMO/TTL to Differential
- Differential Analog to Differential LEMO
- USB to I2C
- Single 3.3 V power line
- Very simple but useful



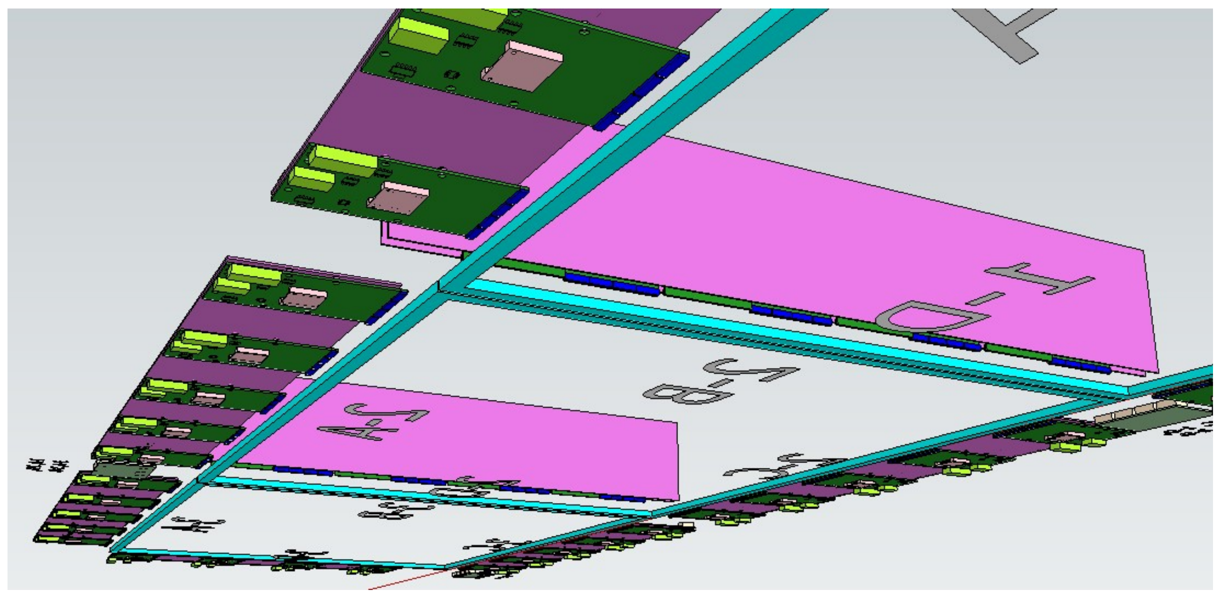
# Electronic layout on one chamber




Cards and modules are supported by an outer carbon-fiber frame which runs all around the chamber.

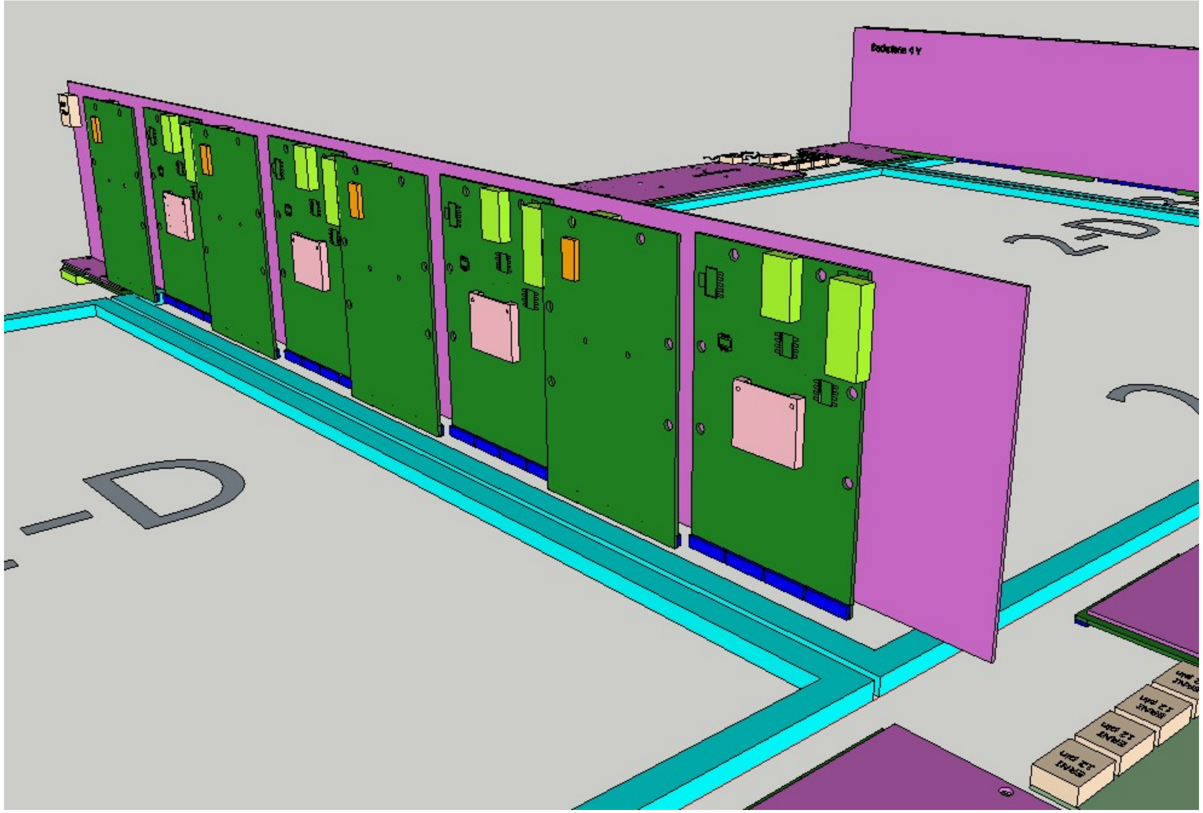
Optimization is in progress.



# FE – **Backplane** - VME

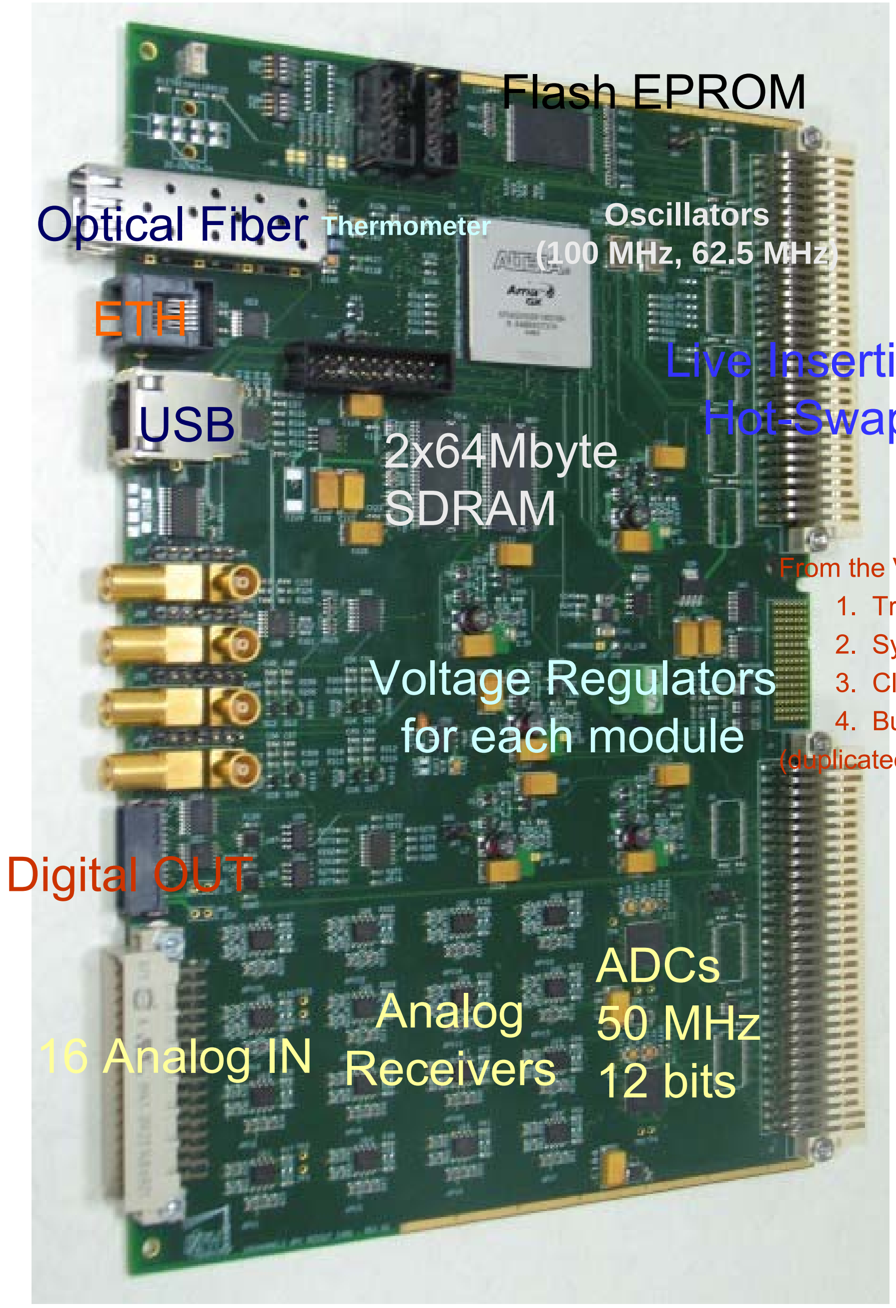
- In Proto 1 release a rigid PCB backplane for analog and digital lines (keep the cable option for testing) can be used
- Backplane is the mechanical supports for the vertical cards in between two GEM modules

•Controlled impedance



# VME64x Controller

- VME controller hosts the digitization of the analog signals coming from the front-end card.
- It handle all control signals required by the front end cards (**up to 16 FE**)
- Compliant to the new JLab/12 VME64x VITA 41 (VXS) standard
- We intend to make it accessible by standard VME as well
- Modular design: with the possibility to easily detach the analog module to extend FEC-VME64x distance
- **Under TEST**




From the VXS backplane:
1. Trigger L1/L2
2. Synch
3. Clock
4. Busy (OUT)

(duplicated on front panel)

# VME64x Controller / ALTERA Firmware

- Firmware on Verilog (under test):
  - VME-32 bit interface (64-bit interface very preliminary)
  - USB-interface (VME and USB share the same resources)
  - PLL configuration interface (APV-ADC clock phasing)
  - I2C master interface
  - Trigger handler (very simple) via front panel LEMO
  - ADC serial configuration interface and de-serializer
  - APV25 frame decoder; value stored on a FIFO accessible from VME and USB.
  - Single channel histogram (useful for delay tuning ...)
  - Front end test signals generator

# Electronics in short

- Front-end card prototype 0: tested, bug fixed and improvement defined
- Front-end card prototype 1: under test
- VME-controller prototype 0:
  - everything mounted except VME transceivers
  - most of the firmware modules implemented
  - under heavy test
- Usable system expected September/2010

## What is needed for GEM luminosity monitor

- For each GEM Luminosity 10x10 $cm^2$ module (400 μm pitch):
- 512 channels/chamber x 6 chambers = 3072 channels -> 4 front end cards + 1/4 VME module
- Total for 6 chambers: 24 fec + 1.5 VME modules
- Related low power supply units

# Test in July

- Reserved last two weeks of July at DESY test beam
- Expect to test SBS GEM module (40x50cm$^2$) which we are waiting from CERN (delay, not yet arrived) with new electronics
- If SBS module not available we will test new electronics with 10x10 cm$^2$ module (shipped back from JLab from PREX)