Recent status and discussion

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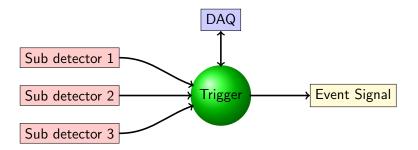


Outline

- Recent Status of Trigger System
- ② Discussion about Trigger Features
- Roadmap



What is the trigger?



Task: Generate Event signal if conditions are fulfilled.



How is the trigger realized?

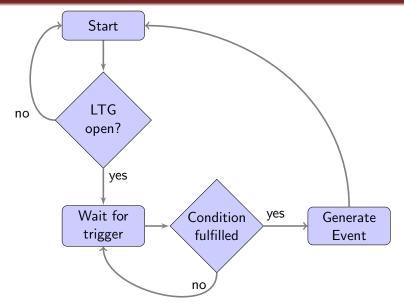


Trigger module

- Logic implemented in FPGA using VHDL
- VME interface for DAQ
- 16 NIM inputs for trigger signals
- 8 NIM outputs for event signal etc.



Trigger strategy





Clocking and re-timing

Synchronos (clocked) implementation of FPGA trigger logic.

 \Rightarrow 10 ns jitter between hit and event signal (100 MHz clock)

Option 1

Bunch clock on TDC

- relative TDC times
- larger ADC gate
- APV clocked 20/40 MHz

Option 2

Re-timing event signal

- ⇒ Chance of wrong re-timing or dead lock
- Sharper prompt peaks

Bunch timing uncertainty 2 ns due to 60 cm long target

⇒ No hardware re-timing needed!



Trigger conditions (Clocked Trigger Logic Block)

- 16 parallel CTLBs (*OR* of conditions)
- Fully configurable via VME registers

```
enable pattern(16)
                         trigger pattern(16)
     Pre-scale factor(24)
```

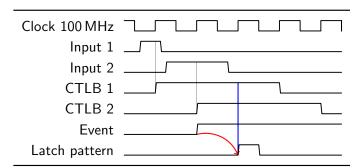
INPUT & enable pattern = trigger pattern?

- \rightarrow Bits: required (11), don't care (00), veto (10)
- Individual scaler for each CTI B
- Special CTLB: Scaler event with 32 bit pre-scaler (T \approx 42 s)



Trigger pattern

- Output: Pre-scaled trigger signal and direct trigger signal
- → CTLB bits latched into trigger patterns. **NOT the inputs!**





Signals from TOF

- OR left
- OR_right
- TopBottomCoinc_left
- TopBottomCoinc_right
- Forward left.
- Forward_right
- Backward left.
- Backward_right

Signals from Lumis

- GEMs left
- GEMs_right
- Scintillator_left
- Scintillator_right



Discussion: Clocking and re-timing

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enable pattern(16) trigger pattern(16)

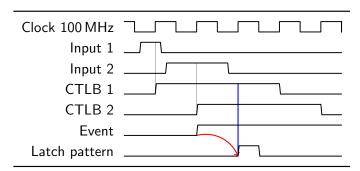
Pre-scale factor(24) ID C
```

INPUT & enable pattern = trigger pattern ?

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 - Individual scaler for each CTLB
 - ullet Special CTLB: Scaler event with 32 bit pre-scaler (T pprox 42 s)



- Output: Pre-scaled trigger signal and direct trigger signal
- → CTLB bits latched into trigger patterns. **NOT the inputs!**





Discussion: Trigger signals from sub-detectors

Signals from TOF

- OR_left
- OR_right
- TopBottomCoinc_left
- TopBottomCoinc_right
- Forward left.
- Forward_right
- Backward left.
- Backward_right

Signals from Lumis

- GEMs left
- GEMs_right
- Scintillator left
- Scintillator_right



Roadmap

- Prepare sub-detector trigger signals
- Obtain countrates during commissioning
- Simulate trigger efficiency and pre-scaling factors
- Generate list of trigger conditions
- Verify trigger contributions

3 and 4 need input and support from collaboration

⇒ Special trigger meeting!

