

A Through-Wafer Electrical Interconnect for Multi-Level MEMS Devices

Amit Mehra, Xin Zhang, Arturo A. Ayón, Ian A. Waitz
and Martin A. Schmidt

Abstract

This paper reports the design, fabrication and experimental demonstration of through-wafer interconnects capable of allowing direct electrical access to the interior of a multi-level MEMS device. The interconnects exploit the ability to conformally coat a high aspect ratio trench with a thick layer of TEOS to isolate a through-wafer silicon plug that can provide electrical contact across two sides of a low resistivity wafer. They hold the potential of a ten-fold reduction in the parasitic capacitance of previously reported through-wafer vias, and are shown to make reliable contacts to the back side of a polysilicon resistive element. The high temperature capability of the interconnects is also examined, however, their application is found to be limited to temperatures below 1000°C due to localized degradation near the isolating trenches.

Amit Mehra and Ian A. Waitz are with the Gas Turbine Laboratory, Department of Aeronautics and Astronautics, Massachusetts Institute of Technology.

Xin Zhang, Arturo A. Ayón and Martin A. Schmidt are with the Microsystems Technology Laboratories, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology.

I. INTRODUCTION

Electrical interconnects in multi-level MEMS devices are complicated by the difficulty in making sealed wafer level leads along bondlines. Specifically, the need for making electrical connections to the igniters and temperature sensors of a 6-wafer level micro gas turbine engine mandates interconnects that pressure-seal under the high temperature operating environment of the combustion chamber [1], [2]. Furthermore, as shown in Figure 1, since the combustion chamber in the engine is thermally insulated from the outer wall by a jacket of air, the electrical leads cannot be taken out laterally along bondlines because they would compromise the insulating property of this recirculating air-jacket.

In response to this need, this paper presents the design, fabrication and experimental testing of a novel through-wafer interconnect scheme that allows direct electrical access through the back side of a silicon wafer. The specific objectives of this paper are three-fold:

1. Present the design of the through-wafer interconnect,
2. Describe the fabrication of a single-wafer test device that utilizes the interconnects to make back side electrical connections to a polysilicon resistor, and
3. Identify operational issues that must be considered prior to their incorporation into other MEMS devices.

The paper is organized as follows: Section II describes the concept of the interconnect, Section III presents the fabrication process. The experimental test results are presented in Section IV; critical design and operation issues are identified in Section V.

II. DESIGN CONCEPT

The concept of the through-wafer interconnect is illustrated in Figure 2. The design is based on the ability to conformally coat a high-aspect ratio trench with a thick insulating layer in order to electrically isolate a circular plug of silicon. This plug is then released via a deep reactive

ion etch (DRIE) from the back side of the wafer to produce an isolated through-wafer contact capable of providing electrical access across two sides of a low resistivity silicon wafer.

The same Figure 2 shows a sample application of these interconnects to connect to a polysilicon resistive element on the other side of the wafer. The success of this design hinges on the ability to deposit conformal films that not only isolate the central plug, but also provide good coverage of the trenches to facilitate resist coating and patterning for subsequent process steps.

III. FABRICATION PROCESS

In order to demonstrate the viability of the through-wafer interconnects, a 4-mask test device was fabricated to make back side electrical contacts to a polysilicon resistive element of the type shown in Figure 2. The process is illustrated in Figure 3; the steps can be summarized as follows:

- (i.) Using DRIE, 100 μm deep circular trenches were etched into 300 μm n-type $\langle 100 \rangle$ silicon wafers that had a resistivity of 0.01-0.02 $\Omega \text{ cm}$.
- (ii.) A 10 μm coating of silicon dioxide was then deposited at 350°C in order to isolate the silicon plug from the rest of the substrate. This was done with a plasma enhanced chemical vapor deposition (PECVD) tool running tetraethylorthosilicate, also known as tetraethoxysilane. This type of silicon dioxide film is commonly known as TEOS.
- (iii.) Following the TEOS deposition, the oxide was chemically-mechanically polished (CMP) down to the silicon surface to allow subsequent photolithography steps.
- (iv.) 2 μm of TEOS were then additionally re-deposited and patterned to provide electrical access for the polysilicon.
- (v.) A 0.5 μm thick LPCVD polysilicon film was then deposited at 625°C, POCl_3 phosphorus-doped at 925°C, and patterned to define the resistive elements. Similar to designs reported by Cole *et al.* [3], the linewidth of the resistor was 20 μm ; the length was approximately 11 mm. The design sheet resistivity was 10 Ω/square ; the overall design resistance was approximately

5.5 k Ω .

(vi.) Finally, 100 μm wide, 200 μm deep, trenches were dry-etched from the back to isolate the silicon plugs and provide electrical contact across the two sides of the wafer.

Since the conformality of TEOS films in a high aspect-ratio trench needed to be understood, the first set of characterization dies contained eight different sets of interconnects with trench widths varying between 10 μm and 31 μm . As shown in Figure 4, “key-holing” of the TEOS was observed in trenches wider than 16 μm .

TEOS film are customarily densified immediately after deposition, among other things, to deplete the hydrogen content of the film. The original processing sequence included this densification step to be performed at 1100°C for one hour in a nitrogen ambient. Extensive TEOS cracking was observed after densification. Furthermore, upon completion of the subsequent polysilicon deposition (performed at 620°C) and diffusion doping (performed at 950°C) some cracks were covered and new ones were observed. Subsequent exposure of the devices to temperatures of 1100°C in an inert ambient caused the films to deteriorate even further (see Figure 5). The origins of these failures are threefold: (i) microdefects effected on the trenches during the polishing and removal (step iii in Figure 3) of the deposited 10 μm TEOS film, defects that could extend several microns into the trench and serve as crack initiation points, (ii) the shrinkage of the TEOS film due to the depletion of the hydrogen content (see Table 1) when exposing the film to high temperatures, and (iii) the appearance of cracks in the TEOS and polysilicon films induced by the mismatch in their coefficient of thermal expansion (CTE).

There are a number of alternatives for solving the observed film failures: (i) the damage induced by chemical-mechanical polishing could be alleviated by wet or dry etching the thick TEOS film, (ii) a thicker polysilicon deposition should be preferred for covering some if the cracks induced in the TEOS film during densification, (iii) the utilization of ion implantation instead of doping by diffusion with the associated drive-in temperature of around 600°C. Furthermore, such a low

drive-in temperature could also serve to densify the TEOS film. In general it can be concluded that higher operating temperatures are always expected to have deleterious effects on the integrity of the films involved.

TABLE I

Hydrogen concentration of PECVD-TEOS films versus annealing temperature (1 hour). (Note: The hydrogen content was measured with Rutherford backscattering spectroscopy with accelerated doubly ionized helium atoms (He^{++}))

T($^{\circ}\text{C}$)	350	700	900	1100
H ₂ (%)	4.00	0.67	0.20	0.17

In accordance with the previous considerations, all subsequent builds excluded film densification. Additionally, some devices also incorporated a 1 μm PECVD nitride coating prior to the TEOS deposition to relieve the residual stress in the film, and were observed to be more conformal.

IV. TEST RESULTS

Figure 6 shows a picture of a test die with eight different pairs of through-wafer interconnects, along with a close-up SEM micrograph of the interconnects and resistors.

The room temperature resistance across the back side contacts was measured to be approximately 6 k Ω . This was within 9% of the intended resistor design value of 5.5 k Ω ; the additional measured resistance was attributed to the polysilicon leads that connected the resistor to the plugs, the through-wafer silicon plugs, and probe contacts.

Among the devices that were fabricated without the nitride layer, only three out of the eight resistors on a die were successfully isolated from the surrounding substrate (10 μm , 13 μm and 16 μm trench widths). Figure 7 shows cross section micrographs of one such interconnect, showing

a continuous layer of polysilicon above the conformally coated isolating trench.

The remaining 5 resistors on the die, that had trenches of widths in excess of 20 μm , were found to be electrically open. This observation indicates that it is preferable to limit the width of the trenches to values such that they can be completely filled with a prescribed TEOS deposition (see Figure 8).

The working samples were tested by contacting the back side of the silicon plugs with probe-tips and passing electrical current across the two interconnects. Figure 9 shows voltage-current curves for the resistive element, and show that the results are repeatable between multiple runs and for different die. The non-linearity of the V-I curve is a result of Joule-heating in the resistor at high temperatures.

Overall, the figure demonstrates the reliability of the electrical connections made by the through-wafer interconnects. Efforts are currently underway to integrate the interconnects with the igniters and temperature sensors of the engine configuration shown in Figure 1.

V. CRITICAL DESIGN AND OPERATION ISSUES

The following observations should be taken into consideration prior to incorporating these interconnects into other MEMS packages:

- (1.) The through-wafer interconnects hold the potential of an order-of-magnitude reduction in parasitic capacitance over previously reported through-wafer vias. As shown in Figure 10, since the effective length of the plug is shorter than that of an equivalent through-wafer via [4], and since the oxide thickness can be ten times larger, the interconnects may be engineered with significantly lower parasitic capacitance.
- (2.) The interconnects also exhibit a reduced mechanical strength because the through-wafer plugs are only supported by the TEOS film in the isolating trench. As currently designed, the interconnects could only withstand mechanical loading not exceeding 1-2 Nt. (3-6 atm. for a

2 mm diameter plug). The structural capability of the isolation plugs could be increased by etching the isolation trench at an angle other than 90° to the plane of the wafer using schemes developed elsewhere [5]. This would permit the application of larger normal loads.

(3.) Electrical breakdown was observed to occur at voltages in excess of 300 V, preferentially in the vicinity of the isolating trench (Figure 11). The preferential location of the breakdown is related to the point of highest electric field intensity, which corresponds to the point where the polysilicon resistor joins the interconnect plug. The applied voltage and film thickness involved ($2\ \mu\text{m}$), represent an electric field intensity of the order of $10^8\ \text{V/m}$. Such a value for dielectric strength agrees with numbers reported in the literature for PECVD oxide film [6]. Furthermore, to verify the repeatability of these depositions, $0.9\ \mu\text{m}$ TEOS films were deposited on a set of 4 blank silicon wafers. One film was left undensified and the rest were densified one hour from 900°C to 1100°C . Subsequently, arrays of aluminum lines were patterned on top of the oxide films using a standard lift-off process. The tests corroborated breakdown strengths in the $10^8\ \text{V/m}$ range.

(4.) High temperature exposure of the interconnects to combustion gas temperature in the 1000°C - 1800°C range severely degraded the polysilicon film around the isolated trenches (see Figure 12), although the polysilicon resistor exhibited no visible deterioration. This localized degradation around the TEOS-filled isolation trench is consistent with the observed deterioration described in previous paragraphs. It is further thought that plasticity in the TEOS film at high temperatures led to polysilicon delamination, and that the presence of stress concentration points along the cracks formed during the exposure to high temperatures aggravated the observed film failure along the trench.

These observations were repeatable in an inert isothermal environment, wherein, progressive, isochronal exposure of the interconnects to temperatures of 200°C , 400°C , 600°C , 800°C , 1000°C , 1100°C and 1200°C for four hours resulted in similar localized degradation of the polysilicon

above the isolating trenches. Figure 13 shows SEM micrographs of an interconnect before and after high temperature exposure in an isothermal furnace, and shows the characteristic polysilicon degradation above the trench.

Since the onset of the degradation was observed at approximately 1000°C, the maximum operating range of the through-wafer interconnects in an inert ambient appears to be limited to $\leq 1000^\circ\text{C}$.

VI. CONCLUSIONS

This paper describes the development of a novel through-wafer interconnect scheme that could greatly facilitate electrical contacts in multi-level MEMS devices by allowing direct electrical access through the back side of a wafer. The technique requires conformal coating of a thick insulating oxide in a high aspect ratio trench so as to isolate a through-wafer plug capable of providing electrical access across two sides of a low resistivity silicon wafer. The interconnects have been shown to make reliable contacts to a polysilicon resistive element, however, as currently designed, material degradation of polysilicon on thick TEOS, and structural considerations limit their use to 3-6 atm., and temperatures below 1000°C.

ACKNOWLEDGMENTS

The authors are grateful to Professor Alan H. Epstein and Professor Stephen D. Senturia for their insightful suggestions, to Mr. Rory C. Keogh for help with the experiments, to Mr. Christopher M. Spadaccini for help preparing the manuscript, and to all the other members of the MIT microengine team for their help and support.

This work was largely supported by ARO, Dr. R. Paur technical manager, and by DARPA, Dr. S. Wilson technical manager. All devices were fabricated at the MIT Microsystems Technology Laboratories; the support of the technical staff is gratefully acknowledged.

REFERENCES

- [1] Epstein *et al.*, “*Micro-Heat Engines, Gas Turbines, and Rocket Engines*”, 28th AIAA Fluid Dynamics Conference and 4th AIAA Shear Flow Control Conference, Snowmass Village, 1997.
- [2] Mehra *et al.*, “*Combustion Tests in the 6-Wafer Static Structure of a Micro Gas Turbine Engine*”, International Conference on Solid-State Sensors and Actuators, Sendai, Japan, 1999.
- [3] Cole *et al.*, “*OBIC Analysis of Stressed, Thermally-Isolated Polysilicon Resistors*”, presented at the International Reliability Physics Symposium, Las Vegas, 1995.
- [4] Chow *et al.*, “*Fabrication of High-Density Cantilever Arrays and Through-Wafer Interconnects*”, presented at the Solid-State Sensor and Actuator Workshop, Hilton Head, 1998.
- [5] Ayón *et al.*, Proceedings of Transducers, pp. 854-857, Sendai, Japan, 1999.
- [6] Madou, *Fundamentals of Microfabrication*, p. 96, CRC Press, 1997.

Figure 1. A schematic cross-section of the 6-wafer combustion chamber for a microengine.

Figure 2. A schematic representation of a polysilicon resistive element connected by two through-wafer interconnects.

Figure 3. Fabrication process for the interconnect.

Figure 4. SEM micrographs showing the conformality of TEOS films deposited in the isolating trenches, and after the backside etch described in Figure 3.

Figure 5. Crack evolution on the isolation trench: (a.) No discontinuities detected after TEOS deposition, (b.) cracking and peeling-off of the TEOS film on the trench observed after densification at 1100°C, (c.) some ruptures are covered after polysilicon deposition (620°C) and doping (950°C) and new cracks appear, (d.) additional cracks observed on polysilicon after annealing at 1100°C.

Figure 6. A picture of a sample test die with eight sets of resistors and interconnects, along with a close-up SEM micrograph of one of the polysilicon resistors.

Figure 7. SEM micrographs of one of the isolated silicon plugs, showing continuity of the polysilicon above the TEOS-filled trench.

Figure 8. SEM micrograph of an electrically open trench that exceeds the maximum width recommended ($\leq 20 \mu\text{m}$) for a $10 \mu\text{m}$ TEOS deposition.

Figure 9. V-I curves for the resistors.

Figure 10. Compared to other through-wafer vias [4], the reduced length and thicker oxide of this interconnect scheme can significantly reduce its parasitic capacitance.

Figure 11. SEM micrograph of an interconnect after electrical breakdown at 300V.

Figure 12. SEM micrographs of the resistor, and left and right interconnects after eight hours of exposure to combustion gases, showing degradation of the polysilicon near the isolating trenches.

Figure 13. SEM micrographs of an interconnect before and after high temperature exposure in an inert isothermal furnace, showing localized polysilicon failure above the isolation trench.

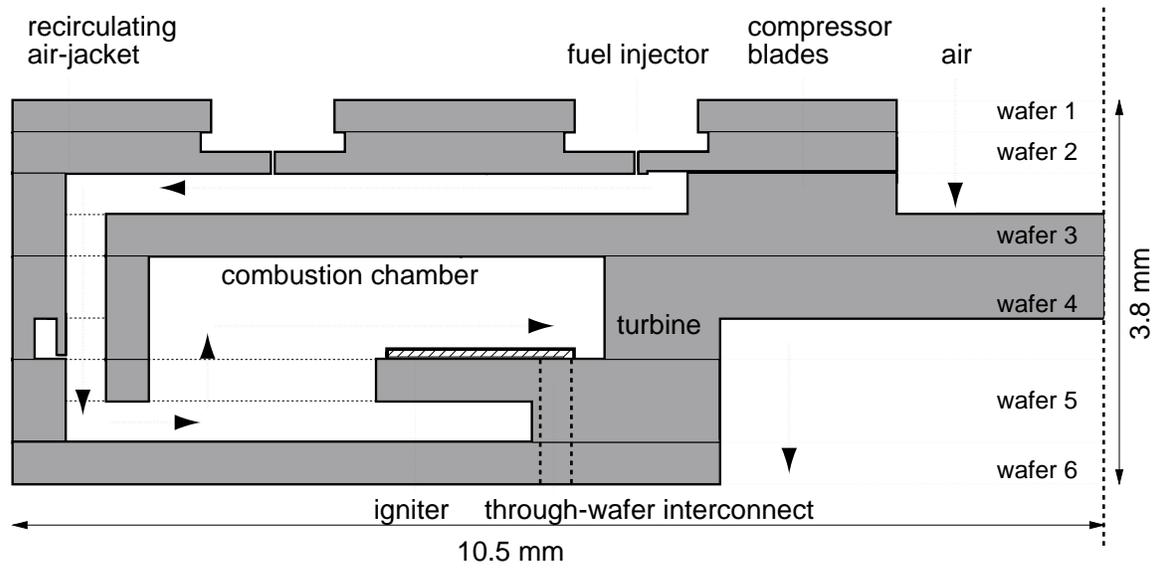


Fig. 1. A schematic cross-section of the 6-wafer combustion chamber for a microengine.

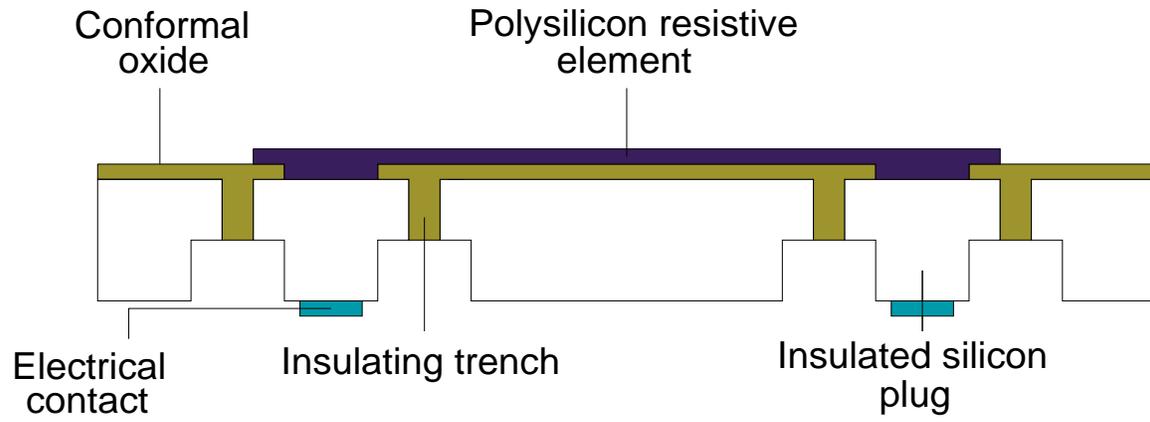


Fig. 2. A schematic representation of a polysilicon resistive element connected by two through-wafer interconnects.

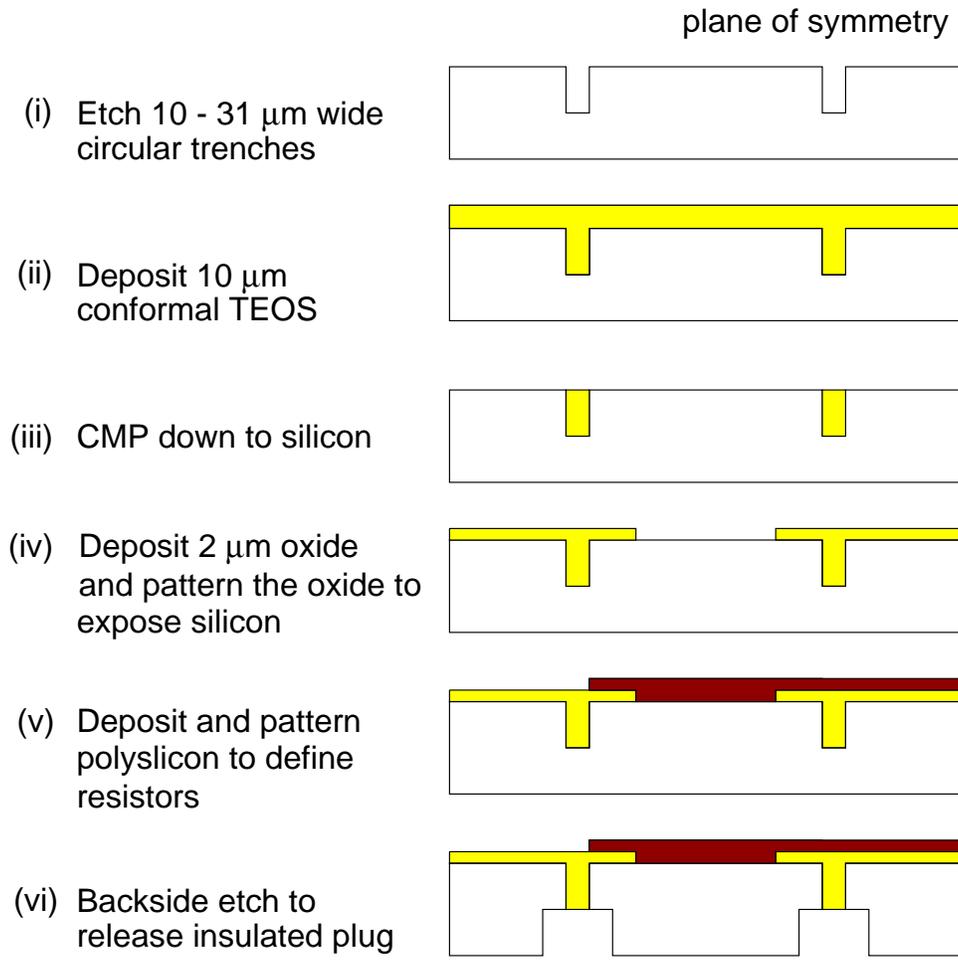
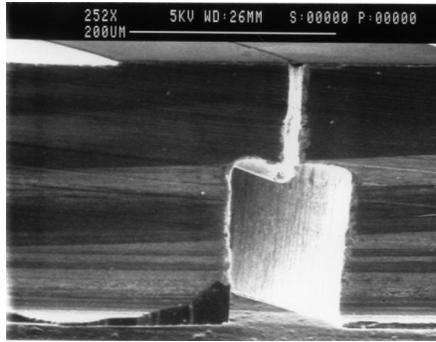
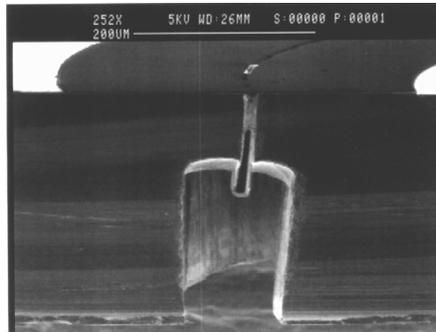


Fig. 3. Fabrication process for the interconnects.



(a) TEOS film conformally deposited in a $16\ \mu\text{m}$ wide insulating trench.



(b) TEOS film key-holing in an insulating trench $31\ \mu\text{m}$ wide.

Fig. 4. SEM micrographs showing the conformality of TEOS films deposited in the isolating trenches, and after the backside etch described in Figure 3.

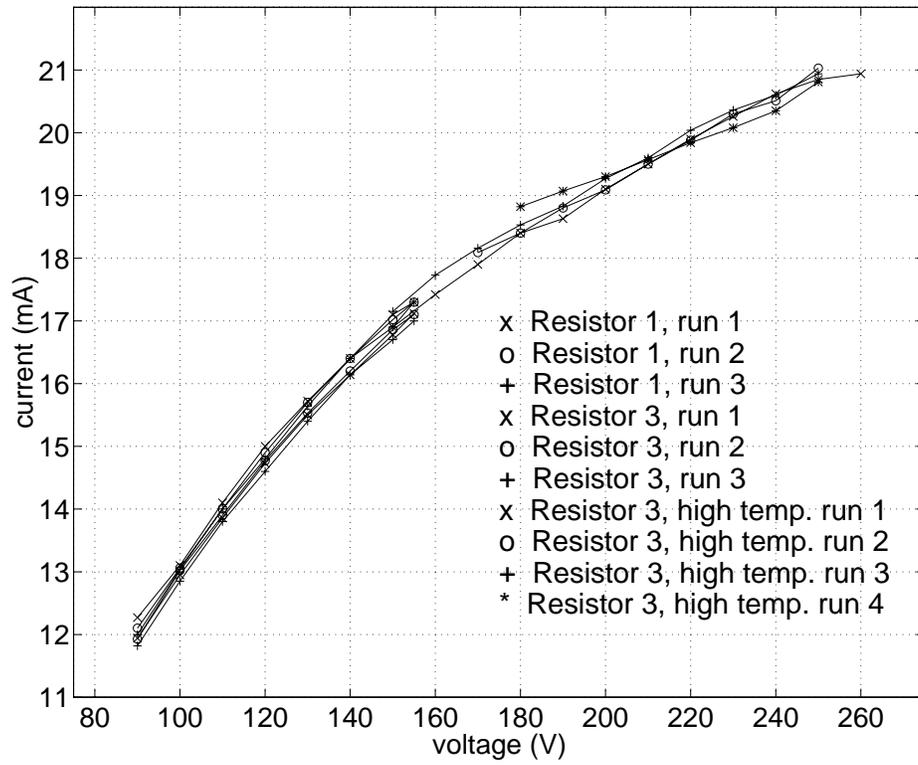


Fig. 5. DISREGARD THIS FIGURE. IT IS JUST TO FILL SPACE.

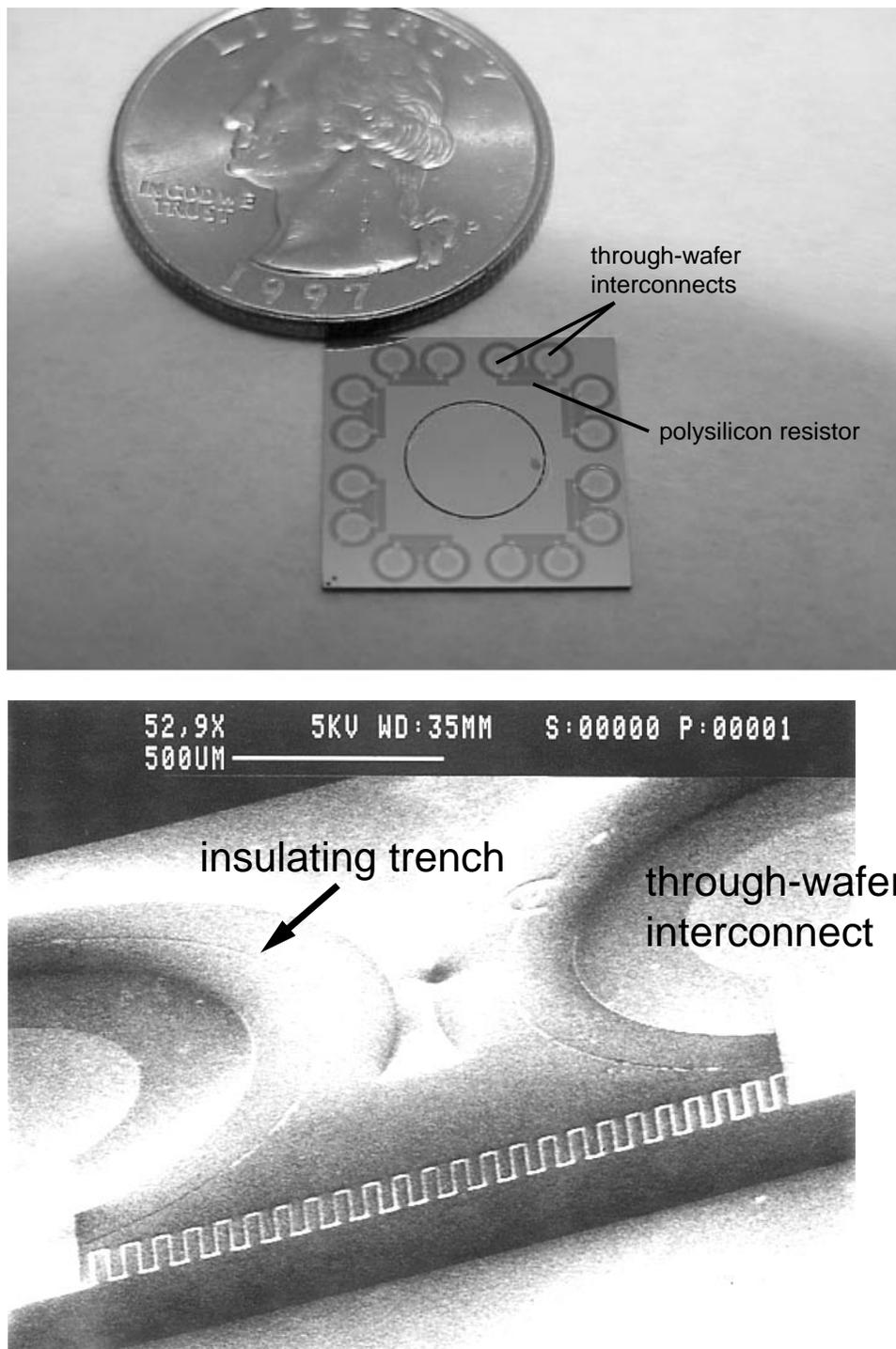


Fig. 6. A picture of a sample test die with eight sets of resistors and interconnects, along with a close-up SEM micrograph of one of the polysilicon resistors.

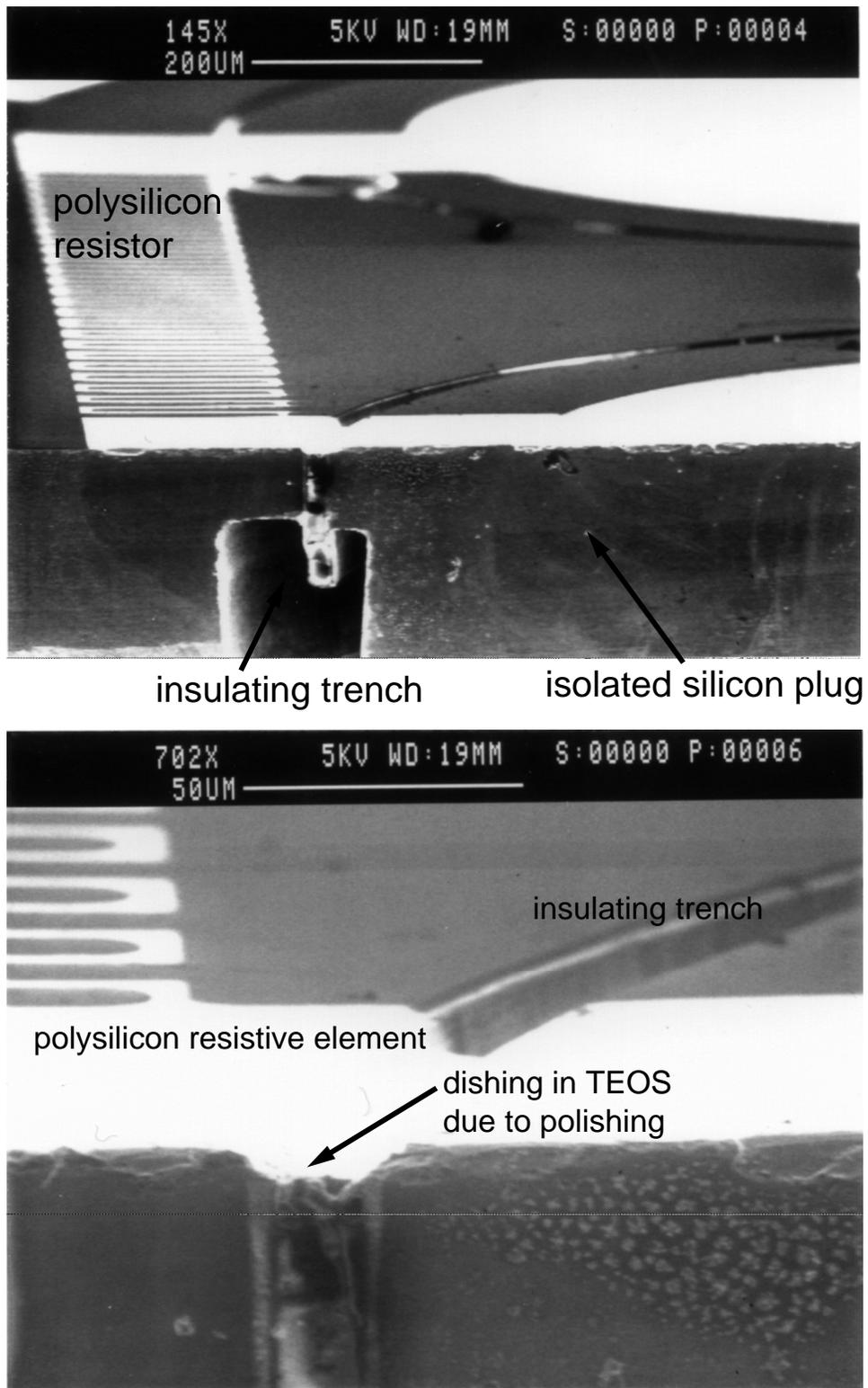


Fig. 7. SEM micrographs of one of the isolated silicon plugs, showing continuity of the polysilicon above the TEOS-filled trench.

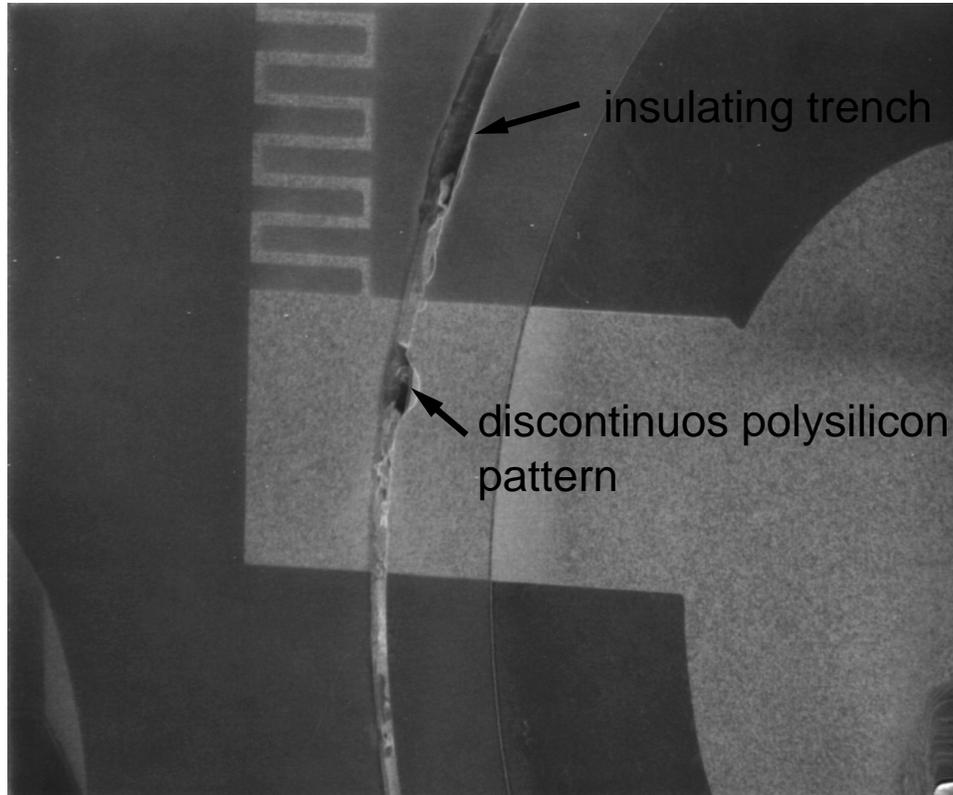


Fig. 8. SEM micrograph of an electrically open trench that exceeds the maximum width recommended ($\leq 20 \mu$) for a 10μ TEOS deposition

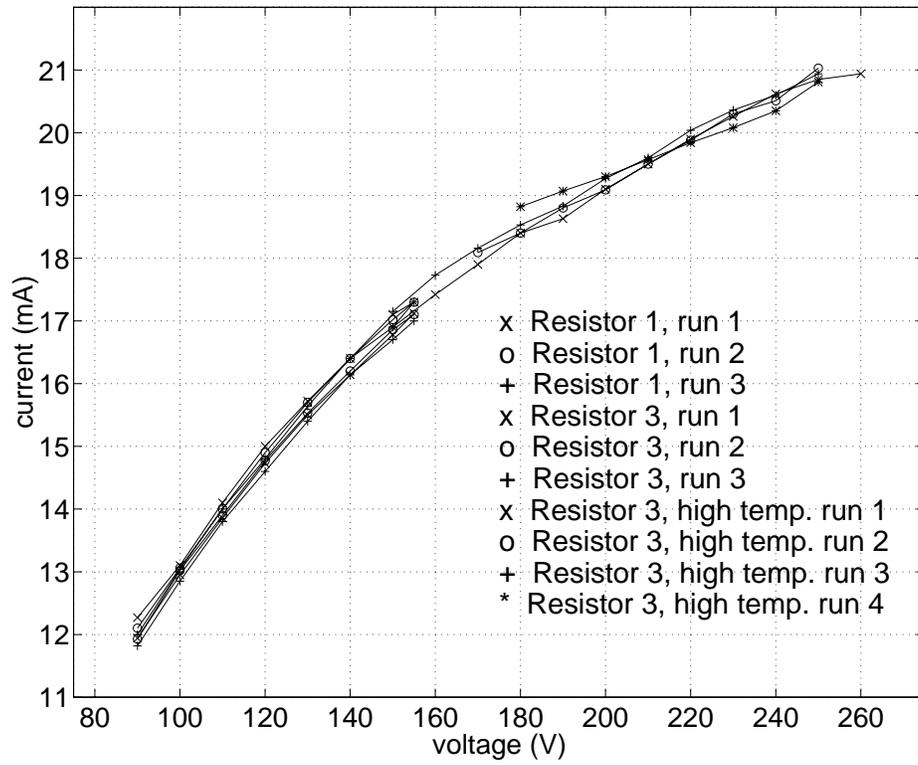


Fig. 9. V-I curves for the resistors.

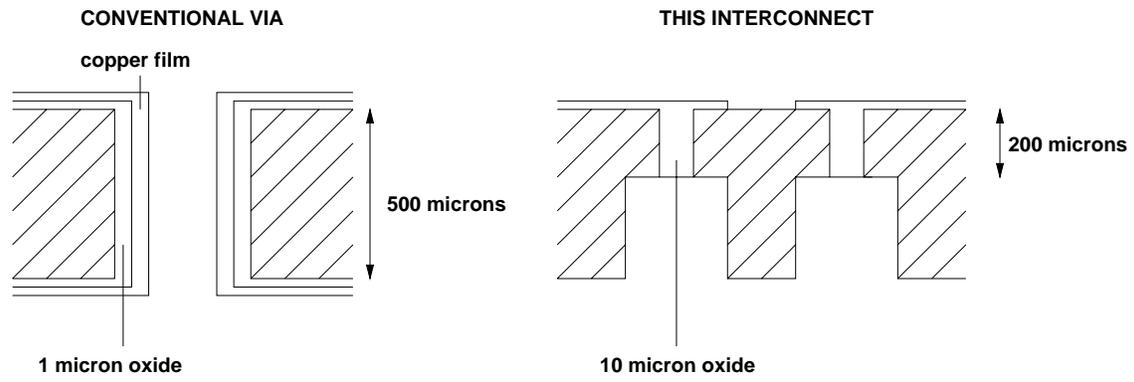


Fig. 10. Compared to other through-wafer vias [4], the reduced length and thicker oxide of this interconnect scheme can significantly reduce its parasitic capacitance.

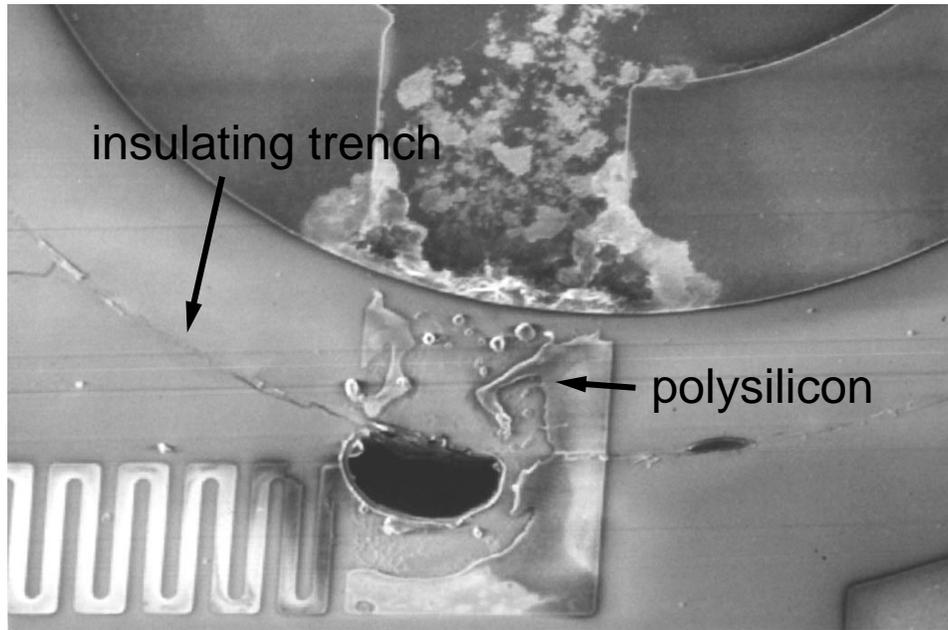


Fig. 11. SEM micrograph of an interconnect after electrical breakdown at 300V.

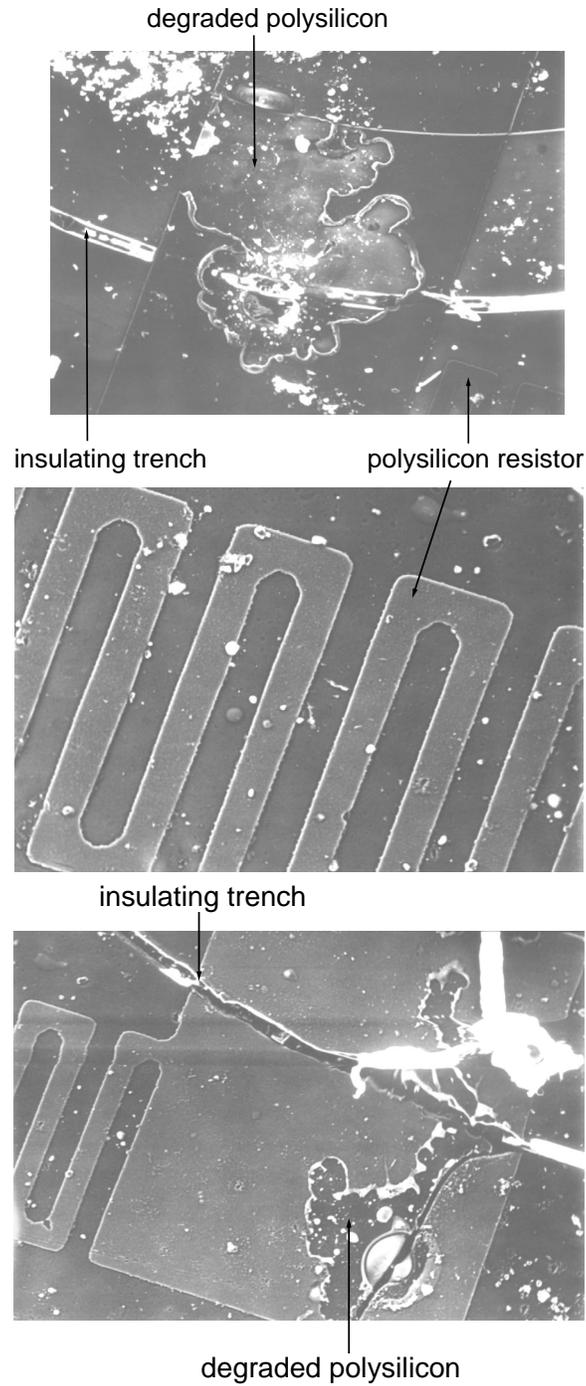
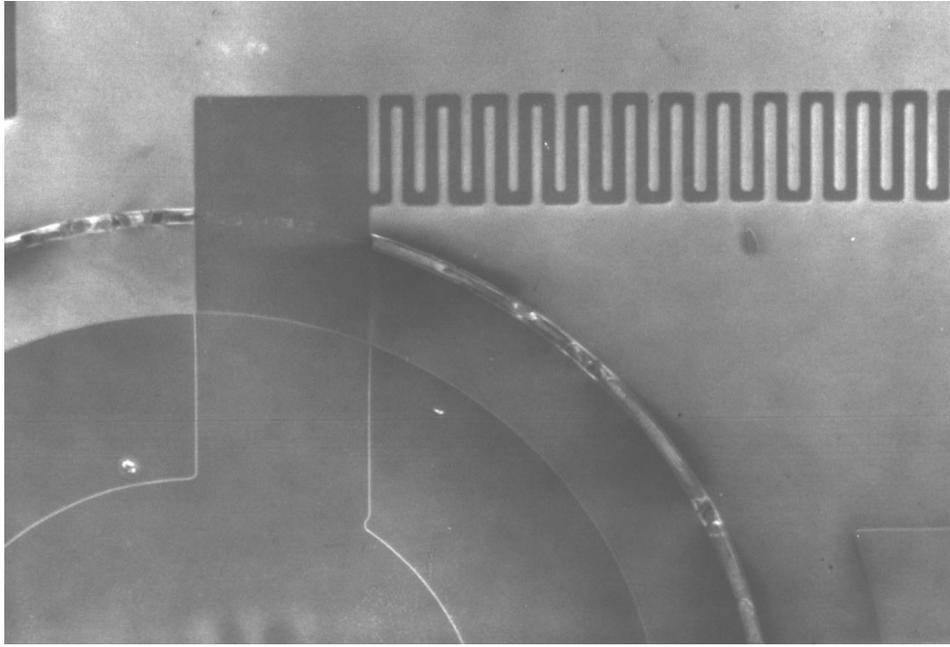
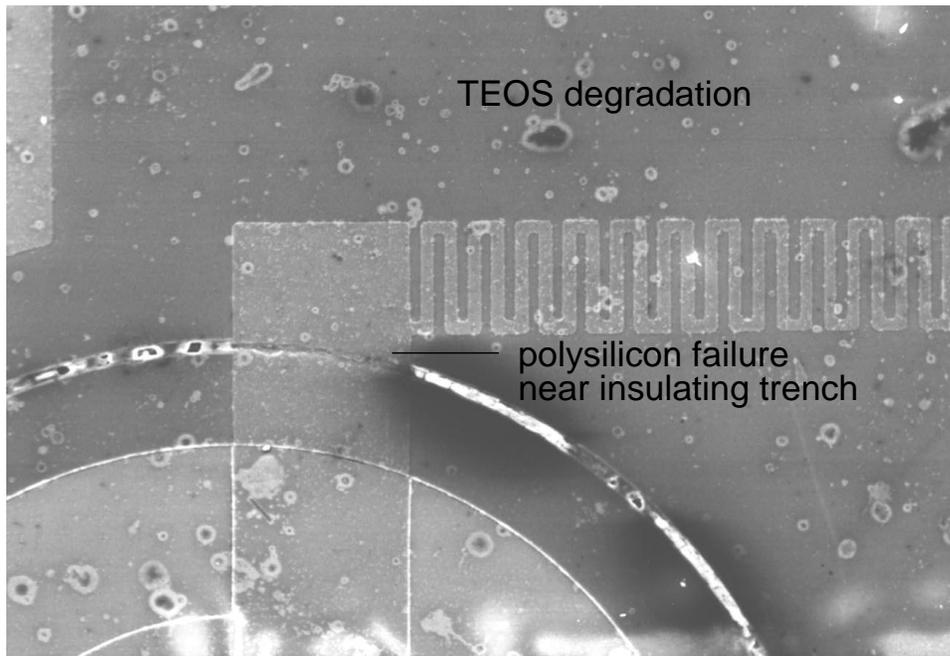


Fig. 12. SEM micrographs of the resistor, and left and right interconnects after eight hours of exposure to combustion gases, showing degradation of the polysilicon near the isolating trenches.



(a) Before high temperature exposure.



(b) After high temperature exposure.

Fig. 13. SEM micrographs of an interconnect before and after high temperature exposure in an inert isothermal furnace, showing localized polysilicon failure above the isolation trench.