40-Gb/s All-Optical Packet Synchronization and Address Comparison for OTDM Networks

S. A. Hamilton, *Member, IEEE* and B. S. Robinson, *Student Member, IEEE,*

***Abstract*—We demonstrate a novel optical time division multiplexing packet-level system-synchronization and address-comparison technique, which relies on cascaded semiconductor-based optical logic gates operating at 50-Gb/s line rates. Synchronous global clock distribution is used to achieve fixed length packet-synchronization that is resistant to channel-induced timing delays, and straightforward to achieve using a single optical logic gate. Four-bit address processing is achieved using a pulse-position modulated header input to a single optical logic gate, which provides boolean XOR functionality, low latency, and stability over $>$1 h time periods with low switching energy $<$100 fJ.**

***Index Terms*—Address comparison, all-optical logic, optical time-division multiplexing, packet synchronization, pulse-position modulation, ultrafast nonlinear interferometer.**

I. Introduction

ULTRAFAST optical time-division multiplexing (OTDM) networks have the potential to provide truly flexible bandwidth-on-demand at burst rates in excess of 100 Gb/s for high-end users, high-speed video servers, terabyte media banks, supercomputers, and aggregates of lower speed users [1]. Because 100-Gb/s channel rates exceed the current speed available from electronics, slot or packet-synchronization and header address-comparison at OTDM packet routers or receiver nodes must be achieved using optical techniques.

There have been several recent demonstrations of systems that provide both packet-synchronization and address-processing [2]–[5]. Each of these packet-level system-synchronization techniques [2]–[4] presents a system designer with significant challenges when the transmitter and receiver are separated by long optical fiber spans due to environmentally induced delay variations, polarization-mode dispersion (PMD), and Gordon–Haus-induced timing jitter [6]. In this letter, we present a novel packet-level, system-synchronization, and address-comparison technique used to achieve all-optical processing of 40-Gb/s data at 50-Gb/s line rates in our OTDM network testbed [5]. We use synchronous global clock distribution to achieve packet synchronization that is resistant to channel-induced timing delays, adaptable to asymmetric packet lengths, and multichannel OTDM transmission, and straightforward to achieve using a single optical logic gate. Header address processing is achieved using a pulse position modulated [7] header input to a single optical logic gate, which provides boolean XOR functionality, capability for all-optical processing at OTDM aggregate data rates, and stable switching with low latency and power.

Manuscript received July 30, 2001; revised September 21, 2001. This work was supported by the Defense Advanced Research Projects Agency (DARPA) under Contract F19628-00-C-0002.

The authors are with the Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, MA 02420 USA (e-mail: shamilton@ll.mit.edu).

Publisher Item Identifier S 1041-1135(02)00271-9.

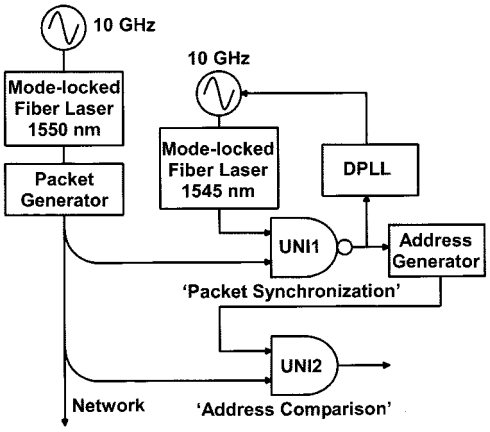

Fig. 1. Functional block diagram for the experimental setup used to demonstrate all-optical packet synchronization and address comparison for OTDM networks. The 1550- and 1545-nm mode-locked fiber lasers provide the control and signal inputs, respectively, to the ultrafast nonlinear interferometer (UNI) optical logic gates. The two lasers are bit-phase synchronized by the dithering phase-locked loop (DPLL).

II. All-Optical Packet-Synchronization and Address-Comparison Experiment

A functional block diagram of our packet-synchronization and address-comparison architecture is shown in Fig. 1. Incoming packets from the network channel at 1550 nm are split and input as the control pulse train into two ultrafast nonlinear interferometer (UNI) [8], [10] optical logic gates. The signal pulse train for each UNI is supplied by a mode-locked fiber laser local to the receiver that provides a 10-Gb/s pulse train consisting of 2.5-ps pulses at 1545 nm. Bit phasing between the network and local receiver pulse trains is maintained using an optoelectronic dithering phase-locked loop (DPLL).

The network packets contain a synchronous global 10-Gb/s clock interleaved between 40-Gb/s pseudorandom binary sequence (PRBS) data where each bit is a 2.5-ps pulse at 1550 nm and the overall line rate is 50 Gb/s. A single optical pulse is removed from the global clock to provide a temporal reference for the beginning of the network packet. This missing pulse provides a straightforward reference that is insensitive to timing jitter and PMD in the optical fiber channel separating the transmitter and receiver in an OTDM network. The PRBS data is modulated using the pulse-position modulation (PPM) format described in [7] with a 10-ps PPM delay to mitigate pattern-dependent-gain-saturation-induced amplitude patterning in the

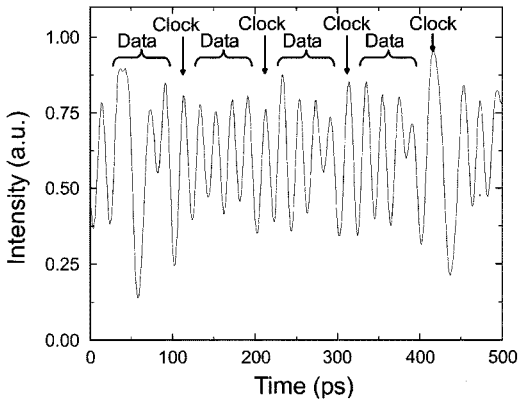

Fig. 2. Experimental digital sampling oscilloscope trace showing a 50-Gb/s line rate network packet containing interleaved 40-Gb/s pseudorandom binary sequence data and 10-Gb/s global-clock pulses. The trace resolution is limited by the 40-GHz photodetector bandwidth.

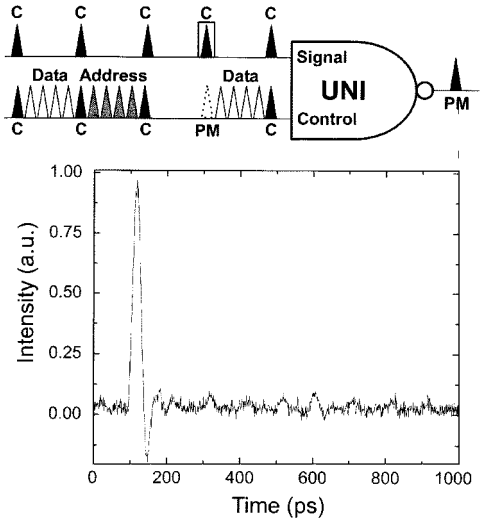

Fig. 3. Packet marker detection functional block diagram and experimental results. The global-clock and local-receiver clock pulses (C) are temporally aligned at the ultrafast nonlinear interferometer (UNI), and the missing packet marker (PM) pulse opens an optical switching window in the signal pulse train, which outputs a single PM pulse from the UNI. The digital sampling oscilloscope trace indicates the PM detection process is achieved with an 11-dB extinction ratio.

semiconductor-based UNI optical logic gates. 40-Gb/s serial data is simulated by passively multiplexing a 10-Gb/s PRBS to 40 Gb/s [11]. In the multiplexer, optical delays $7T/5$ and $4T/5$ (where $T = 100$ ps is the bit period at 10 Gb/s) are used to prevent adjacent bit-placement after multiplexing, thus maintainings the pseudorandom statistics of the aggregate data and providing an opening in each bit period for global clock insertion. A portion of an experimentally measured 50-Gb/s line rate packet showing interleaved 10-Gb/s global clock and 40-Gb/s PRBS PPM data is shown in Fig. 2.

System-synchronization to packet-timing is achieved at the UNI biased to perform the boolean NAND function shown in Fig. 1. At this optical logic gate, the system is initially synchronized via manual tuning of an optical delay line in order to temporally overlap the local-receiver-clock control pulse train and the global-synchronous-clock pulses in the network packet signal pulse train. Bit-phase synchronization is subsequently maintained by the DPLL. Because this UNI is biased as a NAND gate, a single signal pulse at 1545 nm is switched out of the gate only when the missing packet-reference pulse is present in the control stream at the UNI. This single pulse provides a temporal marker local to the receiver that signifies the beginning of a packet. Although this technique is adaptable to variable-length packets, we used a fixed 100-ns-long packet size in our experiment. As shown in Fig. 3, an extinction ratio of 11 dB is achieved for the packet-reference detection process with 2-fJ signal and 93-fJ control pulse train switching energies and a 5-ps temporal switching window at the packet synchronization UNI. We recognize that spectral efficiency is reduced using this packet-synchronization technique. Aggregate data rates of 1.28 Tb/s have been demonstrated for a single OTDM channel [12], however, and the inclusion of a 10-Gb/s global clock in this case results in only a 1% reduction in spectral efficiency.

All-optical address-comparison is achieved at the UNI biased to perform the boolean and function shown in Fig. 1. In this optical logic gate, the local-receiver address is temporally aligned to overlap one of the 10-Gb/s interleaved network packet address channels. The local address is generated from the single packet reference using standard optical multiplexing methods [11]. In this experiment, the local-receiver address

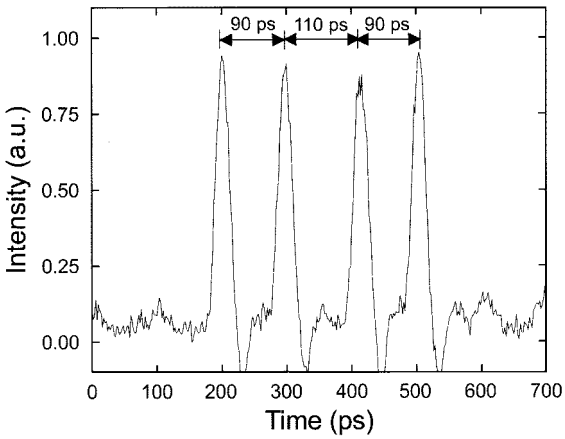

Fig. 4. Experimental digital sampling oscilloscope trace showing the local receiver optical address generated from the single packet marker pulse. The address corresponds to [0101] with a pulse position modulation delay of 10 ps.

[0101] is generated in the PPM format with a 10-ps PPM delay as shown in Fig. 4. The network-packet address is generated in this example by setting the pattern generator to create a 1,000 bit packet consisting of repeating copies of the [010 101 011] unit-cell, such that 111 copies of the unit-cell, plus one remaining bit are contained in each packet. This technique results in a four-bit network-packet address which changes from packet-to-packet by one sequential bit in the nine-bit unit-cell creating five distinct addresses (i.e., [0101], [1010], [1011], [0110], and [1101]). Each network-packet address is then bit-wise compared to the local-receiver address at the UNI with a 5-ps switching window biased for and operation as shown in Fig. 5. An extinction ratio of 7 dB is achieved between matched and unmatched address bits for the address-comparison with 19-fJ signal and 21-fJ control pulse train UNI switching energies. It should be noted that the UNI

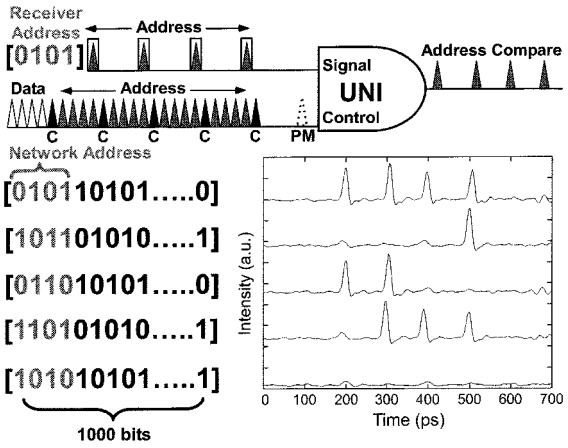

Fig. 5. Address-comparison functional block diagram and experimental results. One 10-Gb/s bit-interleaved channel in the network-packet address and the local receiver address are temporally aligned and bit wise compared at the ultrafast nonlinear interferometer (UNI) with boolean XOR functionality. The digital sampling oscilloscope trace indicates the address comparison results for five distinct network addresses, which is achieved with a 7-dB extinction ratio.

is shown to be stable over time periods longer than 1h, because each logic gate was biased for operation and untouched during the collection of all data shown in this example. In addition, the address space is scaleable and unlimited because keyword comparison [4] is not required. Finally, an important feature of this address-comparison technique is that boolean XOR logic is achieved from an optical and gate, because each address is generated using the PPM format in which a pulse is present for both logical "0s" and "1s." When either a "0" or "1" address match is detected, therefore, the UNI outputs a pulse and an address match is verified in this example when four optical pulses are output from the address-comparison UNI in Fig. 1. The upper speed limit for address comparison using PPM is set by the UNI and gate minimum switching window width, which is approximately equal to twice the optical pulsewidth at full-width at half-maximum (FWHM). Because we use 2.5-ps pulses in our experiment, this optical address comparison technique should be scalable to 200-Gb/s line rates.

III. Conclusion

In this letter, we demonstrate a novel packet-level, system-synchronization, and address-comparison technique that relies on cascaded semiconductor-based optical logic gates operating at 50-Gb/s line rates. Synchronous global-clock distribution is achieved for fixed length packet synchronization that is resistant to channel-induced timing delays, adaptable to asymmetric packet lengths, adaptable to multichannel OTDM transmission, and straightforward to achieve using a single optical logic gate. Four-bit address comparison is achieved using to a single optical logic gate, which provides boolean XOR functionality capability for all-optical processing at 200-Gb/s data rates, low latency, low switching energy < 100 fJ, and stability over >1 h time periods.

Acknowledgment

The authors would like to thank Dr. J. D. Moores, Mr. F. Hakimi, and Dr. P. A. Schulz for helpful discussions and Mr. C. Demers for technical assistance provided during this work.

References

[1] R. A. Barry, V. W. S. Chan, K. L. Hall, E. S. Kintzer, J. D. Moores, K. A. Rauschenbach, E. A. Swanson, L. E. Adams, C. R. Doerr, S. G. Finn, H. A. Haus, E. P. Ippen, W. S. Wong, and M. Haner, "All-optical network consortium—Ultrafast TDM networks," *IEEE J. Select. Areas Commun.*, vol. 14, pp. 999–1013, May 1996.

[2] T. J. Xia, Y. Liang, K. H. Ahn, J. W. Lou, O. Boyraz, Y.-H. Kao, X. D. Cao, S. Chaikamnerd, J. K. Andersen, and M. N. Islam, "All-optical packet-drop demonstration using 100 Gbit/s words by integrating fiber-based components," *IEEE Photon. Technol. Lett.*, vol. 10, pp. 153–155, Jan. 1998.

[3] I. Glesk, J. P. Sokoloff, and P. R. Prucnal, "All-optical address recognition and self-routing in a 250 Gbit/s packet-switched network," *Electron. Lett.*, vol. 30, no. 16, pp. 1322–1323, 1994.

[4] D. Cotter, J. K. Lucek, M. Shabeer, K. Smith, D. C. Rogers, D. Nesset, and P. Gunning, "Self-routing of 100 Gbit/s packets using 6 bit 'keyword' address recognition," *Electron. Lett.*, vol. 31, no. 25, pp. 2201–2202, 1995.

[5] S. A. Hamilton, B. S. Robinson, J. D. Moores, F. Hakimi, and P. A. Schulz, "Ultrafast synchronous all-optical time division multiplexing system demonstration," in *Tech. Dig., OFC'01*, Anaheim, CA, 2001, Paper WO3.

[6] J. P. Gordon and H. A. Haus, "Random walk of coherently amplified solitons in optical fiber transmission," *Opt. Lett.*, vol. 11, no. 10, pp. 665–667, 1986.

[7] B. S. Robinson, J. D. Moores, and D. T. Moriarty, "Pattern independent semiconductor-based interferometric all-optical switching using pulse position modulation," in *CLEO'00 Tech. Dig.*, San Francisco, CA, 2000, Postdeadline Paper CPD-19.

[8] N. S. Patel, K. L. Hall, and K. A. Rauschenbach, "Interferometric all-optical switches for ultrafast signal processing," *Appl. Opt.*, vol. 37, no. 14, pp. 2831–2842, 1998.

[9] K. Tajima, S. Nakamura, and Y. Sugimoto, "Ultrafast polarization-discriminating Mach-Zehnder all-optical switch," *Appl. Phys. Lett.*, vol. 67, no. 25, pp. 3709–3711, 1995.

[10] K. L. Hall and K. A. Rauschenbach, "100 Gbit/s bitwise logic," *Opt. Lett.*, vol. 23, no. 16, pp. 1271–1273, 1998.

[11] K. Suzuki, K. Iwatsuki, S. Nishi, M. Saruwatari, and T. Kitoh, "160 Gb/s sub-picosecond transform-limited pulse signal generation utilizing adiabatic soliton compression and optical time-division multiplexing," *IEEE Photon. Technol. Lett.*, vol. 6, pp. 352–354, Mar. 1994.

[12] M. Nakazawa, T. Yamamoto, and K. R. Tamura, "1.28 Tbit/s-70 km OTDM transmission using third- and fourth-order simultaneous dispersion compensation with a phase modulator," *Electron. Lett.*, vol. 36, no. 24, pp. 2027–2029, 2000.