Microsystems Technology Laboratories

The MIT Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory with a mission to foster research and education in semiconductor process and device technology and in integrated circuits and systems design. MTL provides micro- and nanofabrication and computer-aided design (CAD) infrastructure to the entire campus. MTL has 30 core faculty members who are engaged in diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, microelectromechanical systems (MEMS), and molecular and nanotechnologies. In addition, more than 110 affiliate faculty and senior research staff benefit from the fabrication facilities and CAD infrastructure provided by MTL. Last year, more than 500 researchers, primarily graduate students, conducted research using the MTL infrastructure. An underlying $55 million of annual sponsored research volume supports these fabrication and computational activities; sponsored programs administered directly through MTL have an annual research volume of approximately $12 million. MTL recovers approximately 75 percent of operating expense through charges to users and underwrites the remaining balance through use of unrestricted funds (approximately $1 million for FY2007).

MTL's fabrication environment includes three clean rooms totaling 7,800 sq ft: the state-of-the-art class-10 Integrated Circuits Laboratory, the class-100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation for device, circuit, and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL engages its users in a number of technical events. MTL hosts a regular seminar series spanning diverse technical areas related to devices and circuits. A committee chaired by Professor Joel Dawson arranges the seminar series. They are open to the public. In addition to these regular seminars, MTL also hosts occasional Distinguished Seminars. In February 2007, MTL cohosted (along with the Research Laboratory of Electronics and the Industrial Liaison Program) the visit of Rich Templeton, CEO of Texas Instruments. MTL holds an annual research conference (MARC) run by MTL graduate students in conjunction with a steering committee. The conference is widely attended by industry, faculty, students, and staff. It is a unique opportunity to learn about research in the diverse areas encompassed by MTL and helps encourage interaction among the MTL community.

MTL partners with industry through the Microsystems Industrial Group (MIG). MTL research and operation is significantly subsidized by the MIG consortium. The MIG donates major pieces of equipment to MTL, contributes directed fellowships, and provides access to state-of-the-art IC chip fabrication service. This year, two new members, NEC and Cadence, have joined the MIG. The members of the Industrial Advisory Board (one member from each of our MIG companies) provide significant guidance in shaping the vision of MTL.

Research conducted at MTL can be broadly classified into five categories: circuits and systems, electronic devices, MEMS and BioMEMS, molecular and nanotechnology, and photonics. MTL has four affiliated industrial research centers with more focused interests: the Center for Integrated Circuits and Systems, Intelligent Transportation Research Center, MEMS@MIT, and the Center for Integrated Photonic Systems.

Administration, Management, and Operations

Professor Anantha Chandrakasan is the MTL director with oversight for the daily administration and management of the lab. Two faculty associate directors, professors Jesus del Alamo and Judy Hoyt, assist the director in managing the computational and fabrication infrastructure, respectively. Two staff associate directors provide direct support for the fabrication facilities (Dr. Vicky Diadiuk) and administrative services and industry liaison (Mr. Samuel Crooks).

MTL maintains several committees charged with policy development and implementation including the Policy Board (chair, A. Chandrakasan), the Process Technology Committee (chair, V. Diadiuk), the Computation Committee (chair, J. del Alamo), and the Operations Committee (chair, S. Crooks); MTL also has a Social Committee (chair, Debroah Hodges-Pabon) that builds community spirit among our many users and a Publications Committee (chair, Mara Karapetian) working on MTL's Annual Research Report (http://mtlweb.mit.edu/research/ar.html), Newsletter, and other publications. The members of the MTL community are also involved in a number of other functional committees.

Shared Service Facilities

MTL's microfabrication, testing, and computational facilities are open to the entire MIT community as well as researchers from other universities and government laboratories through the MTL Outreach Programs. Similarly, the Fabrication Facilities Access Program enables local industrial access to the clean room facilities.

MTL has committed significant resources to the acquisition and maintenance of capital equipment. These capital improvements, upgrades, and purchases allow MTL to serve an increasingly diverse user base. As mentioned earlier, many of the MIG member companies donate capital equipment that is used in both the fabrication and the computation facilities. MTL's capital base, acquired primarily through donation and MTL funds, has provided the Institute a valuable source of depreciation that is fully recoverable through facilities and administration.

Fabrication Facilities

MTL's fabrication resources are managed and operated by a group of professional technical staff. All researchers planning to use the MTL fabrication facilities are required to successfully complete a safety and orientation course before they use MTL facilities and must receive training from a research specialist for each piece of laboratory equipment they plan to operate. The facilities support research on projects involving a range of substrates including silicon, germanium, III-V semiconductors, organics, and glass; they include capabilities for deposition of a wide range of materials such

as dielectrics, plastics, semiconductors, metals, and carbon nanotubes. The Process Technology Committee includes students, faculty, and staff and meets weekly to review user process flows in addition to requests for new materials, protocols, and fabrication operational issues.

Computation Facilities

MTL also maintains a comprehensive computation infrastructure, providing a broad array of services to the community. MTL supports the CAD tools required for circuit and system design. Seamlessly connected to the computation infrastructure is MTL's common object representation for advanced laboratories (CORAL), with which the users of MTL's fabrication facilities interface with the fab tools to perform their processes (e.g., reserve time on machines in the fab). The user log is coupled to a sophisticated charging algorithm that calculates user fees on a monthly basis. CORAL was developed in collaboration with Stanford University and continues to evolve as the needs of MIT's microfabrication community require.

Highlights of Research

Trends and Requirements of Future MOSFETs: Dimitri A. Antoniadis

A simple analytical model based on six physical parameters is introduced that describes metal oxide semiconductor field-effect transistor (MOSFET) operation in saturation from subthreshold to strong inversion. The model is used to derive a new formulation of the intrinsic switching delay of MOSFETs, which is used as a metric of device performance. It is shown that the carrier velocity in the MOSFET channel at the top of the barrier near the source (virtual source) is the main driving force for improved transistor performance with scaling. A historical trend of channel velocity including the most recent results of strain engineering is derived and is used to examine the tradeoffs between key device elements required for the performance scaling trend to continue in future "high-performance" complementary metal oxide semiconductor (CMOS) generations.

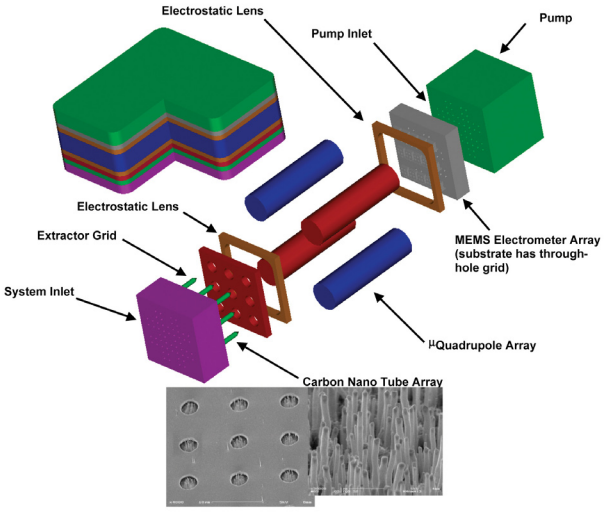
Micro Gas Analyzers: Akintunde Ibitayo Akinwande

The micro gas analyzer project in MTL is developing technologies for real-time, tiny (2 cm^{-3}) and very low power (1 W), high-resolution (0.5 Da) mass spectrometers that operate at high pressure (100 mTorr), low detection limit (1 part per trillion), and short total analysis time (4 s). The overall goal is to scale conventional devices to smaller dimensions and use massively parallel arrays of scaled devices to improve sensitivity. This will lead to reduced size, lower voltage of operation and power, increased sensitivity and specificity, and the ability to operate at higher vacuum pressures reducing the pumping requirements at the microscale level. The sheer portability of these sensors should introduce a host of new applications and deployment scenarios such as wearable chemical and biological sensors or remote unattended gas sensors with wireless interrogation capability.

The team led by MIT, including partners at the University of Texas at Dallas, Cambridge University, Clean Earth Technology, and Raytheon, has recently demonstrated the following key components: (a) ionization source for chemical and biological species in the gas stream based on gated arrays of field emission devices and field ionization

devices, (b) a microfabricated mass filter based on arrays of linear quadrupoles, (c) a microfabricated mass detector that has an embedded resonant microstructure, (d) a microfabricated vibrating reed electrometer for charge detection, and (e) a microfabricated vacuum pump.

Performance Variation in High-Speed Circuits: Duane Boning



Duane Boning and his group are developing test circuits and analysis methods to understand manufacturing variation and its impact on integrated circuits. One aspect of this work focuses on variation in high-speed circuits, including key components in the radio frequency front end for millimeter-wave circuits. In collaboration with IBM, a test chip fabrication in 65-nm silicon on insulator (SOI) CMOS technology was designed and fabricated, with a 2:1 static current-mode logic divider circuit and a voltage-controlled oscillator (VCO) circuit. These subcircuits operate near the limits of the technology and can be quite sensitive to device and passive variations, making them good probes to study manufacturing variation in the process. Measurements indicate substantial variation in the self-oscillation frequency of a feedback-connected divider (in the range of 50 to 70 GHz) and in the VCO. Interestingly, the VCO and divider circuits show different sensitivities for variation and are not correlated with each other, which imposes additional challenges to achieve robust integration and high yield. This work was reported at the International Solid-State Circuits Conference (ISSCC) 2007 and Radio Frequency Integrated Circuits 2007 Conference (see figure 2).

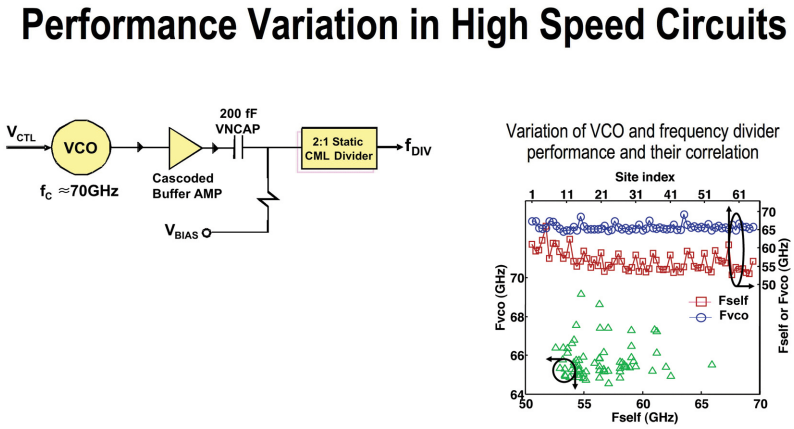


Figure 2: Exploration of variation in key components of a high-speed radio frequency front end, including (VCO) and 2:1 static current-mode logic frequency divider. (Right, top) Self-oscillation frequency of divider and VCO frequency for different chips across the wafer, indicating different sensitivities of these circuits to process variation. (Right, bottom) Lack of correlation is seen between VCO and divider frequency variations.

Ultra-Low-Power Impulse Radio: Anantha P. Chandrakasan

We have developed a low-power radio using impulse-based ultra-wideband (UWB) technology. By eliminating components with long startup times, such as a phase-locked loop, all components in a pulsed-UWB transceiver can be disabled during the interval between pulses. The transmitter chip used an all-digital architecture that requires no analog bias currents—that is, energy is dissipated only in switching events, i.e., CV^2, and by subthreshold leakage currents. This transmitter supports three channels in the 3- to 5-GHz band and requires only 43 pJ/bit at a data rate of 16.7 Mb/s. The receiver integrated circuit uses a noncoherent architecture that operates down to 0.5 V. Using duty-cycling, adjustable bandpass filters, and a relative-compare baseband, the receiver achieves 2.5 nJ/b at 100 Kbs. The transmitter and receiver integrated circuits were fabricated in a 90-nm CMOS process. A complete wireless system has been demonstrated using two integrated circuits. This work was reported at ISSCC 2007 (see figure 3).

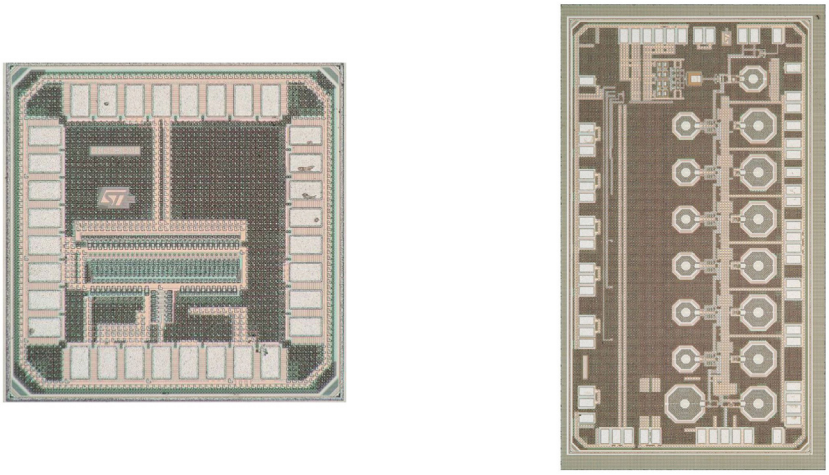


Figure 3: Die photograph of (left) the UWB transmitter and (right) the UWB receiver.

An Organic Imager for Flexible Large-Area Electronics: Akintunde I. Akinwande, Vladimir Bulovic, Charles G. Sodini

Interest in organic semiconductor technologies is sustained in part by the promise of large-area and flexible electronics. Early work has focused on the fabrication and characterization of discrete devices such as a single organic field effect transistor (OFET) or organic photodetector (OPD). Creating an addressable imaging system, however, requires an integrated approach for both device fabrication and testing. In this work, we demonstrate a near room temperature (<95ºC) process flow fabricating integrated OFETs and OPDs by using a combination of photolithography and ink-jet printing techniques, both suitable for use on mechanically flexible substrates. We fabricate and test a proof of concept active-matrix imager consisting of OFET switches with OPDs, two metal layers, and patterned lateral photodetectors. We measure the OPD responsivity of 6×10^{-5} A/W and an on/off ratio of up to 880 (see figure 4).

Beyond Si: Compound Semiconductor Transistors for Logic Applications: Jesus A. del Alamo

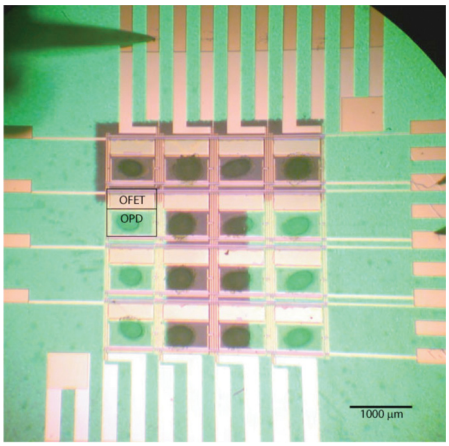


Figure 4: Die photograph of imaging array under test.

The microelectronics revolution has, for the last 40 years, brought us exponential improvements in the performance, functionality, and power efficiency of integrated electronics with an impact that reaches deeply into many aspects of human life. Moore's law has been fueled by the extraordinary size-scaling properties of silicon-based transistors.

Unfortunately, silicon technology is about to hit fundamental limits that will drastically slow down, if not altogether halt, progress. To address this problem, Professor del Alamo's group at MIT is investigating transistors based on III-V compound semiconductors—in particular, InGaAs. This is a material in which electrons travel at speeds many times faster than in Si. In MTL, Professor del Alamo's students have fabricated InGaAs transistors with a critical dimension of 60 nm. They found that these transistors exhibit logic figures of merit that in many respects exceed those of state-of-the-art Si transistors, even though they operate at a lower voltage of 0.5 V. Professor del Alamo's current research targets even smaller devices. His group's goal is 20 nm and the development of a manufacturing process suitable for the integration of millions of these transistors (see figure 5).

Nano/Microfluidic Systems for Protein Sample Preparation: Jongyoon Han (Department of Electrical Engineering and Computer Science/Department of Biological Engineering)

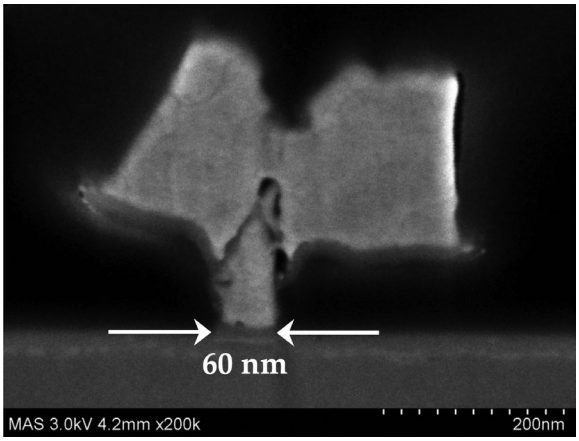


Figure 5: Cross-sectional view of new InGaAs transistor showing critical gate dimension of 60 nm.

Sample preparation is currently the most challenging bottleneck of any biological research, which critically limits the pace of our study on biological systems. Also, molecular diagnostics (biomarker detection) is severely hampered by the complexity of typical biosamples such as blood, saliva, and urine. Automatic, integrated sample fractionation and preconcentration tools will enable many novel molecular diagnostic tools and sensors, which will have a significant impact on early diagnosis of common diseases. Our research focus has been the integration of many nano/microfluidic tools for proteomic sample preparation we developed over the past three years to build truly integrated, automatic sample preparation microdevices. Efforts are under way to integrate protein preconcentrator and standard immunoassays, as well as the integration efforts for preconcentration with mass spectrometry tools. The most interesting result of the last year was the publication of anisotropic nanofilter array (Fu, J., R.R. Schoch, A.L. Stevens, S.R. Tannenbaum, and J. Han. 2006. Patterned

anisotropic nanofluidic sieving structure for continuous-flow separation of DNA and protein. *Nature Nanotechnology* 2(2):121–128.) This paper introduces a novel concept for biomolecule separation by creating a sieving structure that is anisotropic (meaning molecular sieving properties in the system will depend on the direction of motion of molecules), enabling high-throughput size separation of proteins and other smaller biomolecules (see figure 6).

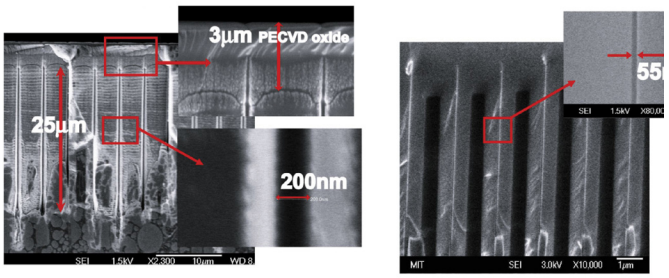


Figure 6: Cross-sectional scanning electronic micrograph of slot-like vertical nanochannels with a gap size of 200 nm (left) and 55 nm (right). The depths are 25 µm by 15-min KOH etching. The close-up shows complete trench sealing by 3 µm PECVD oxide.

Breaking the Analog Circuit Bottleneck: Hae-Seung Lee

Analog circuits are an essential part of most electronic systems. Unfortunately, they are not power efficient and often are the major power consumers of the system. Operational amplifiers (Op Amps) are one of the major sources of power inefficiency in analog circuits. Professor Lee's research group, in collaboration with Professor Charles G. Sodini, developed a new class of analog circuits called comparator-based switched capacitor (CBSC) circuits to eliminate the bottleneck caused by Op Amps. They observed that an accurate output voltage is necessary only at the sampling instant by the next sampling circuit. Thus, in a CBSC, a comparator detects the virtual ground crossing rather than driving as an Op Amp does. A CBSC is more power efficient by as much as an order of magnitude or more. The CBSC technique has a wide range of applications including A/D converters, D/A converters, discrete-time amplifiers, and filters (see figure 7).

Making Better Use of Time in Mixed-Signal Circuits: Michael H. Perrott

As analog device characteristics are expected to steadily degrade in future CMOS processes, there is a pressing need to develop mixed-signal circuit architectures that leverage digital circuits to improve analog processing of signals. To address this issue, Professor Perrott's group at MIT is investigating the use of time as a signal domain to perform operations such as the digitization of analog signals. At the recent 2007 VLSI Symposium, Professor Perrott's group demonstrated an analog-to-digital converter (ADC) circuit that used the relative timing of signal edges from a VCO to perform fast and efficient quantization of

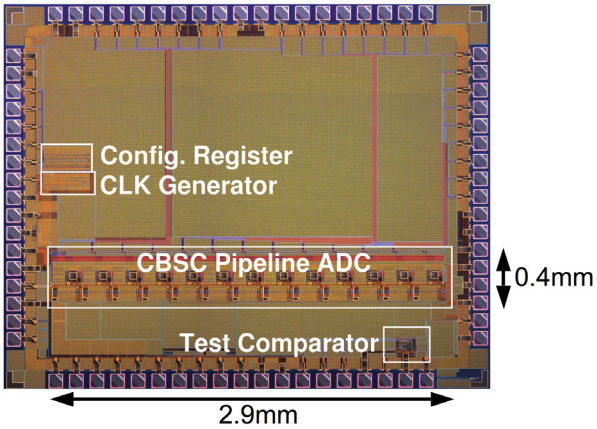


Figure 7: Microphotograph of the original comparator-based pipeline ADC [T. Sepke, ISSCC 2006]. Performance: 10 bit, 8 MHz, 2.5 mW.

an input analog signal. Compared with a more conventional ADC circuit presented at the same conference, the VCO-based structure achieved higher performance (i.e., 12-bit conversion with 10-MHz signal bandwidth) with significantly better power and area efficiency. Professor Perrott's current research targets even higher performance (i.e., 14-bit conversion with 20-MHz signal bandwidth) with better power efficiency through continued architectural innovation of VCO-based quantizers (see figure 8).

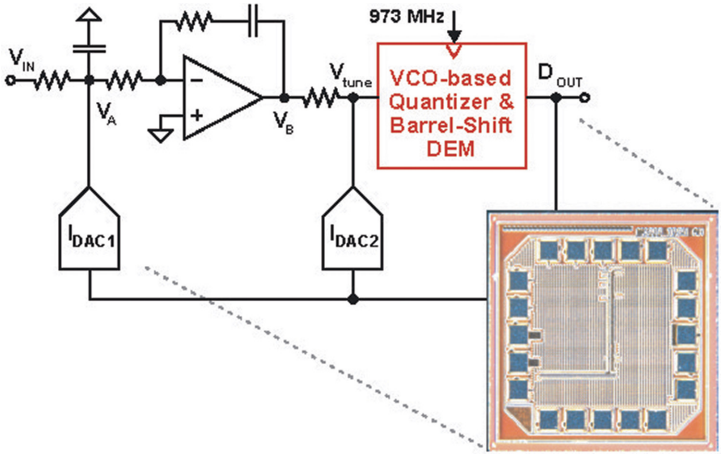


Figure 8: Proposed VCO-based ADC achieving 12-bit performance with 10-MHz signal bandwidth (presented at VLSI 2007).

MoJet: A Molecular Jet Method for Evaporative Printing of Organic Materials at Atmospheric Pressure: Martin Schmidt and Vladimir Bulovic

Organic semiconducting materials hold great promise for a wide range of electronic and optical applications because of their capacity to be deployed in large-area integrated devices, such as information displays and chemical sensor arrays, and compatibility with deposition on arbitrary substrates, such as flexible plastic surfaces or metal foils that could be used for large-area processing. In spite of this great potential, challenges remain in being able to deposit high-quality organic materials in a manner that permits scaling to large areas at low manufacturing cost. To fabricate the highest quality organic semiconducting thin films, powders of purified organic stock need to be deposited by evaporative methods, which require large and costly vacuum thin-film deposition systems. Simpler, ink-jet printing methods can also be used, but such solution-based methods come at the cost of compromised materials properties. Our molecular jet (MoJet) printing technology circumvents the above challenges, as it is designed and developed as a method for evaporative deposition, without the need for a vacuum, yet it is functionally equivalent to ink-jet printing. In a cross-disciplinary effort that combines the expertise in MEMS development of the Schmidt group and the molecular thin-film processing experience of the Bulovic group, we developed and demonstrated a novel MEMS-based printhead utilizing a unique

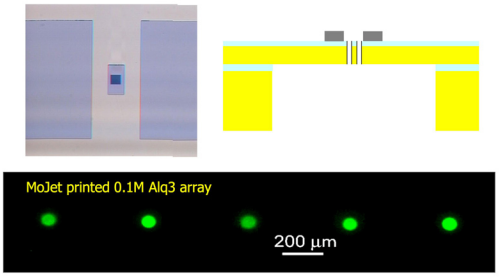


Figure 9: Microphotograph of a molecular jet (MoJet) print head fabricated using MEMS technology. (Upper right) Cross-sectional illustration of the MoJet print head. (Lower) Example of optical organic material printed with the MoJet print head.

microporous microheater design capable of reaching sublimation temperatures in excess of 900ºC. The printhead was utilized to demonstrate high-quality deposition of organic materials in ambient conditions with print resolution as small as 50 μm, validating its utility in the manufacture of large-area integrated organic devices (see figure 9).

New Faculty: Research Directions

Nitride-Based Transistors for Next-Generation Electronics: Tomás Palacios

Amazing properties of nitride semiconductors (large tunable bandgap, piezoelectricity, polarization, biocompatibility) make them the most complete semiconductor family. Because of these properties, nitrides have been widely used in optoelectronics, detectors, MEMS, biosensors, and transistors. However, in spite of their outstanding performance, nitride devices are still far from reaching their theoretical limit.

Professor Palacios's group focuses on the combination of nitrides with new device structures and advanced fabrication technologies. These devices use the unique properties of nitrides to provide unprecedented performance in wireless communications, energy generation, and biosensing. For example, new transistors with a tenfold increase in power performance at sub-millimeter wave frequencies are under development in the group. These and other devices will play a fundamental role in overcoming the tremendous challenges of 21st century electronics (see figure 10).

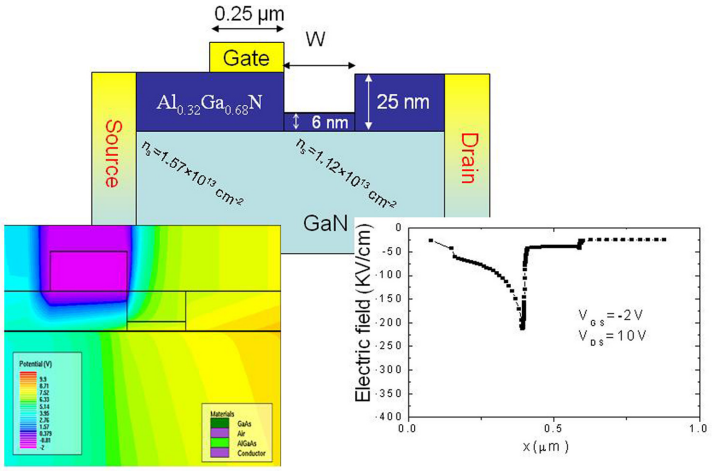


Figure 10: Device structure and electric field simulations of a new transistor design with an expected 50% higher frequency performance.

Awards/Honors for Core MTL Faculty

- Fellow, National Academy of Engineering—Dimitri A. Antoniadis
- Fellow, IEEE—Jesus A. del Alamo
- 2006 Jack Kilby Award for Outstanding Student Paper at ISSCC—Comparator-based switched capacitor circuits for scaled CMOS techniques: Todd Sepke, John K. Fiorenza, Charles G. Sodini, Peter Holloway, Hae-Seung Lee
- Manuel Landsman Career Development Chair—Karl Berggren
- ISSCC 2007 Beatrice Winner Editorial Award—Minimum energy tracking loop with embedded dc-dc converter delivering voltages down to 250 mV in 65-nm CMOS: Yogesh Ramadass, Anantha P. Chandrakasan
- DAC/ISSCC Student Design Contest 2007—Design of an ultra-low-voltage UWB baseband processor: Vivienne Sze, Anantha P. Chandrakasan

Affirmative Action

MTL supports the affirmative action goals of the Institute.

Anantha P. Chandrakasan
Director
Professor of Electrical Engineering and Computer Science

More information about the Microsystems Technology Laboratories can be found at http://mtlweb.mit.edu/.