Microsystems Technology Laboratories

The MIT Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory with a mission to foster research and education in semiconductor process and device technology and in integrated circuits and systems design. MTL provides micro- and nanofabrication and computer-aided design (CAD) infrastructure to the entire campus. MTL has 34 core faculty members who are engaged in diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, microelectromechanical systems (MEMS), and molecular and nanotechnologies. Recent additions to MTL's core membership are professors Sang-Gook Kim (Mechanical Engineering), Li-Shiuan Peh (Electrical Engineering and Computer Science), and Dana Weinstein (Electrical Engineering and Computer Science). In addition, 81 affiliate faculty and senior research staff benefit from the fabrication facilities and CAD infrastructure provided by MTL. Last year, more than 550 researchers, primarily graduate students, conducted research using MTL's advanced infrastructure. During FY2009, MTL recovered approximately 83% of operating expenses through charges to users and underwrites the remaining balance through use of unrestricted funds (approximately $.75 million for FY2008). Sponsored programs administered directly through MTL have an annual research volume of approximately $15 million.

MTL's fabrication environment includes three clean rooms totaling 7,800 square feet: the state-of-the-art class-10 Integrated Circuits Laboratory, the class-100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation for device, circuit, and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL engages users in a number of technical events. MTL hosts a regular seminar series spanning diverse technical areas related to devices and circuits. A committee chaired by professor Joel Dawson arranges the seminar series, open to the public. In addition to these regular seminars, MTL hosts occasional distinguished seminars. Most recently, MTL, in collaboration with the School of Engineering, cohosted the visit of Irwin Jacobs, founder of Qualcomm, in February 2008. MTL holds an annual research conference (MARC) run by MTL graduate students in collaboration with a steering committee chaired by professor Joel Voldman. The conference is widely attended by industry, faculty, students, and staff. MARC is a unique opportunity to learn about research in the diverse areas encompassed by MTL and helps encourage interaction among the MTL community. The 2009 event, though it underwent a last-minute venue change due to inclement winter weather, was as beloved by attendees as it has been in previous years, attracting hundreds of visitors to the Stata Center at MIT. MTL also introduced a new event, the Workshop on Next-Generation Medical Electronics, a two-day event held on campus featuring a panel discussion from leading experts on the topic and a lively poster session. The event will return in 2009 with professor Charles Sodini as event chair.

MTL partners with industry through the Microsystems Industrial Group (MIG). MTL research and operation are significantly subsidized by the MIG consortium. MIG donates major pieces of equipment to MTL, contributes directed fellowships, and

provides access to state-of-the-art integrated circuit chip fabrication service. This year, two new members joined the MIG: Qualcomm and Veeco Instruments. Members of the Industrial Advisory Board (http://www-mtl.mit.edu/mig/iab.html) provide significant guidance in shaping the vision of MTL.

Research conducted at MTL can be broadly classified into eight categories: circuits and systems, electronic devices, energy, materials, medical electronics, MEMS and BioMEMS, nanotechnology, and photonics. MTL has four affiliated industrial research centers with more focused significant guidance in shaping the vision of MTL.

Administration, Management, and Operations

Professor Anantha Chandrakasan is the MTL director with oversight for daily administration and management of the lab. Three faculty associate directors—professor Jesus del Alamo, professor Judy Hoyt, and professor Hae-Seung "Harry" Lee—assist the director in managing the computational and fabrication infrastructure as well as the communications and sponsor relations aspects of the lab, respectively. Two staff associate directors provide direct support for the fabrication facilities (Dr. Vicky Diadiuk) and administrative services, compliance, and industry liaison (Mr. Samuel Crooks).

MTL maintains several committees charged with policy development and implementation, including the policy board (A. Chandrakasan, chair), process technology committee (V. Diadiuk, chair), and computation committee (J. del Alamo, chair). MTL also has a social committee (Debroah Hodges-Pabon, chair) that builds community spirit among our many users and a publications committee (Mara Karapetian, chair) working on MTL's Annual Research Report (http://mtlweb.mit.edu/research/ar.html) and newsletter. MTL community members are also involved in other functional committees.

Shared Service Facilities

MTL's microfabrication, testing, and computational facilities are open to the entire MIT community as well as researchers from other universities and government laboratories through the MTL Outreach Programs. Similarly, the Fabrication Facilities Access Program enables local industrial access to the clean room facilities.

MTL has committed significant resources to the acquisition and maintenance of capital equipment. These capital improvements, upgrades, and purchases allow MTL to serve an increasingly diverse user base. Many of the MIG member companies donate capital equipment that is used in the fabrication and computation facilities.

Fabrication Facilities

MTL's fabrication resources are managed and operated by a group of professional technical staff. All researchers planning to utilize MTL fabrication facilities are required to successfully complete a safety and orientation course before use and must receive training from a research specialist for each piece of laboratory equipment they plan to operate. The facilities support research on projects involving a range of substrates including silicon, germanium, III–V semiconductors, organics, and glass; they include capabilities for deposition of a wide range of materials such as dielectrics, plastics,

semiconductors, metals, and carbon nanotubes. The process technology committee includes students, faculty, and staff and meets weekly to review user process flows in addition to requests for new materials, protocols, and fabrication operational issues.

Computation Facilities

MTL also maintains a comprehensive computation infrastructure, providing a broad array of services to the community. MTL supports the CAD tools required for circuit and system design. Seamlessly connected to the computation infrastructure is MTL's common object representation for advanced laboratories (CORAL), with which the users of MTL's fabrication facilities interface with the fab tools to perform their processes. The user log is coupled to a sophisticated charging algorithm that calculates user fees on a monthly basis. CORAL was developed in collaboration with Stanford University and continues to develop as the needs of MIT's microfabrication community require.

Research Highlights

Micro-Gas Analyzers: A.I. Akinwande

The micro-gas analyzer project in MTL includes researchers from academia and industry (Cambridge University, UK; University of Texas at Dallas; Clean Earth Technology; and Raytheon). The project is developing technologies for real-time, tiny (2 cm^3), low-power (1 W), and high-resolution (0.5 Da) mass spectrometers that operate at high pressures (100 mTorr) with low detection limits (1 ppt) and short total analysis times (4 s). The overall goal is to scale conventional devices to smaller dimensions through MEMS technology and using massively parallel arrays of scaled devices to improve sensitivity. The sheer portability of these sensors would introduce a host of new applications and deployment scenarios such as wearable chemical and biological sensors or remote unattended gas sensors with wireless interrogation capabilities. The key advantages of this miniaturization are the portability it enables and the reduction in pump power needed due to the relaxation on operational pressure.

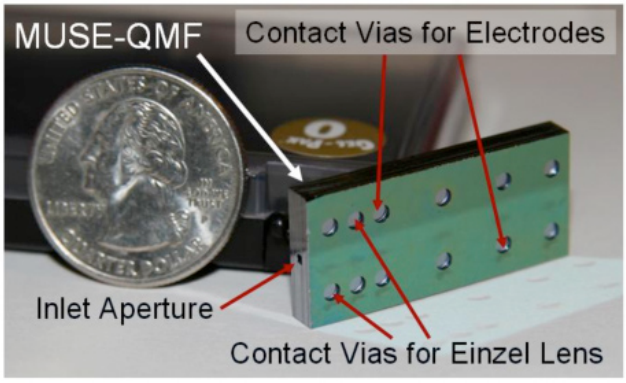

Figure 1. Fabricated micro-square electrode quadrupole mass filter (MuSE-QMF) next to a US quarter.

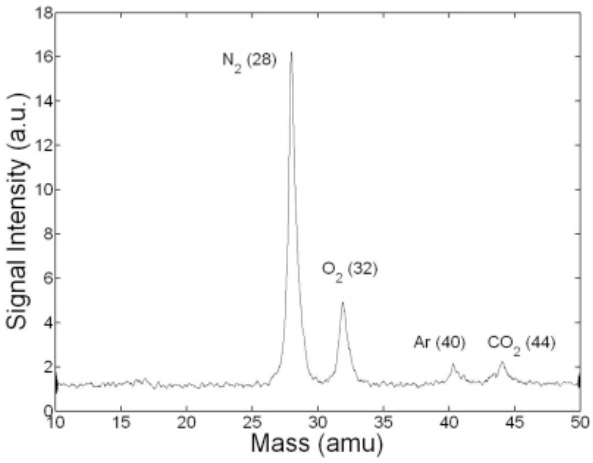

Figure 2. Mass spectrum for air using the MuSE-QMF driven in the second stability region at 2 MHz.

In the last year, we have demonstrated all the key microfabricated components of the micro-gas analyzer: (a) ionization source for chemical and biological species in the gas

stream based on gated arrays of field emission devices and field ionization devices, (b) a microfabricated mass filter based on arrays of linear quadrupoles, (c) a microfabricated mass detector that has an embedded resonant microstructure, (d) a microfabricated vibrating reed electrometer for charge detection, and (e) a microfabricated vacuum pump. Figure 1 shows one of the key microfabricated components, the micro-square electrode quadrupole mass filter (MuSE-QMF) whose fabrication process consists of thermal oxidation, the use of deep reactive ion etching to define the features, and the fusion bonding of five patterned silicon wafers. Figure 2 is a typical mass spectrum obtained from one of the devices. The main peaks for air (nitrogen, oxygen, argon, carbon dioxide) can be clearly distinguished in Figure 2. The MuSE-QMF demonstrated a mass range of 650 amu using the first stability region and a minimum peak width of 0.3 amu in the second stability region.

A New Semiempirical Short-Channel MOSFET Current-Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters: A. Khakifirooz, O. Nayfeh, and D.A. Antoniadis

A simple semiempirical model for the drain current $I_D(V_{GS},V_{DS})$ of short-channel MOSFETs applicable in all regions of device operation has been developed. The model is based on the so-called "top-of-the-barrier transport" model, and we refer to it as the "MIT virtual source," MVS for short, model. In contrast to current models in use that require a very large number of parameters, the new model achieves very accurate results by using a very small number of physical parameters. Of these parameters, five are directly obtainable from standard device measurements: Gate capacitance in strong inversion conditions—typically at maximum voltage $V_{GS} = V_{DD}$, subthreshold swing, drain-induced barrier lowering coefficient, current in weak inversion—typically I_{off} at $V_{GS} = 0$ V—and high V_{DS} and the total resistance at $V_{DS} = 0$ V and $V_{GS} = V_{DD}$. The four fitted physical parameters are carrier low-field mobility, parasitic source–drain resistance, the saturation region carrier velocity at the so-called virtual source, and effective channel length. The modeled current versus voltage characteristics and their derivatives are continuous from weak to strong inversion and from the linear to saturation regimes of operation. Remarkable agreement with published state-of-the-art planar short-channel strained devices is demonstrated with physically meaningful values of the fitted physical parameters. Moreover, the model allows for good physical insight in device performance properties, such as extraction of the virtual source velocity, a parameter of critical technological importance for allowing for continued MOSFET performance scaling. The simplicity of the model and the fact that it uses only physically meaningful parameters provides an easy way for technology benchmarking and performance projection. The model has already been implemented in an experimental version of the standard circuit simulator "SPICE" in collaboration with professor J. Roychowdhury of the University of California, Berkeley. It has also been used in collaboration with Professor Chandrakasan's group in a new statistical analysis method for SRAM circuit cells, achieving significant speed-up over standard BSIM model-based SPICE. Other applications of the model include physical characterization of state-of-the-art III–V FETs fabricated at MIT by professor J. del Alamo's group and implementation as an industry standard tool for evaluation of MOSFET technology in the International Technology Roadmap for Semiconductors.

A Pulsed UWB Receiver SoC for Insect Motion Control: D.C. Daly, P.P. Mercier, M. Bhardwaj, J. Voldman, and A.P. Chandrakasan

Scientists and engineers have been fascinated for decades by cybernetic organisms (or cyborgs), fusing artificial and natural systems. Cyborgs enable harnessing biological systems that have been honed by evolutionary forces over millennia. An emerging cyborg application is hybrid-insect flight control, where electronics and MEMS devices are placed on and within insects to alter flight direction. Through our research, a cyborg insect system was developed consisting of a highly integrated ultra-wideband (UWB) receiver system-on-chip (SoC) mounted on a miniature printed circuit board (PCB) and attached to a moth with a harness [D.C. Daly, P.P. Mercier, M. Bhardwaj, A.L. Stone, J. Voldman, R.B. Levine, J.G. Hildebrand, and A.P. Chandrakasan, "A pulsed UWB receiver SoC for insect motion control." In *IEEE ISSCC Digest of Technical Papers*, February 2009, pages 200–201.]. Several circuit and architectural optimizations were made to reduce average power consumption to the order of milliwatts. Three-dimensional die stacking and a flexible PCB resulted in an overall system weight of only 1 g. Preliminary flight control of a moth was demonstrated, with a battery-powered receiver successfully receiving a packet and stimulating the moth, thereby changing its direction of flight.

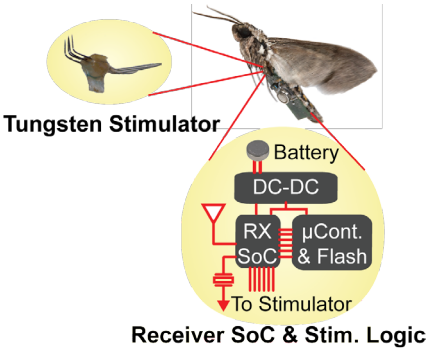

Figure 3. Hybrid-insect flight control system.

A New Architecture for Radio Transmitters: J.L. Dawson

Professor Dawson's group currently focuses on two areas: new architectures for wireless transceivers and improved electronics for biomedical electronics. One of our most exciting new transceiver architectures is illustrated in Figure 4. We call it an asymmetric multilevel outphasing transmitter, and its most important attribute is that it allows a wireless transmitter to be highly efficient and highly linear at the same time. This accomplishment is considered a "holy grail" in transmitter designs, and failure to reach this goal is the reason, for example, that a cellular phone cannot stream live video without running down the battery in a matter of minutes. We presented simulation results with this architecture at this year's RFIC Symposium, and we are currently testing a prototype integrated circuit.

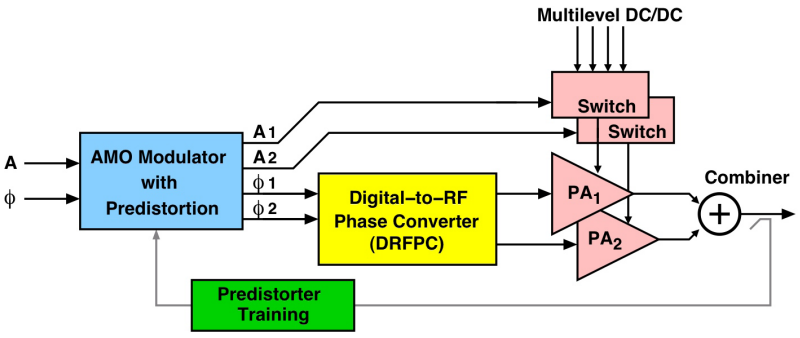

Figure 4. Illustration of the architecture of the asymmetric multilevel outphasing transmitter.

World Record InGaAs Heterostructure Field-Effect Transistor: D.-H. Kim and J.A. del Alamo

Professor del Alamo's group is investigating a new generation of transistors that are capable of extending the microelectronics roadmap for several more generations. This research group is attempting to do this by taking advantage of the extraordinary electron transport properties of InGaAs, InAs, and other compound semiconductors.

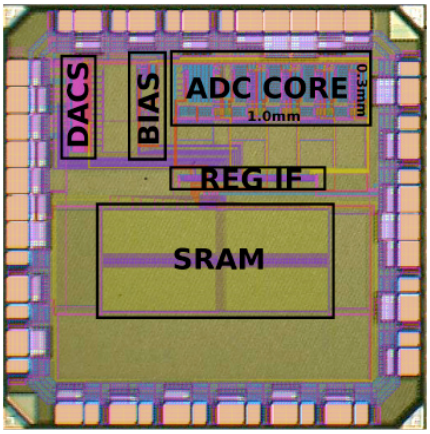

Figure 5. 30-nm InAs transistor with world record frequency performance.

In the last year, Dr. Dae-Hyun Kim, a postdoctoral associate in Professor del Alamo's group has achieved 30 nm gate length InAs high electron mobility transistors (HEMT) that display a world-record frequency response. For the first time, a transistor has been fabricated that exhibits a current-gain cut-off frequency and a power-gain cut-off frequency that are both more than 600 GHz. Both are measured at the same bias point. These two figures of merit are widely used in the community to evaluate the suitability of transistors for high-frequency and high-speed operation. The values reported by the del Alamo group are the highest combination ever on any transistor type on any material system. This bodes well for the suitability of transistors on this material system for ultra-high-speed logic and teraherz applications.

Kim, D.-H., and J.A. del Alamo. 2008. 30 nm E-mode InAs PHEMTs for THz and Future Logic Applications. International Electron Devices Meeting, San Francisco, December 2008, page 719.

Breaking the Analog Circuit Bottleneck: Hae-Seung Lee

Since development of the revolutionary ultra-low-power analog circuits in 2006, Professor Lee's group has focused its research on the advancement of comparator and zero-crossing-based circuits. These circuits have a theoretical potential for a reduction in power consumption of an order of magnitude or more and offer superior compatibility with deep submicron technologies. The latest results were reported at the prestigious International Solid-State Circuits Conference in San Francisco in

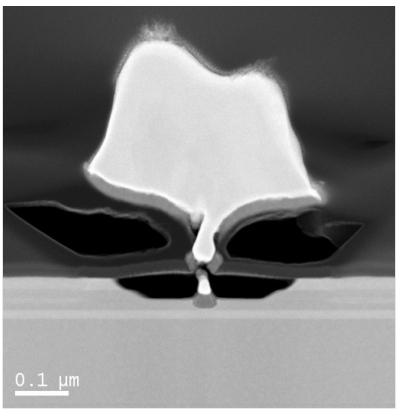

Figure 6. Microphotograph of the zero-crossing-based analog-to-digital converter. Performance: 12 bit, 50 MS/s, 5 mW.

February 2009. The 12-bit, 50 MS/s analog-to-digital converter built in a standard 90-nm CMOS technology consumes an unprecedented 5 mW of power. This performance corresponds to power more than a factor of 4 lower than the best published result. The measured thermal noise floor suggests that an additional factor of 4 reduction in power consumption would be readily achieved with design optimization.

Brooks, L., and H.-S. Lee. 2009. A 12b 50MS/s Fully Differential Zero-Crossing-Based ADC Without CMFB. In ISSCC Digest of Technical Papers*, San Francisco, CA, February 2009, pages 166–167.*

Graphene Ambipolar Electronics: A. Hsu, H. Wang, J. Wu, D. Nezich, J. Kong, and T. Palacios. Sponsorship: MIT/Army Institute for Soldier Nanotechnologies and the Office of Naval Research

Graphene, a one-atom-thick layer of carbon atoms, has recently been identified as an outstanding material for future electronics. Our group is using some of the unique properties of this new material to demonstrate new electronics devices. One of the most intriguing of these properties is the ambipolar transport of graphene, its ability to conduct current with both electrons and holes in the same device. On the basis of this property, we have recently demonstrated several new graphene devices, including frequency multipliers, mixers, and zero-volt detectors. Figure 7 shows an optical micrograph of a graphene frequency multiplier. Because of the strong nonlinearity introduced by the ambipolar transport, an input sinusoidal signal doubles its frequency when it passes through the graphene device. Numerous applications are being considered for this device, including high-frequency signal generation, teraherz imaging, and high-speed communications. This work on advanced graphene devices has been featured in *Nature*, *Physics World*, and more 500 other journals and websites worldwide in the last year.

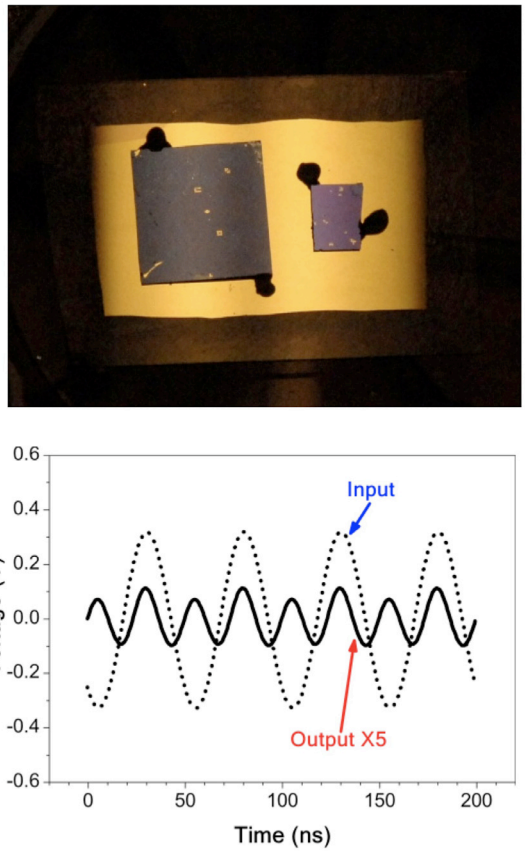

Figure 7. Picture of one of our graphene frequency multipliers. The figure also shows the response of the device to sinusoidal signals. The frequency of the output signal is double that at the input. (Photo: Donna Coveney.)

Professor Carl V. Thompson's Group

In the past year, Professor Thompson's group has achieved several significant milestones in development of processing techniques for producing arrays of one-dimensional nanostructures and nanomaterials for use in microsystems such as next-generation electronic circuits. Through catalyst engineering studies, Professor Thompson's group has discovered new ways to produce arrays of carbon nanotubes (CNTs) with controlled numbers of tubes per area and with controlled diameters and chirality (which strongly affects electronic conductivity). In addition, through collaborations with Intel Corporation, Professor Thompson's group has developed new processes for low-temperature growth of CNTs on metallic underlayers in ways that are compatible with processing Si-based integrated circuits.

In other work on one-dimensional nanostructure arrays, Professor Thompson's group developed techniques for producing aligned single-crystal silicon nanowires in arrays with separately controlled wire diameters, spacing, and length and with controlled ordering symmetry. This was achieved at room temperature on silicon substrates with a combination of metal-catalyzed etching and interference or block-copolymer lithography. Current research focuses on using these structures in on-chip power management and energy storage devices. Applications in sensing and biotechnology are also under investigation.

Through collaborations in the Singapore–MIT Alliance, Professor Thompson's group developed a technique in which microfabricated arrays of cantilevers and a special deposition technique enable combinatorial studies of the properties of binary and ternary alloy systems in single deposition and characterization processes. As an application of this technique, they studied metal alloy systems that readily form metallic glasses and demonstrated a strong correlation between the volume change on crystallization and the ease of glass formation. New compositions that readily form glasses were also discovered. This work was published in *Science*.

Awards/Honors for Core MTL Faculty

MacVicar Fellowship, March 2009—Vladimir Bulovic

Semiconductor Industry Association University Researcher Award, 2009—Anantha Chandrakasan

Presidential Early Career Award for Scientists and Engineers, July 2009—Joel Dawson

Jonathan Allen Junior Faculty Award at the Research Laboratory of Electronics, August 2008; CAREER Award, November 2008, National Science Foundation; Jerome H. Saltzer Teaching Award, May 2009—Jing Kong

Office of Naval Research Young Investigator Award, March 2009; CAREER Award, July 2009, National Science Foundation; Best Paper Award at the International Conference on Advances in Electronics and Microelectronics, 2008, for the paper "New Technologies for Improving the High Frequency

Performance of AlGaN/GaN High Electron Mobility Transistors" by Jinwook W. Chung and Tomas Palacios—Tomas Palacios

IEEE/ACM William J. McCalla ICCAD Best Paper Award, IEEE/ACM International Conference on Computer Aided Design, San Jose, CA, November 2008; 2008 IEEE Transactions on Advanced Packaging Best Paper Award, May 2009—Vladimir Stojanovic

Analytical Chemistry Young Innovator Award, November 2008; Louis Smullin Departmental Teaching Award—Joel Voldman

Affirmative Action

MTL supports the affirmative action goals of the Institute.

Anantha P. Chandrakasan
Director
Professor of Electrical Engineering and Computer Science

More information about the Microsystems Technology Laboratories can be found at http://mtlweb.mit.edu/.