Microsystems Technology Laboratories

The Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory with a mission to foster research and education in semiconductor process and device technology, and in integrated circuits and systems design. MTL provides micro- and nanofabrication and computer-aided design (CAD) infrastructure to the entire campus. MTL has 43 core faculty members who are engaged in diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, microelectromechanical systems (MEMS), and molecular and nanotechnologies. The most recent additions to MTL's core membership include Polina Anikeeva, Department of Materials Science and Engineering (DMSE); Nicholas Fang, Department of Mechanical Engineering (DME); Silvija Gradečak, DMSE; Pablo Jarillo-Herrero, Department of Physics; William Tisdale, Department of Chemical Engineering; Kripa Varanasi, DME; Evelyn Wang, DME; and Michael Watts, Department of Electrical Engineering and Computer Science (EECS). In addition, 88 affiliate faculty and senior research staff benefit from the fabrication facilities and CAD infrastructure provided by MTL. Last year, more than 955 researchers, primarily graduate students from 35 departments, laboratories, and centers, conducted research using MTL's advanced infrastructure (Figure 1). During FY2011, MTL recovered approximately 70% of operating expenses through charges to users and underwrote the remaining balance through unrestricted funds (approximately $1.45 million). Sponsored programs administered directly through MTL have an annual research volume of approximately $15.5 million.

MTL's fabrication environment includes three clean rooms, totaling 7,800 square feet: the 6-inch capable class-10 Integrated Circuits Laboratory, the class-100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation for device, circuit, and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL engages users in a number of technical events. MTL hosts a regular seminar series spanning diverse technical areas related to devices and circuits. A committee chaired by professor Tomás Palacios organizes the seminar series, open to the public. In addition to these regular seminars, MTL hosts occasional distinguished seminars. Most recently, it hosted the visit of Tunç Doluca, president and chief executive officer at Maxim Integrated Products. MTL holds an annual research conference (MARC) run by MTL graduate students, in collaboration with a steering committee chaired by professor Jing Kong and co-chaired by students Joy Johnson (professor Duane Boning group) and Geoffrey Supran (professor Vladimir Bulović group). The conference is widely attended by industry, faculty, students, and staff. MARC is a unique opportunity to learn about research in the diverse areas encompassed by MTL and helps encourage interaction among the MTL community. The 2012 event was held at the Waterville Valley Resort, in New Hampshire and attracted 212 attendees. MTL also held the third workshop on next-generation medical electronics, a two-day event held on campus that featured talks from leading experts on the topic, as well as a lively poster session.

MTL partners with industry through the Microsystems Industrial Group (MIG). The MIG consortium subsidizes MTL research and operations significantly, donating major pieces of equipment to MTL, contributing directed fellowships, and providing access to state-of-the-art integrated circuit chip fabrication services. Members of the MIG Industrial Advisory Board provide significant guidance in shaping the vision of MTL.

Research conducted at MTL can be broadly classified into the following categories: circuits and systems, electronic devices, energy, materials, medical electronics, MEMS and BioMEMS, nanotechnology, and photonics. MTL has five affiliated research centers, with focused themes: the Center for Integrated Circuits and Systems, the Center for Graphene Devices, MEMS@MIT, the Medical Electronic Device Realization Center, and the MIT Center for Excitonics.

Administration, Management, and Operations

Professor Bulović is director of MTL with oversight for daily administration and management of the laboratory. Four faculty associate directors—professors Jesús del Alamo, Judy Hoyt, Karl Berggren, and David Perreault (until May 2012; replaced by professor Jeffrey Lang, June 2012)—assist the director in managing the computational and fabrication infrastructure as well as the communications and sponsor relations aspects of the laboratory. Two staff associate directors provide direct support for the fabrication facilities (Vicky Diadiuk), and administrative services, compliance, legal matters, license agreements, and industry liaisons (Samuel Crooks).

MTL maintains several committees charged with policy development and implementation, including the policy board (Professor Bulović, chair), process technology committee (Vicky Diadiuk, chair), and computation committee (Professor del Alamo, chair). MTL also has a social committee (Debroah Hodges-Pabon, chair), which builds community spirit among its many users, and a communications committee (Mara Karapetian, chair), which works on MTL's Annual Research Report and newsletter, among other publications. MTL community members are also involved in other functional committees.

Shared Service Facilities

MTL's microfabrication, testing, and computational facilities are open to the entire MIT community, as well as to researchers from other universities and government laboratories, through the MTL Outreach Programs. Similarly, the Fabrication Facilities Access Program enables local industrial access to the clean room facilities.

MTL has committed significant resources to the acquisition and maintenance of capital equipment. These capital improvements, upgrades, and purchases allow MTL to serve an increasingly diverse user base. Many of the MIG member companies donate capital equipment that is used in the fabrication and computation facilities.

Fabrication Facilities

MTL's fabrication resources are managed and operated by a group of professional technical staff. All researchers planning to utilize MTL fabrication facilities are first required to successfully complete a safety and orientation course, and must receive training from a research specialist for each piece of laboratory equipment they plan to operate. The facilities support research on projects involving a range of substrates, including silicon, germanium, III–V semiconductors, organics, and glass; they include capabilities for deposition of a wide range of materials, such as dielectrics, plastics, semiconductors, metals, carbon nanotubes, and graphene. The process technology committee includes students, faculty, and staff and meets weekly to review user process flows, in addition to requests for new materials, protocols, and fabrication operational issues.

In AY2012, MTL opened the Electron Beam Lithography (EBL) facility in a purpose-built, temperature-controlled room in 24-041. The EBL houses the recently installed ELS-F125 Electron Beam Lithography tool, made by Elionix. The EBL facility is jointly run by the Research Laboratory of Electronics and MTL, and provides students and researchers from across MIT and neighboring institutions with access to patterning at the smallest sizes available anywhere (capable of patterning features smaller than five nanometers). Electrons are accelerated to an energy of 125 kilovolts and then swept across resist-coated substrates, such as silicon wafers, to form arbitrary patterns that can later be transferred into underlying or deposited materials. Large areas can be patterned across substrates ranging from 5-mm-square chips to 200-mm-diameter wafers. The tool has been operational since early April 2012.

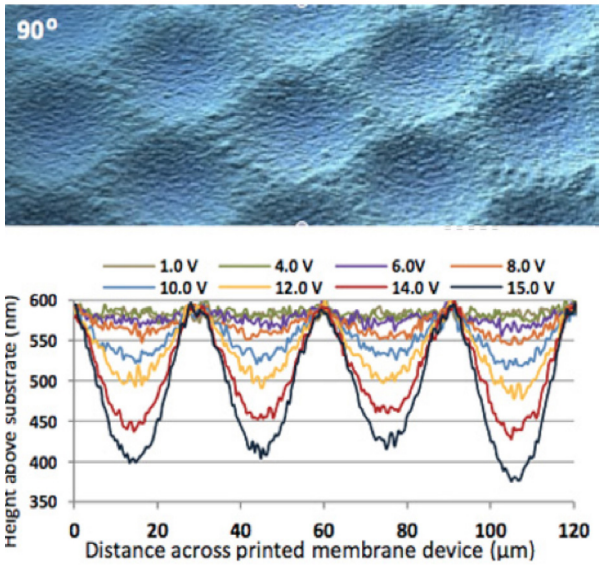
Computation Facilities

MTL also maintains a comprehensive systems and software infrastructure that provides a broad array of services to the community. The laboratory supports a large community of research workstations and servers, as well as a number of servers that are used to offer various services to the MTL community. In addition, MTL offers a wide variety of commercial CAD tools used for circuit and system design research to the general MIT community. Also, MTL has developed a suite of software tools to help manage three core pieces of the laboratory's operations—user management (MUMMS), equipment usage/management (CORAL), and billing (Cost Recovery). While CORAL was developed in collaboration with Stanford University, MUMMS and Cost Recovery were developed at MTL, and all three tools have also been deployed at MIT's Center for Materials Science and Engineering.

Research Highlights

Printed Microelectomechanical Systems Membranes on Silicon

At the Institute of Electrical and Electronics Engineers (IEEE) 25th International Conference on Micro Electro Mechanical Systems (January 2012), Professors Bulović and Lang reported a new, simple method for additive fabrication of thin (125 nm thick) gold membranes on patterned silicon dioxide (SiO2) substrates for acoustic MEMS. The deflection of these membranes, suspended over cavities in a SiO2 dielectric layer atop a conducting electrode, can be used to produce sound or monitor pressure. This new process avoids fabrication of MEMS diaphragms via wet or deep reactive-ion etching, which in turn removes the need for etch-stops and wafer bonding. Membranes of 1 mm2 in area have been fabricated and their deflection was measured using optical interferometry. The membranes have a maximum deflection of about 150 nm across 28 μm diameter cavities. Young's modulus of these films is shown to be 70 GPa, and their potential sound pressure generation at 15 V is calculated to exceed 50 dB, if used as an earphone.

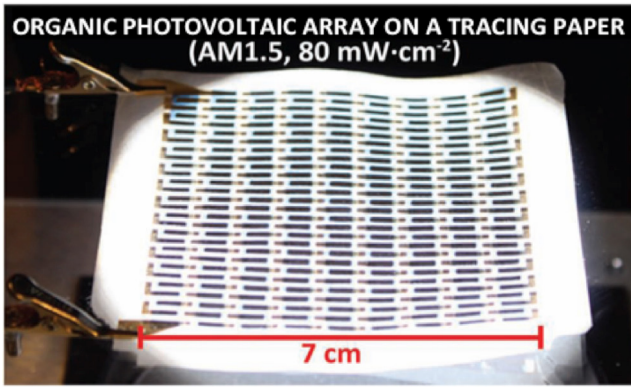


Pressure sensor array fabricated on a silicon dioxide substrate using contact-transfer, under 15 volts actuation, imaged using optical interferometry. The gold membrane above most of the sensor cavities is showing about 150 nm of deflection in the center of each cavity.

Solar Cells on Paper

In Advance Materials 23 (2011), Professors Bulović and Gleason demonstrated a substrate-independent vapor printing process of conductive polymer films that enabled them to fabricate organic solar cells on glass, plastic, and paper substrates. Their demonstrations illustrate the near-term potential for implementation of paper-thin photovoltaics in new venues and on nontraditional media. The paper photovoltaic arrays produce > 50 V, power common electronic displays in ambient indoor lighting, and can be tortuously flexed and folded without loss of function. The polymer vapor printing process employs no solvents or rare elements (e.g., indium) and the substrate remains at low temperature. The vapor-printed electrodes conform to the geometry of rough substrates, eliminating the need for more costly and heavier substrates such as

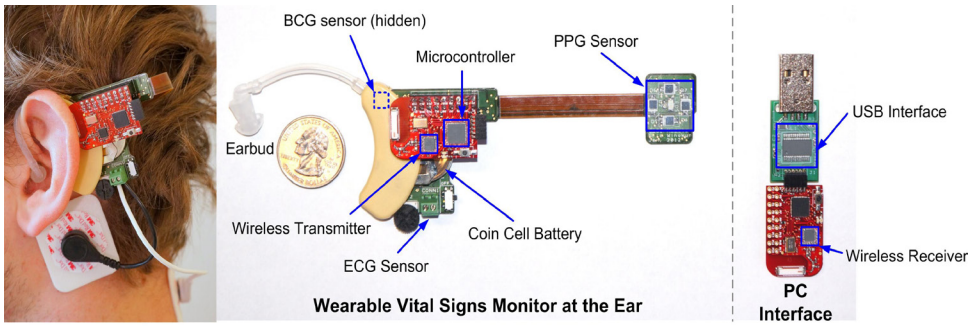
ultra-smooth plastics. Additionally, a thin-film vapor-deposited encapsulation layer extends lifetime, even allowing for operation while submerged in water, but produces no substantial change in weight, feel, or appearance of the paper circuits. This all-dry fabrication and integration strategy should enable the design and implementation of new, low-cost photovoltaic and optoelectronic systems without substrate limitations.



Large-area monolithic photovoltaic array, consisting of 250 organic photovoltaic cells printed on tracing paper.

A Wearable Vital Signs Monitor at the Ear

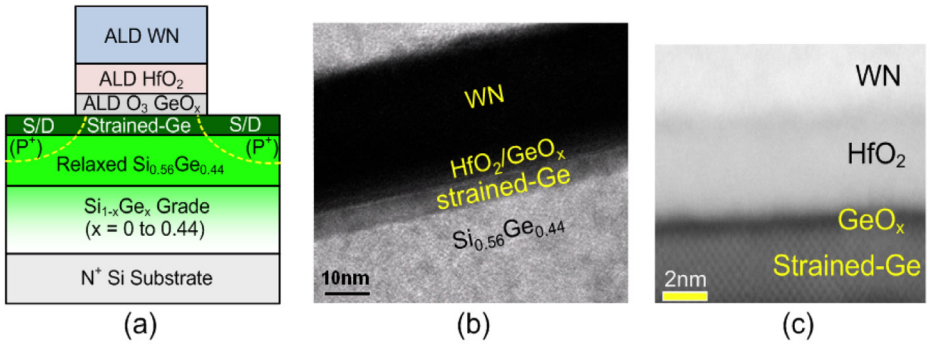
Vital signs monitors aid the early detection of cardiovascular diseases by providing the long-term data necessary for an accurate and timely diagnosis. The site behind the ear is used as a location for a non-invasive and wearable vital signs monitor that continuously measures heart rate, pre-ejection period, blood oxygenation, and blood pressure. The device uses the ear as a discreet and natural anchor that reduces device visibility and the need for skin adhesives. This location offers physiological signals including the electrocardiogram (ECG), the ballistocardiogram (BCG), and the photoplethysmogram (PPG). The ECG measures the heart's electrical activities and offers continuous heart rate. The BCG measures the head's mechanical reaction to the blood expelled by the heart and offers the heart's pre-ejection period when used with ECG. The PPG measures the blood's optical qualities and offers blood oxygenation and cuff-less blood pressure when used with BCG. Human clinical tests are currently underway to validate the device.



The wearable vital signs monitor is shown being worn at the ear, with its components labeled.

Ultra-thin Strained-germanium Channel Metal Oxide Semiconductor Field-effect Transistors with Sub 1-nm Equivalent-oxide-thickness Gate Dielectric

Strained germanium (Ge) has the highest hole mobility of any semiconductor, and is compatible with Silicon (Si) integrated circuit manufacturing technology. Thus, p-metal-oxide-semiconductor field-effect transistors (MOSFETs) utilizing strained Ge layers as an alternate to Si are under investigation. The Ge must be thin (<10 nm) to maintain large strain. Professor Hoyt's group is studying the process technology and physics of hole transport in these nanoscale layers. A key requirement is to develop a high-quality insulator with sub 1-nm equivalent-oxide-thickness (EOT) that is compatible with strained Ge. In a paper published by the group in IEEE Electron Device Letters, transistors were demonstrated with the thinnest EOT published to date (~1 nm) on strained Ge, and hole mobility that is five times higher than that measured on similarly fabricated Si control devices. The gate insulator was formed by atomic layer deposition. These results indicate that strained-Ge p-MOSFETs are promising candidates for future high-performance, low power-supply-voltage integrated circuits.

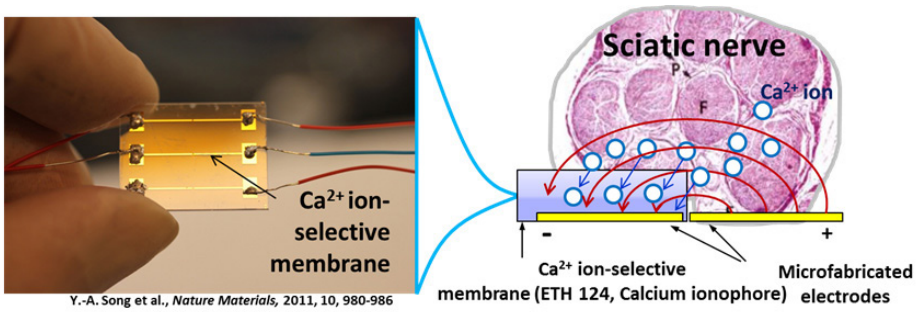


(a) Device schematic and corresponding cross-sectional, (b) Transmission Electron Microscopy (TEM), and (c) Scanning TEM images of the fabricated ultra-thin strained-Ge channel p-MOSFETs with GeOx/HfO2 gate insulator.

Electrochemical Activation and Inhibition of Neuromuscular Systems through Modulation of Ion Concentrations with Ion-selective Membranes

Conventional functional electrical stimulation aims to restore functional motor activity of patients with disabilities resulting from spinal cord injury or neurological disorders. However, intervention with functional electrical stimulation in neurological diseases lacks an effective implantable method that suppresses unwanted nerve signals. The group has developed an electrochemical method to activate and inhibit a nerve by electrically modulating ion concentrations in situ along the nerve. Using ion-selective membranes to achieve different excitability states of the nerve, either a reduction of the electrical threshold for stimulation by up to approximately 40%, or voluntary, reversible inhibition of nerve signal propagation is observed. This low-threshold

electrochemical stimulation method is applicable in current implantable neuroprosthetic devices, whereas the on-demand nerve-blocking mechanism could offer effective clinical intervention in disease states caused by uncontrolled nerve activation, such as epilepsy and chronic pain syndromes.

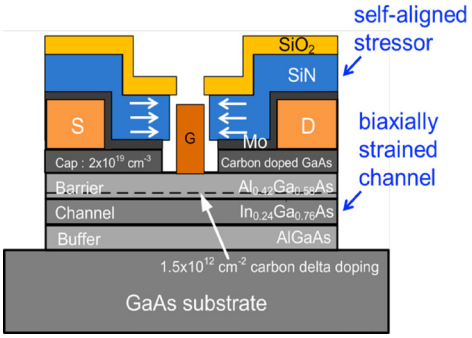


Experimental set-up for stimulation of frog sciatic nerve with a Ca2+ ISM device.

InGaAs Quantum-well Field-effect Transistors that Incorporate Process-induced Uniaxial Strain and Epitaxially-grown Biaxial Strain

Recently, InGaAs-channel n-type field-effect transistors (FETs) have attracted a great deal of interest for future sub-10 nm complementary metal-oxide-semiconductor (CMOS) applications. Promising device results have been demonstrated. In the quest for an all InGaAs–based complementary logic technology, realizing a high-performance p-channel InGaAs FET remains a challenge. The key problem is the relatively small hole mobility (μh) of InGaAs, which is of the same order as in Si.

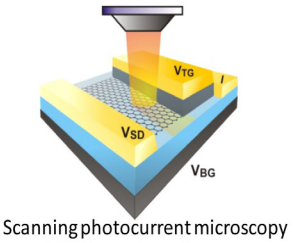
A well-established way to improve hole mobility is through the application of uniaxial strain to the channel material. Recent studies carried out in Professor del Alamo's group suggest that by combining uniaxial strain and biaxial strain, the effective mass (m*) and μh in InGaAs quantum wells can be significantly enhanced. To explore the device potential of this new concept, the group has fabricated InGaAs FETs through a process that incorporates uniaxial strain introduced through a self-aligned stressor on a heterostructure with the channel under biaxial strain. Results demonstrate substantial enhancements in transport characteristics. A 36% increase in the intrinsic transconductance of devices with a gate length of 2 μm was observed. The structure exhibits promising gate-length scalability and is compatible with self-aligned source drain metal contacts. The group's proposed device architecture holds promise to implement high-performance p-channel III-V FETs in a variety of material systems for future CMOS applications.



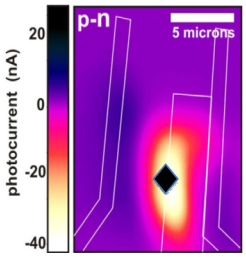
Fabricated P-channel InGaAs quantum-well FET with built-in stressor and biaxially strained channel. A refractory contact metal layer and SiN stressor are both self-aligned to the gate edge.

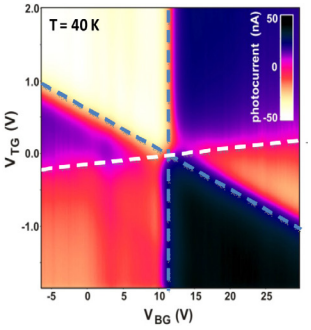
Graphene Hot Carrier Optoelectronics

Graphene, an atomically thin conducting membrane, is considered an excellent optoelectronic material candidate for photodetection and energy-harvesting applications due to its broadband optical response and high internal quantum efficiency. However, previous to this work, measurements had not clearly determined the intrinsic photocurrent generation mechanism. As recently reported in *Science*, this work explored the intrinsic photoresponse of monolayer and bilayer graphene photo-detector devices and determined the intrinsic response. In addition to demonstrating a novel photodetector device, it was found that photon absorption leads to a population of high-temperature "hot" electrons and holes that result in a highly efficient photothermoelectric effect. This process, which is unlike conventional photovoltaic processes observed in traditional photo-detectors, may lead to ultra-efficient solar cells, since the photo-generated charge carrier population remains hot while the lattice stays cool.



Scanning photocurrent microscopy of dual-gated graphene p-n junction photodetectors





Six regions of photocurrent vs. V_{BG} and V_{TG} result from photo-thermoelectric origins of photoresponse

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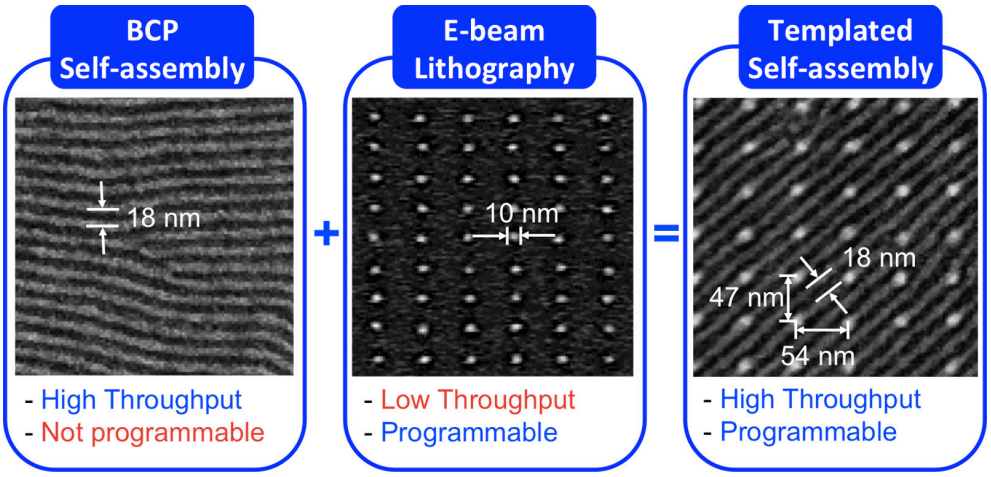
(top left): Schematics of dual-gated graphene photodetector device. (top right): Photocurrent as a function of top and bottom gate voltages exhibits 6-fold alternating sign regions. (bottom left): spatial map of photocurrent distribution in the pn junction regime.

Aligned Sub-10-nm Block Copolymer Patterns Templated by Post Arrays

Within the next ten years, the semiconductor industry requires a process enabling fabrication of sub-10-nm complex patterns over a large area. Electron-beam lithography has been used for fabricating sub-10-nm patterns but its throughput is not high enough for industrial applications. Here, the process of fabricating aligned sub-10-nm patterns with high throughput based on templated self-assembly of block copolymers is demonstrated. On an unpatterned substrate, 16kg/mol polystyrene-b-polydimethylsiloxane (PS-b-PDMS) resulted in 18-nm-pith PDMS cylinders without long-range order (Figure 9, left). To control the orientation of the PDMS cylinders, a block copolymer film was annealed on the substrate with a rectangular lattice of posts As a result, the PDMS cylinders were aligned along the angle that makes the pitch of the PDMS cylinders close to its natural pitch (Figure 9, right). Because the posts occupied only 3% of the final pattern, the throughput of EBL was increased by a factor of ~30.



(left): Scanning electron microscope (SEM) image of PDMS cylinders on an unpatterned substrate. (center): SEM image of a rectangular lattice of posts with a diameter of 10 nm and a height of 19 nm—the posts were fabricated by electron-beam lithography. (right): SEM image of PDMS cylinders templated by post arrays.

Seamless Integration of GaN and Si Complementary Metal-Oxide-Semiconductor for Future Electronics

Until now, chip designers had to compromise regarding what semiconductor material to use in electronic circuits. Silicon offers unprecedented scalability and circuit complexity, while transistors made of compound semiconductors (III-V) have much better performance in terms of high frequency or power delivery. The group has been working for the last five years in the development of a new technology that enables the seamless integration of Si CMOS electronics with state-of-the-art GaN III-V devices in the same chip. The group has demonstrated the first full-wafer integration of these devices. This integration enables a wide variety of opportunities for advanced circuit designs that could bring analog-to-digital converters, power modules, and radio frequency (RF) transmitters to new levels of efficiency, performance, and speed in the near future. Circuit designers are no longer constrained by material properties but now can choose the best material for each function.

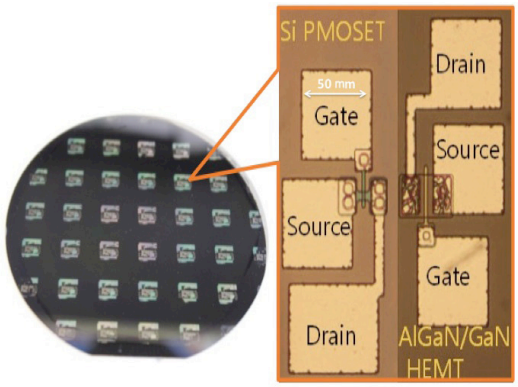
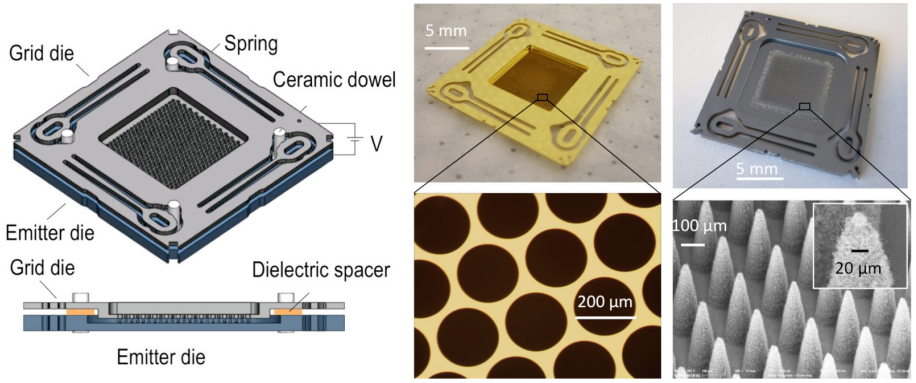


Image of the first wafer-scale integration of GaN and Si devices. The hybrid GaN/Si wafer has a diameter of four inches (photo credit: Hyung-Seok Lee).

Multiplexed Electrospray Sources with Micro-nano Hierarchical Structures for Healthcare, Manufacturing, and Space Applications

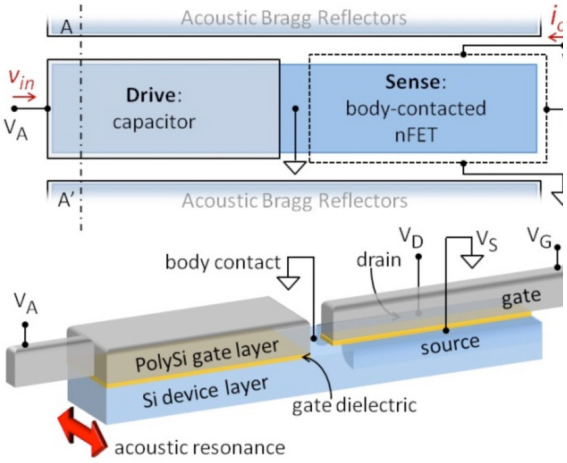
Using micro- and nanotechnology, the group is developing massively multiplexed electrospray sources capable of high-throughput generation of nanostructured elements with low morphological spread (droplets, ions, fibers); these devices could make economically feasible and innovative applications in healthcare (nanofiber tissue scaffolding), manufacturing (nanostructured composites, printable MEMS), and space exploration (highly throttleable mass/power-efficient nanosatellite thrusters). The group pioneered the field of multiplexed MEMS electrospray and some of its ideas—such as decoupling the emitter and electrode process flows to achieve high-yield fabrication and high-electrical insulation, and implementing individual emitter flow control to achieve uniform and steady emission—have been adopted by other leading research groups. The group is currently exploring hierarchical structures that seamlessly integrate micro- and nano-sized features to optimize the performance of the electrospray array. Figure 11 illustrates one of the latest MEMS multiplexed electrospray sources with hierarchical micro-nano integration: the group used silicon-based batch-microfabrication techniques to manufacture monolithic arrays of electrospray emitters with as many as 2,000 emitters in 1 cm2 that turn on at low voltage, and used batch nanofabrication techniques to create a conformal porous carbon nanotube layer on top of the emitters to visibly increase the flowrate per emitter.



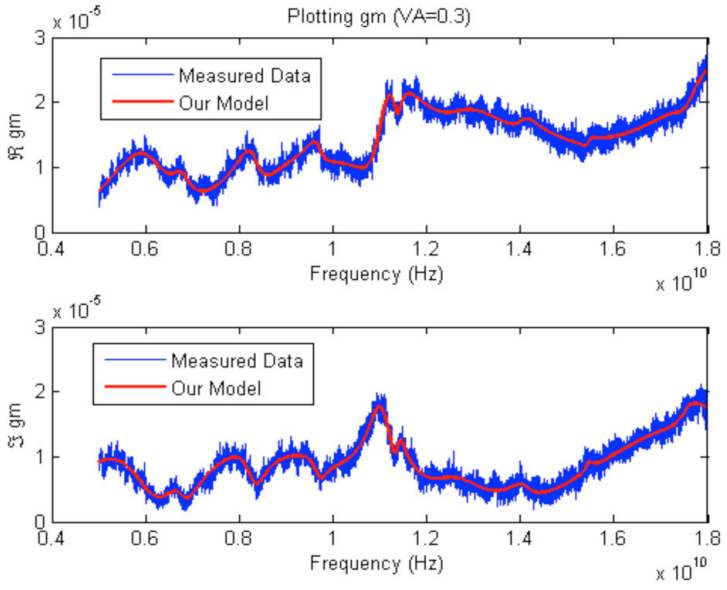
(left): Schematic of a massively multiplexed MEMS electrospray source with integrated extractor. (center): Each emitter is surrounded by a proximal electrode to achieve low-voltage activation of the emitter. The emitters are coated with a conformal carbon nanotube porous layer that increases transport of liquid to the emission sites (emitter tips). The extractor and the emitting dies are assembled using a set of DRIE-patterned deflection springs—a technology the group pioneered for HV MEMS.

Compact Parameterized Modeling of Radio Frequency Nano-Electro-Mechanical Resonators

Design and optimization of novel RF Nano-Electro-Mechanical (NEM) resonators such as Resonant Body Transistors require modelling across multiple cross-coupled domains, including mechanical (distributed stress and elastic wave models), electrical (semiconductor devices and RF small signal models), and thermal. To address this need, the group has developed an algorithm that automatically generates compact models for NEM resonators. The resulting compact models allow the circuit designers to run circuit-level direct current, transient, AC, and periodic steady state analyses using any commercial circuit simulator. The models are parameterized. Values for the model coefficients are calibrated using measurements from NEMS resonator devices. The algorithm guarantees that when circuit designers arbitrarily change values for the device parameters, the instantiated models will never cause numerical instabilities and convergence issues when connected to other device models and circuits within the circuit simulator. Results show high-quality fit to the measured data, even in the presence of noise and spurious resonant peaks.



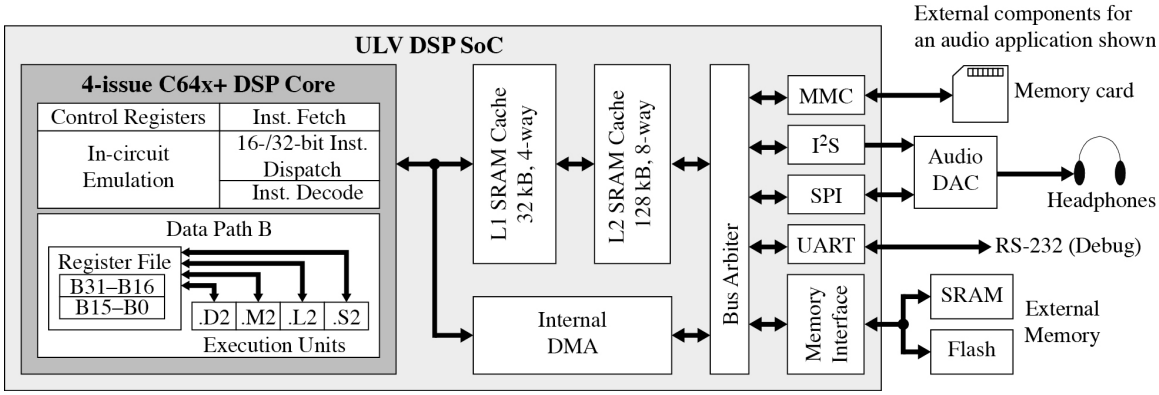
Acoustic Bragg reflectors diagram.



Measured data on a Si-based NEMS-CMOS (blue noisy line) and the output from our model (red smooth line).

Optimizing a Cellphone-class Digital Signal Processor for Highly Voltage-scalable Operation

Digital logic circuits are most energy efficient when operated at very low (near subthreshold) voltages. However, significant variation of the transistor threshold (VT) voltage from transistor to transistor complicates designing ultra-low voltage circuits. Working in close collaboration with Texas Instruments, the group developed a modified implementation of an existing Texas Instruments 4-issue VLIW digital signal processor (DSP) system-on-chip (SoC), optimizing it to operate across voltages ranging 1.0 V down to 0.6 V. The goal of the project was to achieve reliable ultra-low voltage operation with corresponding ultra-low power, without compromising high performance at high voltages. The SoC was implemented in 28 nm CMOS, using logic cells and static random-access memory cells optimized for both high-speed and low-voltage operating points. A new statistical static timing analysis methodology was also used on this design, in order to more accurately model the effects of local VT variation and achieve a reliable design with minimal extra margin. The chip has been verified to be operational from 587 MHz at 1.0 V (113 mW) down to 3.6 MHz at 0.34 V (720 μW) when operating from external memory (caches disabled).



Block diagram of the voltage-scalable DSP system-on-a-chip.

Awards and Honors for Core Faculty

Vladimir Bulović: Semiconductor Equipment and Materials International Award for North America (2012), and Faculty Research Innovation Fellowship (2011).

Trisha Andrew (Vladmir Bulović postdoctoral researcher): L'Oreal Fellowship (2011).

Pablo Jarillo-Herrero: Department of Energy Early Career Award (2011–2012), and Presidential Early Career Award for Scientists and Engineers (2011–2012).

Tomás Palacios: Awarded tenure with EECS, Presidential Early Career Award for Scientists and Engineers (October 2011), and IEEE Distinguished Microwave Lecturer on Nanotechnology (2011–2013).

Jesús del Alamo: 2012 Intel Outstanding Researcher Award in Emerging Research Devices.

Donghyun Jin (Jesús del Alamo group): "Mechanisms Responsible for Dynamic On-resistance in GaN High-voltage High Electron Mobility Transistors [HEMTs]," Charitat Award Runner-up, International Symposium on Power Semiconductor Devices 2012, Brugges, Belgium.

Sung Jae Kim (Jongyoon Han group): Poster award at MARC2012 (January 2012), and winner of Technology Idol event, organized by Global Water Intelligence.

Zohaib Mahmood, Luca Daniel: "Guaranteed Passive Parameterized Modeling of Multiport Passive Circuit Blocks," Proceedings of TECHCON Conference 2011, Austin, TX (September 2011).

Ling Xia: "Effects of Strain on p-channel III-V FETs for Beyond-silicon CMOS Applications," MTL Doctoral Dissertation Seminar, Spring 2012.

Zheng Zhang, Ibahim Elfadel, Luca Daniel: "Model Order Reduction of Fully Parameterized Systems by Recursive Least Square Optimization," Best Paper Award nomination, IEEE/Association for Computing Machinery International Conference on Computer-aided Design (November 2011).

Vladimir Bulović
Director
Professor of Electrical Engineering