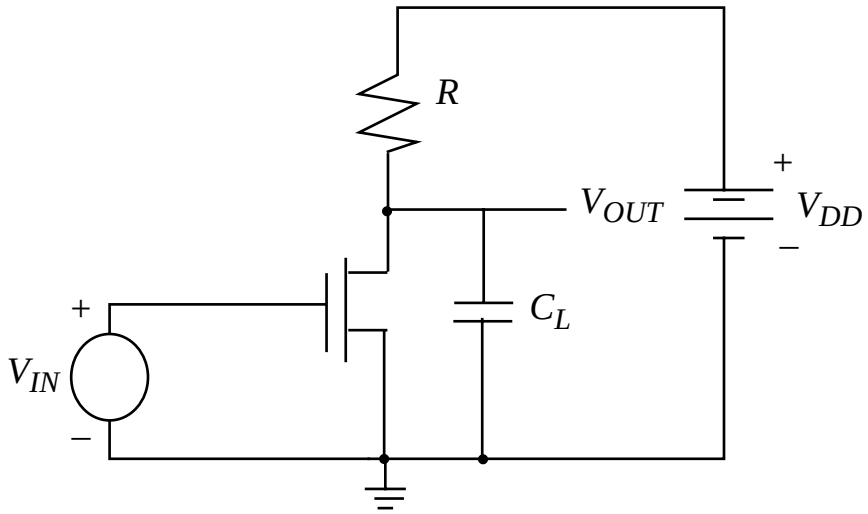
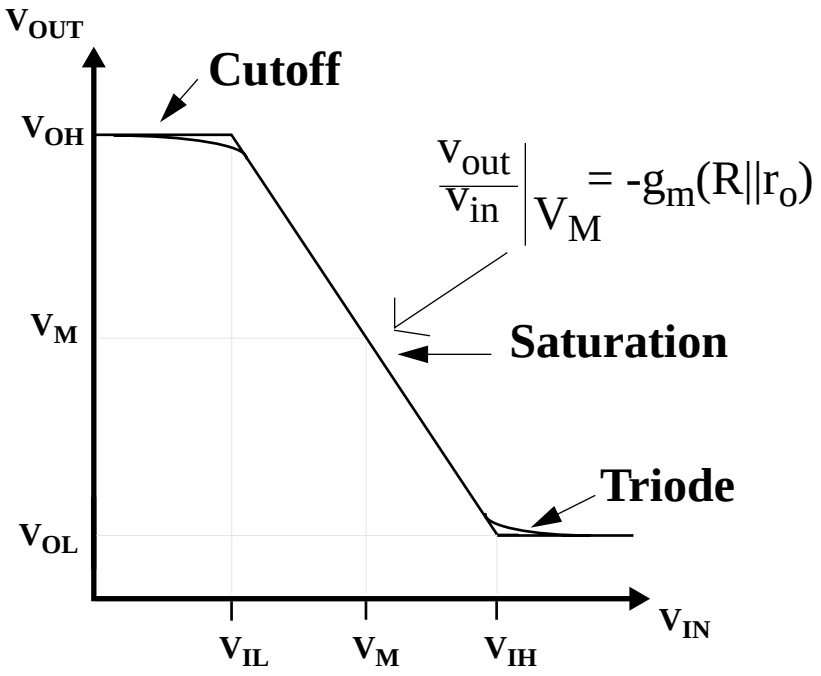
I. NMOS Inverter with Resistor Pull-Up



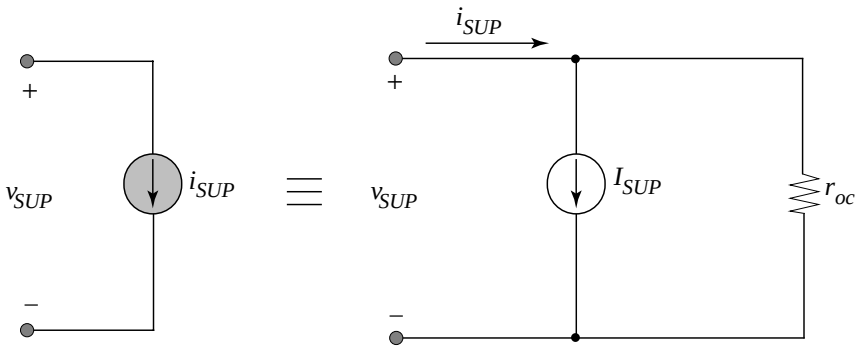


II. NMOS Inverter with Current-Source Pull-Up

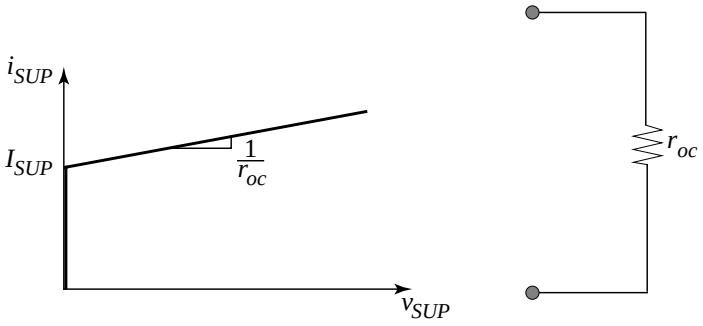
A. Motivation

- With the resistor pull-up we could increase R to sharpen transfer characteristic BUT it slows down inverter operation.

B. Idealized Current-Source "Pull-Up"



(a)

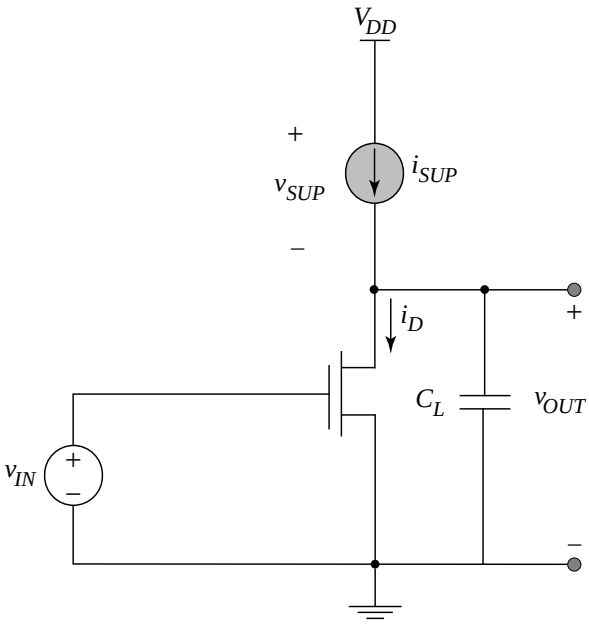


(b) (c)

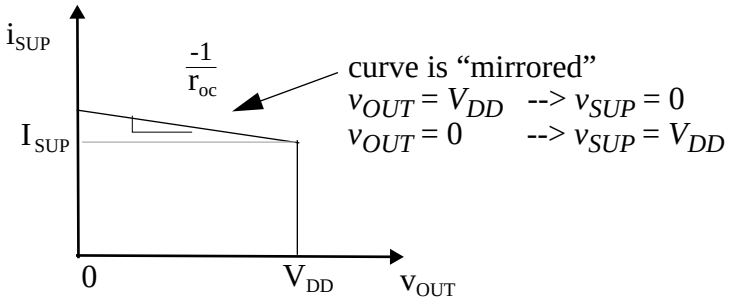
- Incremental resistance can be large --> high small-signal gain
- Current is large ---> Fast transitions

C. NMOS Inverter with Current-Source Pull-Up

- Replace resistor with current source

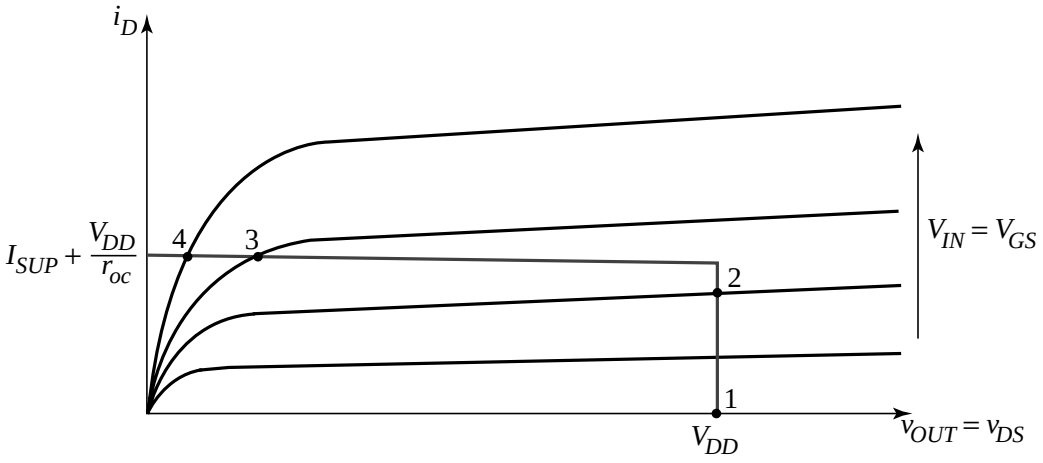


- Find the voltage transfer curve graphically by superimposing i_{SUP} vs. v_{OUT} (load line) on top of the drain characteristics

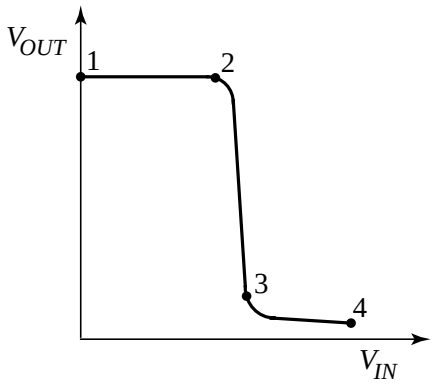


D. Load Line Analysis

- Voltage transfer curve is much closer to that of the ideal inverter



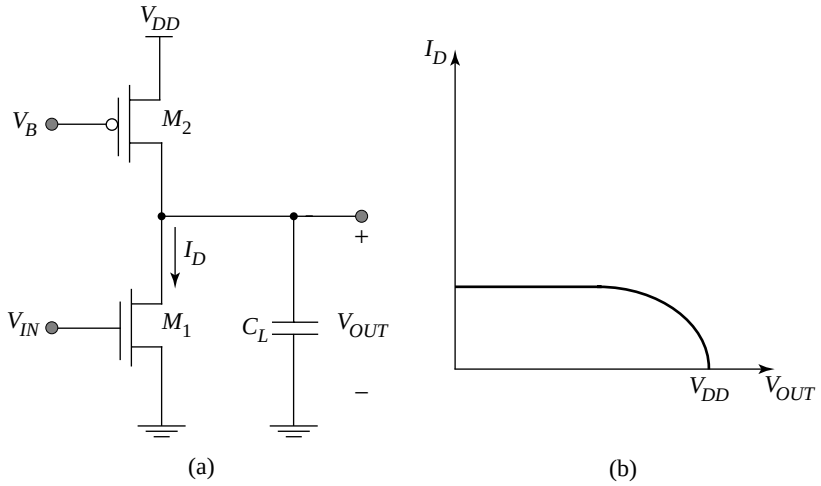
(a)

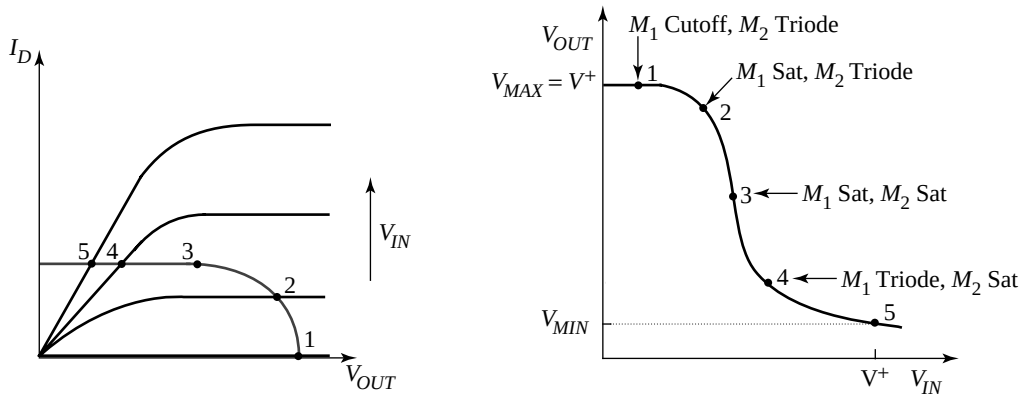


(b)

E. PMOS as a Current-Source Pull-Up

- Substitute p-channel MOSFET (with bulk connected to the source to make V_{SB} =0 and source connected to the supply voltage)
- The bias voltage V_B is selected so that the appropriate source-gate voltage drop is obtained: $V_{SG2} = V_{DD} - V_B$. The supply current i_{SUP} as a function of the supply voltage $v_{SUP} = V_{SD2} = V_{DD} - V_{OUT}$ is:





- In order to find the slope at $V_{IN} = V_M$, we note that both transistors are saturated there (near point 3) and that our small-signal models from Chapter 4 are valid

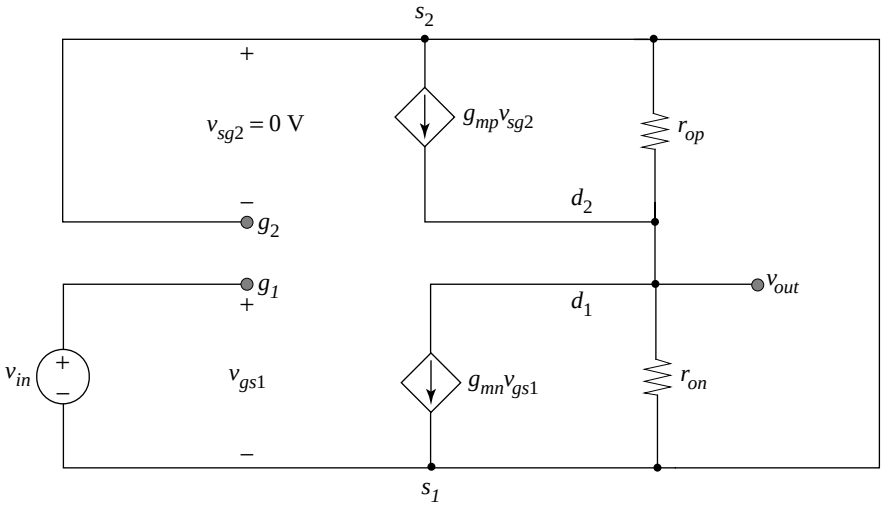
F. Calculate midpoint - V_M

- V_M is the input voltage V_{IN}, where the output voltage $V_{OUT} = V_{IN}$
- Both transistors are saturated
- Equate drain currents, omitting the channel length modulation terms

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(V_M - V_{T_n}\right)^2$$

$$-I_{Dp} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p\left(V_{DD} - V_B + V_{Tp}\right)^2$$

G. Find slope of transfer characteristic at V_M



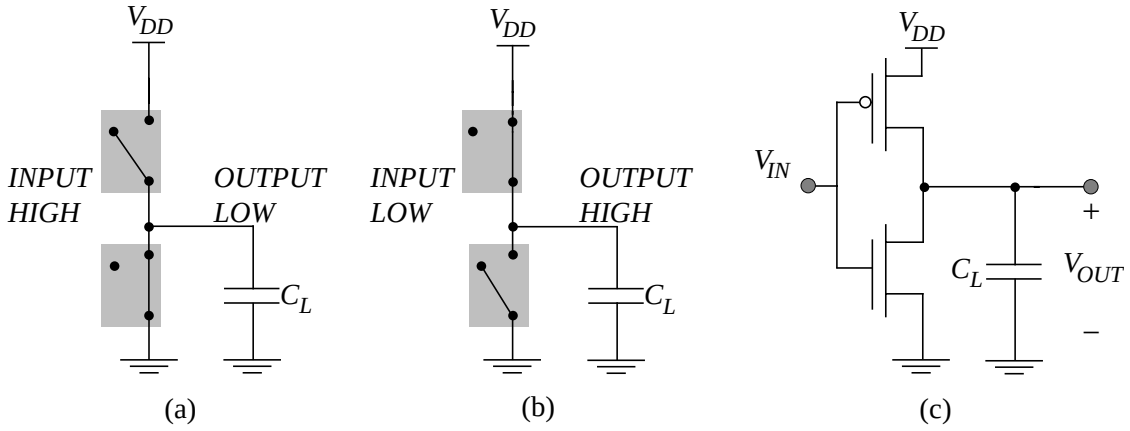
$$\left.\frac{dv_{OUT}}{dv_{IN}}\right|_{V_M} = \frac{v_{out}}{v_{in}} = -g_{mn}\left(r_{on}\,||\,r_{op}\right)$$

III. Complementary MOS (CMOS) Inverter

A. Motivation

- When input is high, the n-channel MOSFET is in the triode region conducting $I_D = I_L$ from V_{DD} to ground.
- Power dissipation of $P = I_L$ x V_{DD}
- Need a current source load which *itself* is switchable -- turning itself off when the output is low.

B. Concept

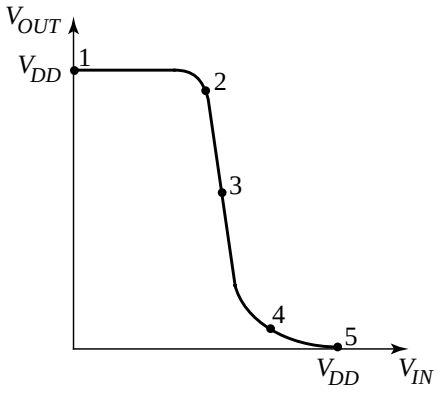


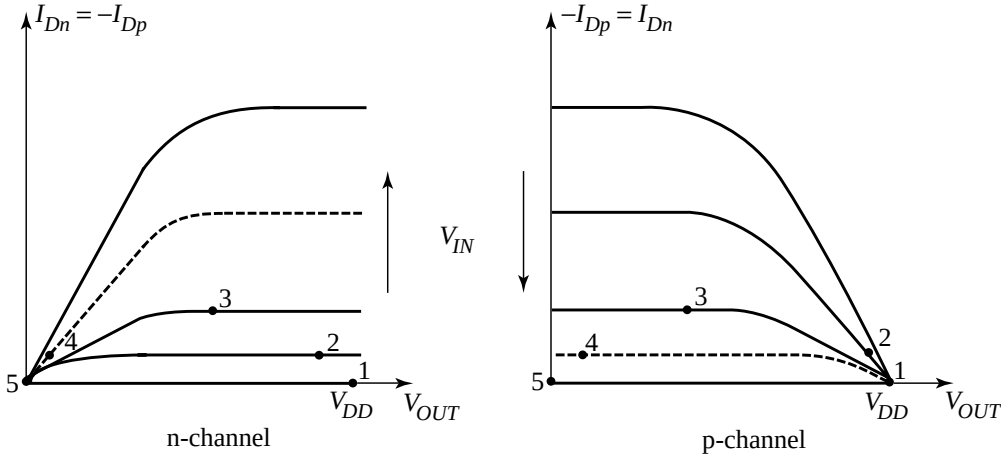
C. Practical realization:

- Connect input to gate of p-channel device.
- $V_{IN} = V_{DD}$ --> $V_{SG2} = V_{DD} - V_{IN} = 0 < |V_{Tp}|$ --> cutoff
- $V_{IN} = 0$ --> $V_{SG2} = V_{DD} - V_{IN} = V_{DD} >> |V_{Tp}|$ --> on (triode region)
- NMOS transistor is off when PMOS is in triode region
- PMOS transistor is off when NMOS is in triode region

D. CMOS Transfer Characteristic

- Plotting the p-channel load on the n-channel "driver's" drain characteristics allows us to find the input-output voltage pairs which satisfy the constraint
- $I_{Dn} = -I_{Dp}$





- We can arrange to have the upper and lower noise margins be identical, if the transistor geometries are selected appropriately

III. Quantitative Noise Margins

A. Calculate V_M

- V_M is the input voltage V_{IN}, where the output voltage $V_{OUT} = V_{IN}$
- Both transistors are saturated
- Equate drain currents, omitting the channel length modulation terms

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_M - V_{Tn})^2$$

$$-I_{Dp} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - V_M + V_{Tp})^2$$

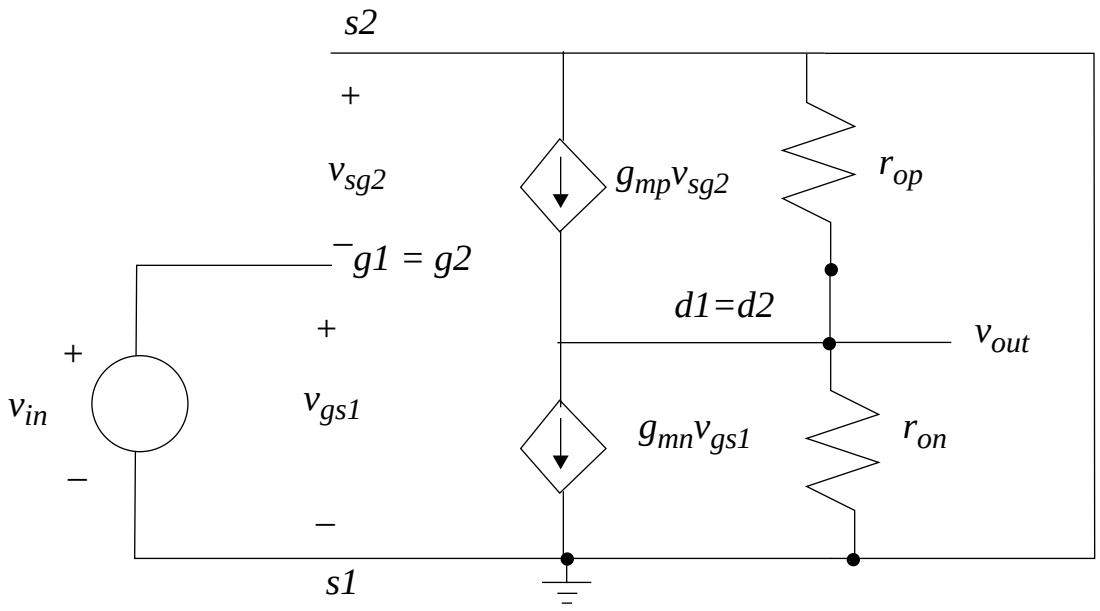
- Let $k_n = \mu_n C_{ox} (W/L)_n$ and $k_p = \mu_p C_{ox} (W/L)_p$

$$\frac{1}{2}k_n (V_M - V_{Tn})^2 = \frac{1}{2}k_p (V_{DD} - V_M + V_{Tp})^2$$

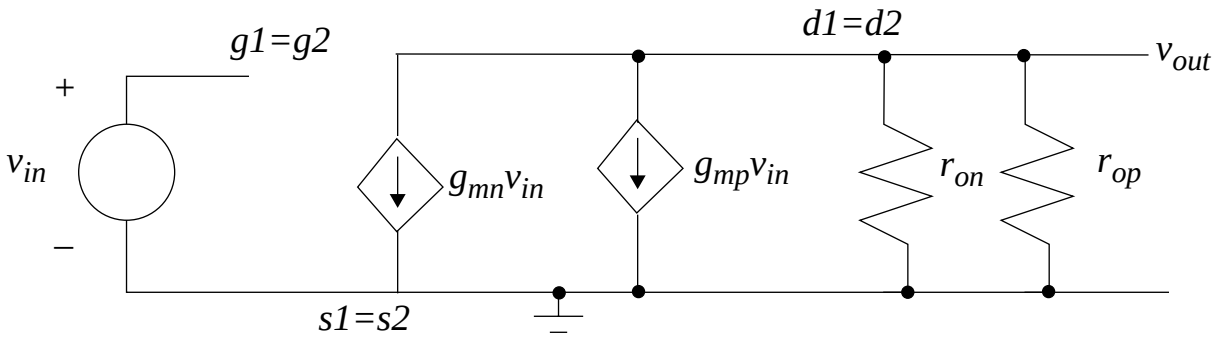
- Result:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

B. Small-Signal Model: CMOS Inverter at $V_{IN} = V_M$



- p-channel MOSFET small-signal source-gate voltage is $v_{sg2} = - v_{in}$



C. Approximate Transfer Curve

- The small-signal gain (which is the slope of the transfer curve when the input is equal to the mid-point voltage) is:

$$v_{out}/v_{in} = -(g_{mn} + g_{mp})\left(r_{on} \| r_{op}\right) = A_v$$

- An inverter optimized for gain can have values in the 100's.
- Real inverters have a channel length which is as small as possible (to minimize the area ... and maximize speed)
- Output resistance is lowered and a typical value is v_{out} / v_{in} = -5.

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{A_v}$$

$$V_{IH} = V_M - \frac{V_M}{A_v}$$