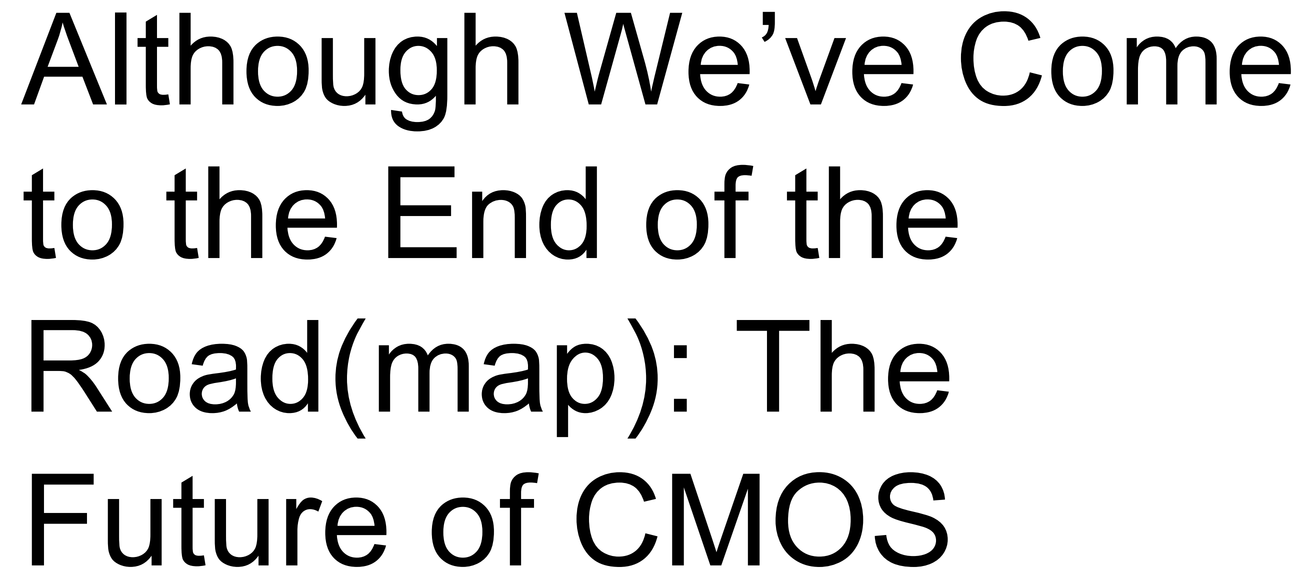

Although We've Come to the End of the Road(map): The Future of CMOS

Nicole DiLello

6.Insight

April 3, 2007

Boyz II Men

Although we've come
To the end of the road
Still I can't let go
It's unnatural
You belong to me
I belong to you

♥ *You = silicon* ♥

Outline

- Introduction
- Current technology
- Next generation
- 20 years from now
- Conclusion

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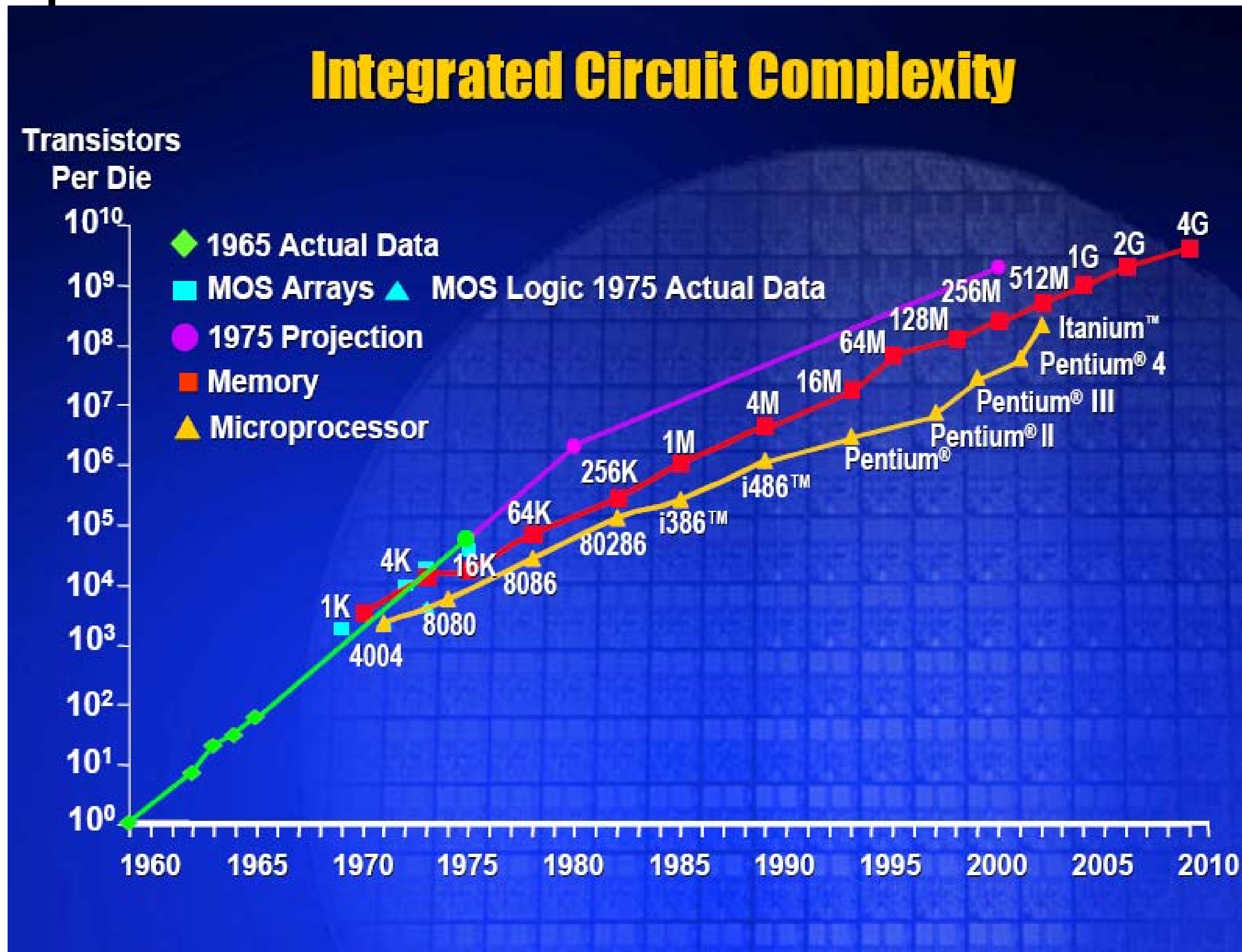
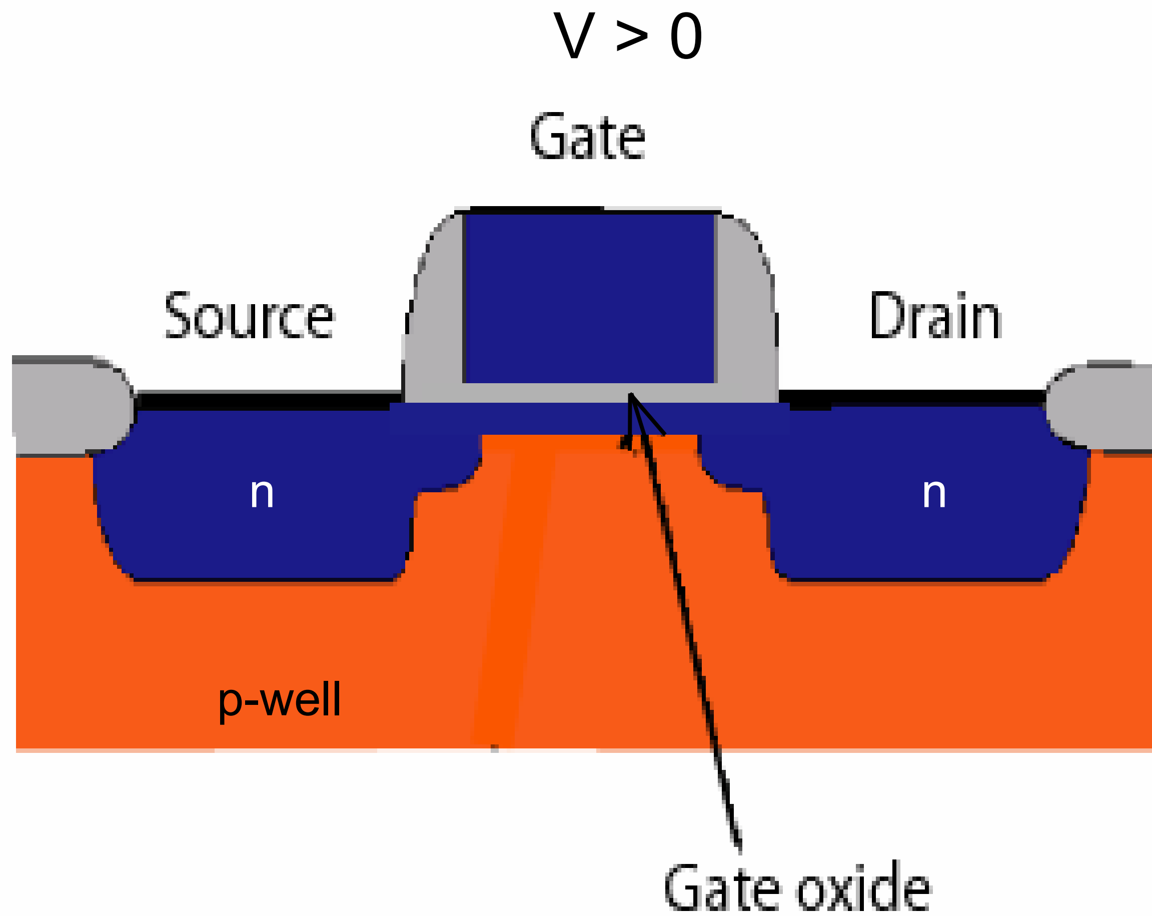
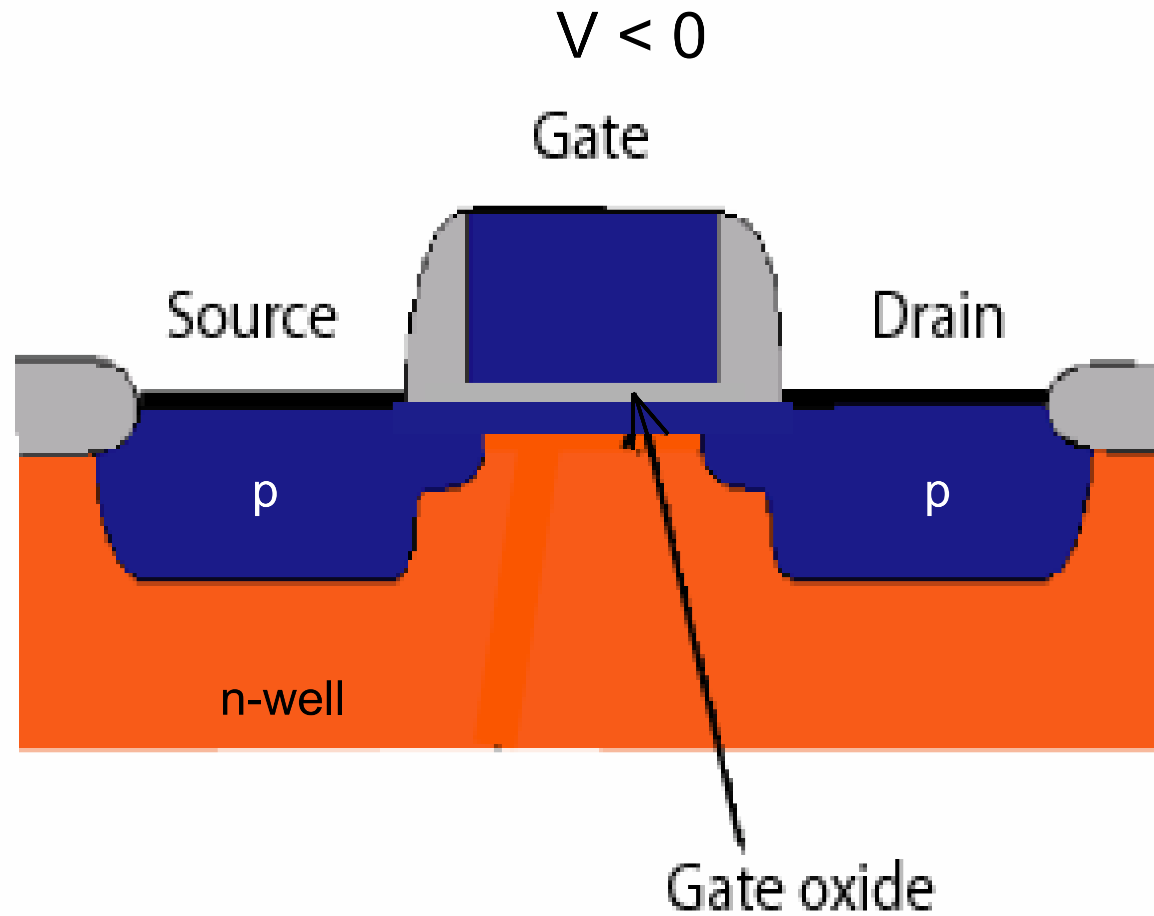
Moore's Law



nMOSFET



pMOSFET

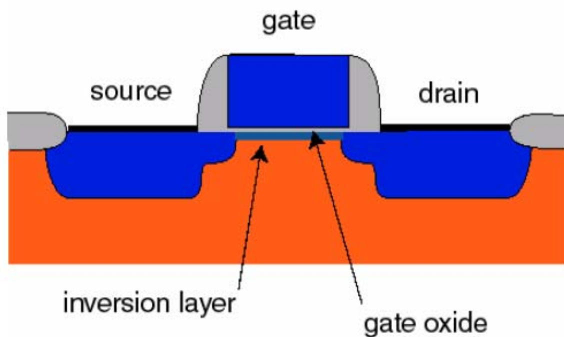


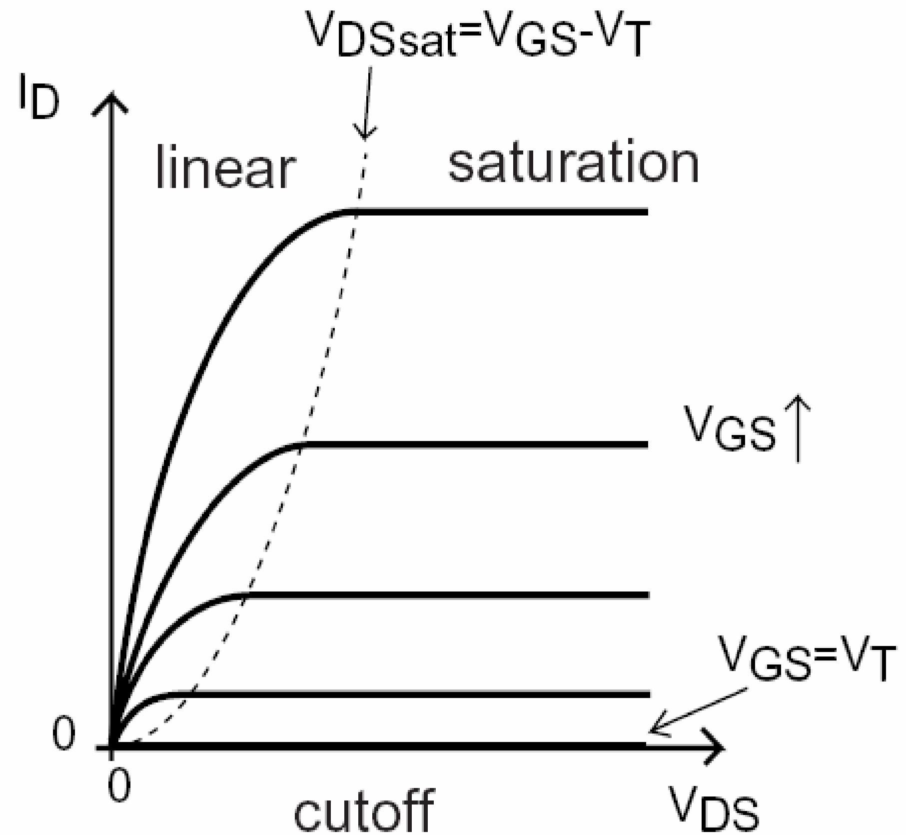
Before continuing…

- nMOS + pMOS = CMOS
- Standard MOSFET
  - Made entirely from Si
  - Crystalline
  - n/p regions are doped

p		n
5 10.811 B BORON	6 12.011 C CARBON	7 14.007 N NITROGEN
13 26.982 Al ALUMINIUM	14 28.086 Si SILICON	15 30.974 P PHOSPHORUS
31 69.723 Ga GALLIUM	32 72.64 Ge GERMANIUM	33 74.922 As ARSENIC

MOSFET Characteristics





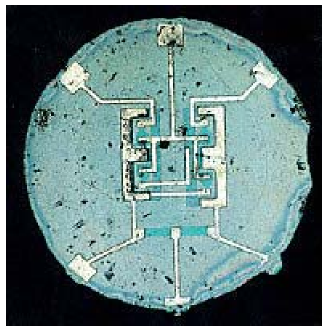
$$I_{D,linear} = \frac{W}{L}\mu\, C_{ox}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}$$

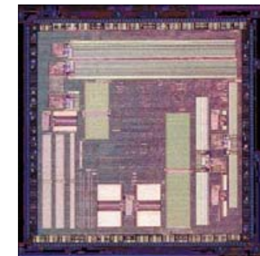
$$I_{D,Sat} = \frac{W}{2L}\mu\, C_{ox}(V_{GS} - V_T)^2$$

Following Moore's Law…

$$I_{D,linear} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS} \qquad I_{D,Sat} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_T)^2$$

- Make transistors smaller
- International Technology Roadmap for Semiconductors (ITRS)
  - U.S., Europe, Japan, Taiwan, Korea
  - Chip manufacturers, academia





ITRS (2005)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
$J_{g,limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm^2)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
UTB FD (µA/µm)				0.17	0.19	0.22	0.22	0.29	0.29
DG (µA/µm)							0.1	0.11	0.11

ITRS (2005)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
L_g: *Physical* L_{gate} *for High Performance logic (nm) [1]*	**11**	**10**	**9**	**8**	**7**	**6**	**5**
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	5	5					
DG (Å)	6	6	5	5	5	5	5
Gate Poly Depletion & Inversion-Layer Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	4	4					
DG (Å)	4	4	4	4	4	4	4
EOT_{elec}: *Electrical Equivalent Oxide Thickness in inversion [4]*							
Extended Planar Bulk (Å)							
UTB FD (Å)	9	9					
DG (Å)	10	10	9	9	9	9	9
$J_{g,limit}$: *Maximum gate leakage current density [5]*							
Extended Planar Bulk (A/cm^2)							
FDSOI (A/cm^2)	3.27E+03	3.70E+03					
DG (A/cm^2)	1.00E+03	1.10E+03	1.22E+03	1.38E+03	1.57E+03	1.83E+03	2.20E+03
V_{dd}: *Power Supply Voltage (V) [6]*	0.9	0.8	0.8	0.7	0.7	0.7	0.7
$V_{t,sat}$: *Saturation Threshold Voltage [7]*							
Extended Planar Bulk (mV)							
UTB FD (mV)	164	166					
DG (mV)	190	192	195	200	201	205	208
$I_{sd,leak}$: *Source/Drain Subthreshold Off-State Leakage Current [8]*							
Extended Planar Bulk (μA/μm)							
UTB FD (μA/μm)	0.36	0.37					
DG (μA/μm)	0.11	0.11	0.11	0.11	0.11	0.11	0.11

Red brick wall

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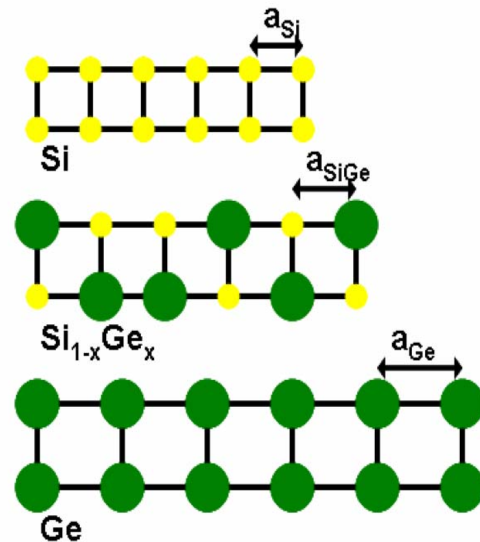
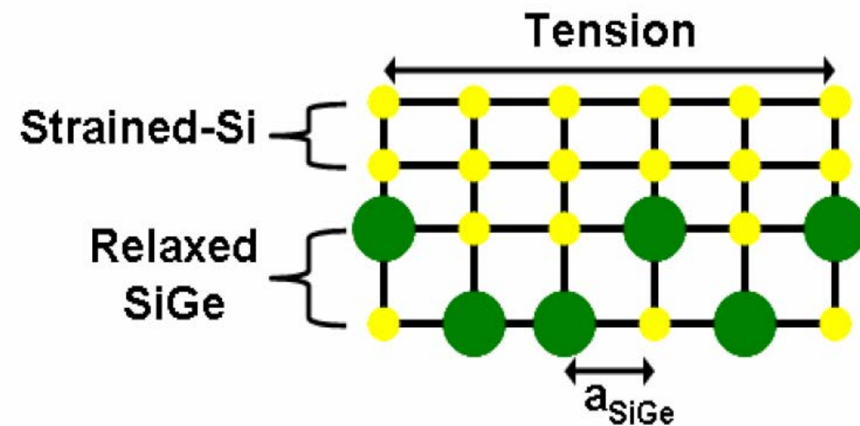
Strain Engineering - nMOS

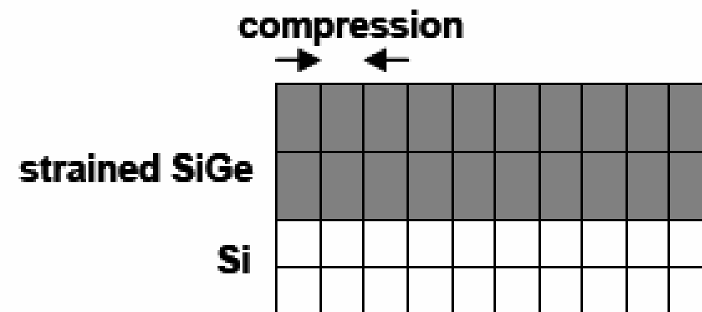
$$I_{D,linear} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}$$

$$I_{D,Sat} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_T)^2$$





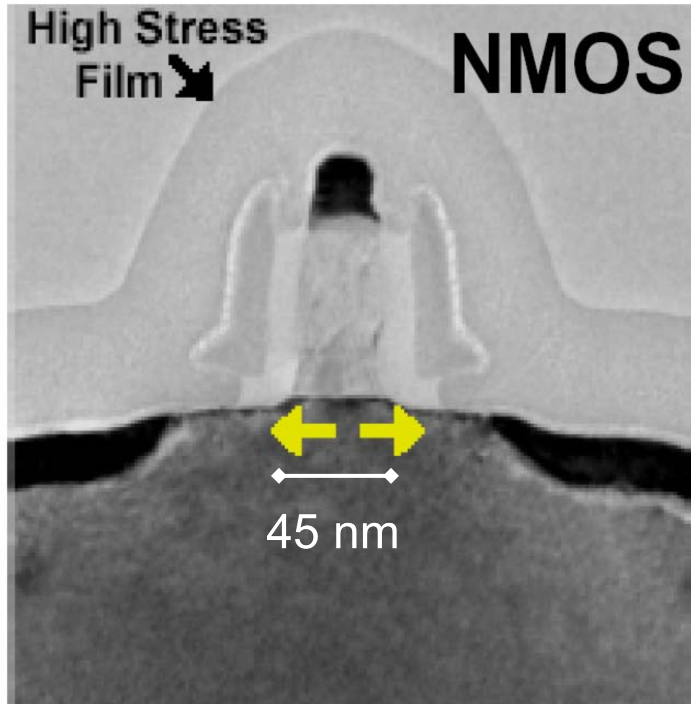
Strain Engineering - pMOS

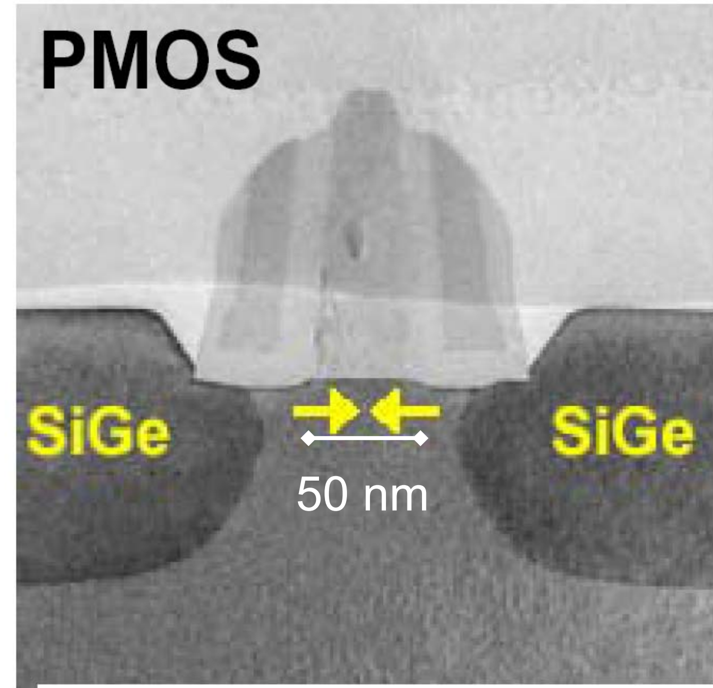


μ_e increases for tensile strain

μ_h increases for compressive strain

Current Production





Nitride film causes tensile stress in channel → increase μ_e

SiGe causes compressive stress in channel → increase μ_h

Can induce stress for both nMOS and pMOS on the same wafer!

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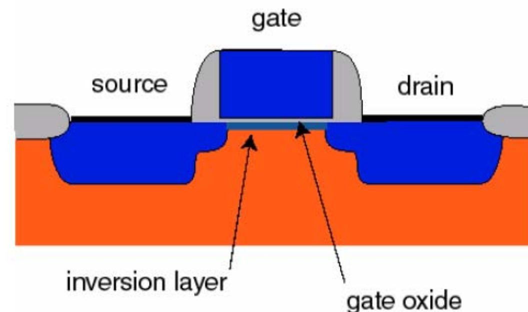
C_{ox} rears its ugly head

$$I_D = \frac{W}{L}\mu_e C_{ox}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}$$

$$I_D = \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_T)^2$$

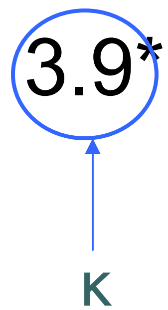
Problems with both!

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$



SiO_2: How do I love thee? Let me count the ways…

- Native oxide for Si → easy to grow
- Good quality: resistant to water, other atmospheric elements
- Matches Si lattice well → no dangling bonds
- High breakdown voltage
- $\varepsilon_{SiO2} = 3.9 * \varepsilon_0$

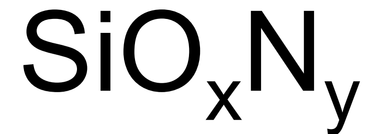


High-κ (k, if you're lazy)

- Measured in terms of "equivalent oxide thickness" (EOT)
- Can make thicker layers
  - $t_{ox} \approx 1$ nm

$$t_{high-\kappa} = \frac{\kappa_{high-\kappa}}{\kappa_{SiO_2}} t_{SiO_2}$$

If κ = 16, can have a thickness of 4 nm that gives roughly the same C_{ox} as 1 nm of SiO_2.



SiO_xN_y

- Relatively easy to integrate (just add some N_2)
- Increases κ a bit (κ_{Si3N4} ~ 7)
- Intel introduced at 90 nm node (2004)
- Probably limited to a thickness of ~1.3 nm
- Need a better fix

Some Other Options

TABLE I. Comparison of relevant properties for high-κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

[a]Calculated by Robertson (See Ref. 153).

[b]Mono.=monoclinic.

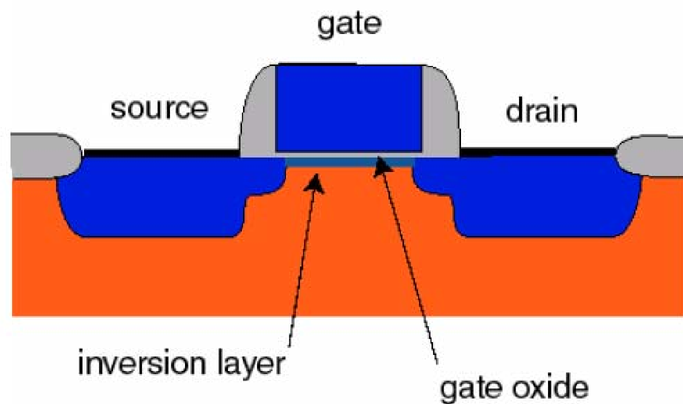
[c]Tetrag.=tetragonal.

Pick me!

Intel's Announcement

- Jan. 27, 2007, *New York Times*: 45 nm process (in production later this year) will use Hf-based dielectric (HfO_2? Si-based alloy? Shhhh…) and metal gate
- Leakage current is down, drive current is up, power consumption is down
- IBM: Hey, we did it too!

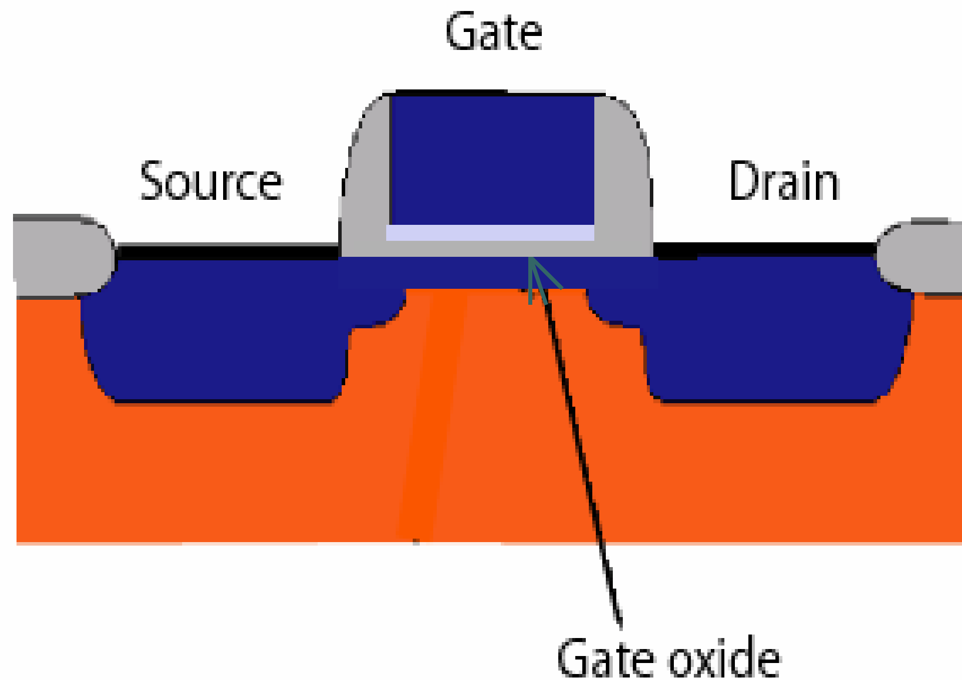
Poly-Si Gates



- Currently: gates made from poly-Si
- Doped at $>10^{20}$ cm^{-3}
- Pro: same material for nMOS and pMOS
- Cons: Can only dope so high, poly depletion effects

Poly depletion

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$



Deplete 3 – 4 Å in the gate → adds 3 – 4 Å to dielectric (significant when dielectric is 12 Å) → reduces C_{ox}

Metal Gate

- No poly depletion
- Lower series resistance
- Different for nMOS and pMOS

- Incorporating SiGe, Hf-based dielectric, and metal gates show that the industry is willing to (slowly) incorporate new materials

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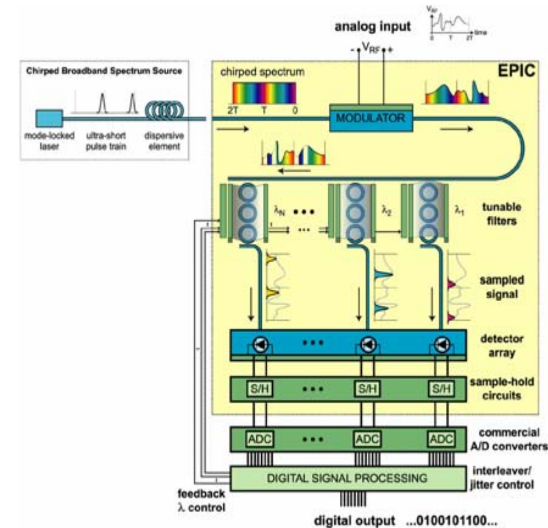
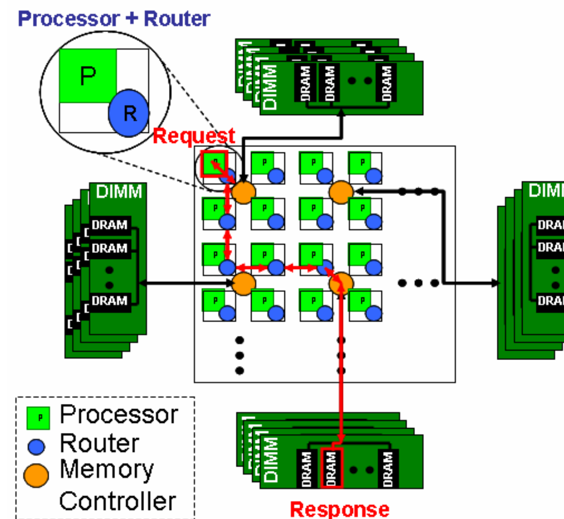
Look at bigger picture

- What if we change the mode of transportation entirely?
  - Tunneling FET (TFET)?
  - Carbon nanotubes?
  - Computation bubbles?
  - PHOTONICS!
- Before we go crazy-nuts, should probably look into a hybrid system

Integrated electronic/photonic system

- Photonics are good for transmitting data, high frequency applications
- Electronics are good for processing data, especially in a small area
- Let's use both!



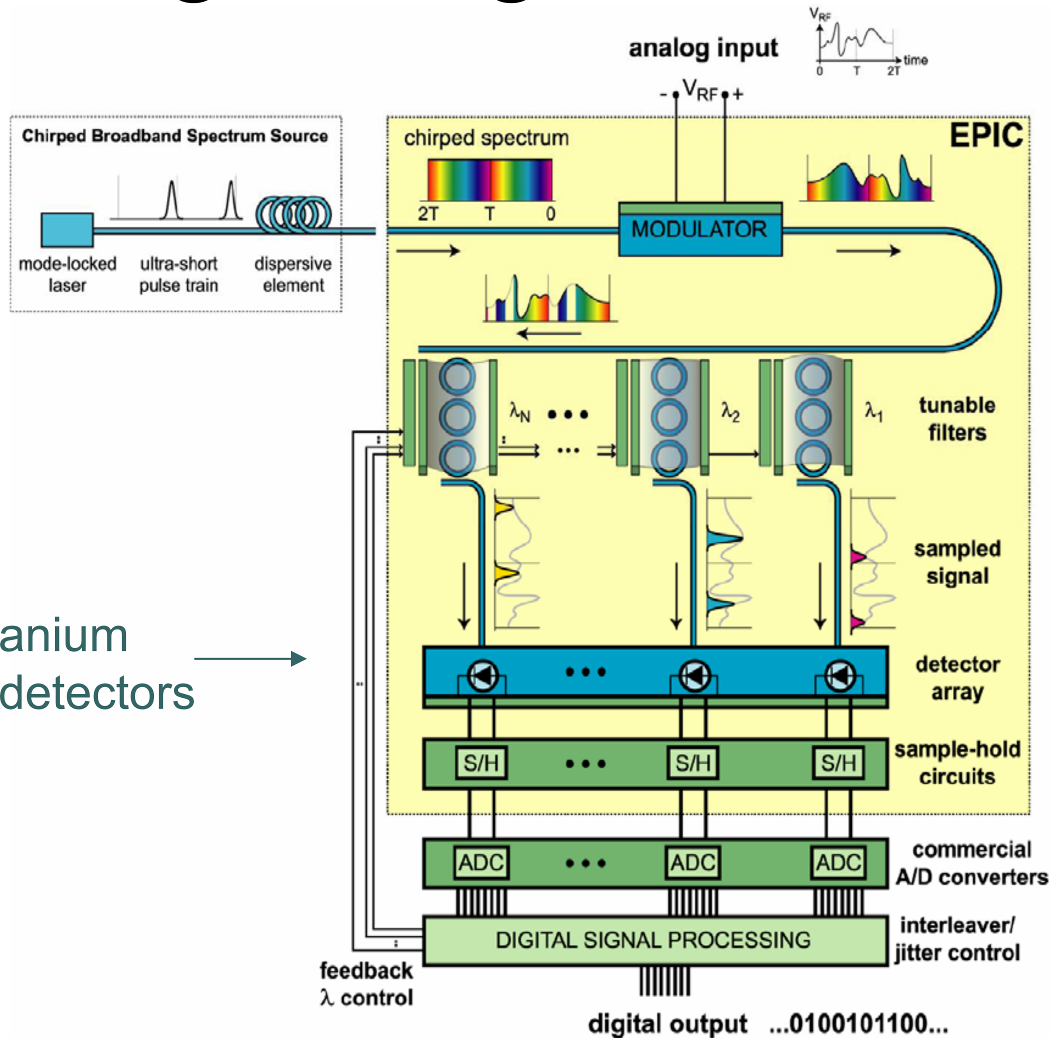


Analog-to-digital Converter

Use of a mode-locked laser → low sampling jitter!

Germanium photodetectors

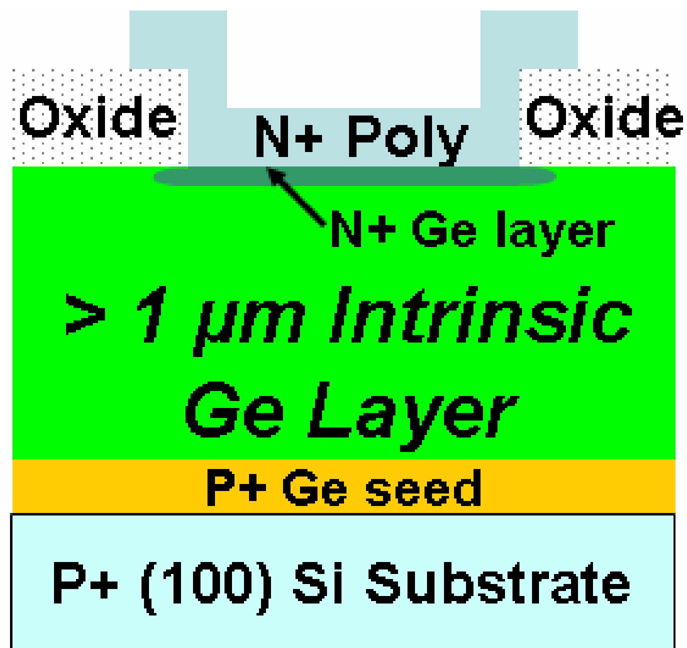
Parallel processing on different wavelengths

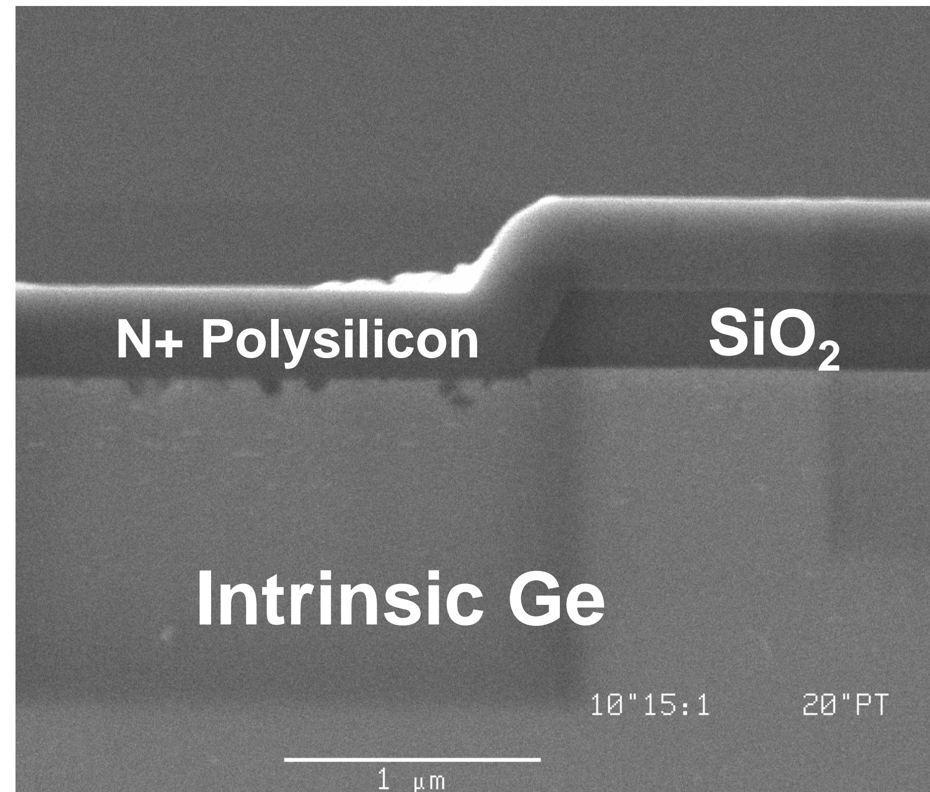


But still Si-based

- Everything on-chip → faster!
- Integrate laser
- Si modulator
- Ge photodetectors
  - SiGe already in CMOS process
- SiO_2 and SiN_x waveguides
  - Already in CMOS process
- Key: Optical sampling drastically reduces the timing jitter

Germanium photodiode

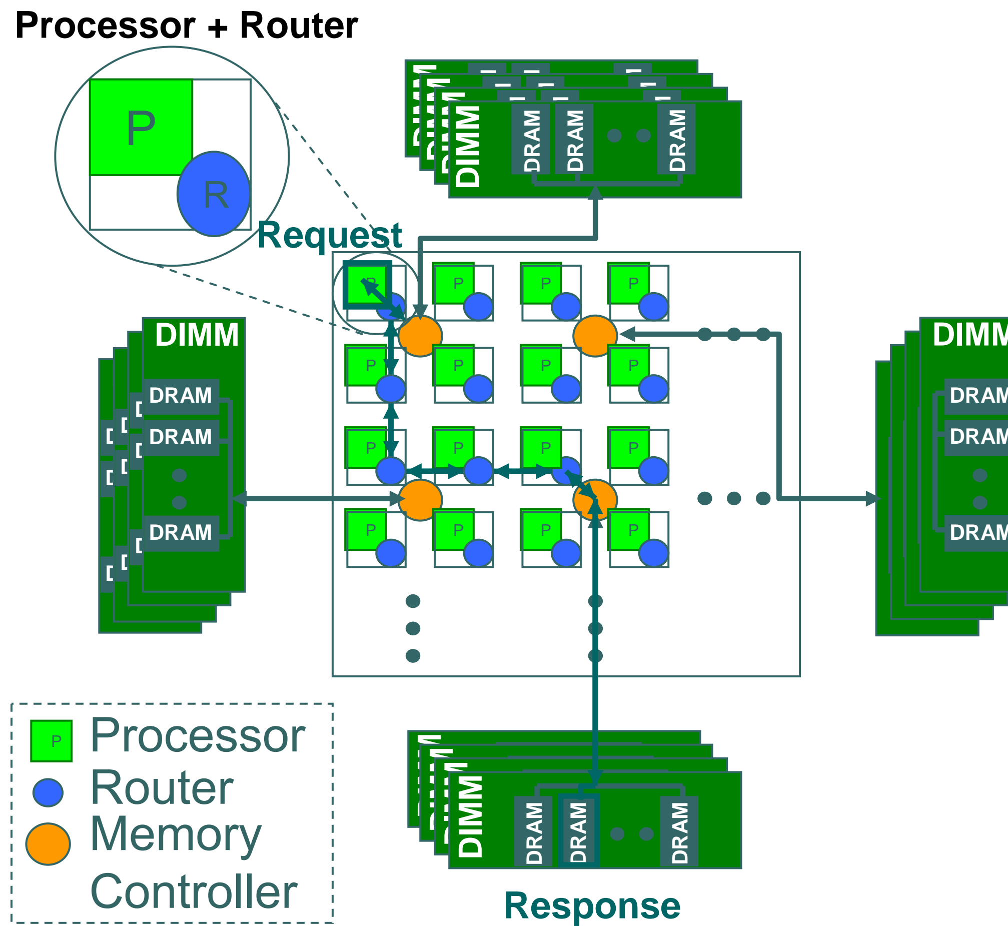




Another system: Multi-core Processor

- Working within an existing CMOS process
- Materials constraints
- Process constraints
- Pros: 1,000 cores, much more energy efficient, faster

Diagram of System



Helpful Classes

- Devices: 6.012, 6.720J, 6.728, 6.730, 6.731
- Processing: 6.152J, 6.774, 6.781
- Optics/Photonics: 6.013, 6.630, 6.631
- Circuits: 6.002, 6.301
- Computer Architecture: 6.823

Groups at MIT

- Strain engineering – Hoyt, Fitzgerald
- High-κ materials – Antoniadis
- Electronic Photonic Integrated Circuits (EPIC) – Kaertner, Hoyt, Ram, H.I. Smith, Ippen
- Multi-core processor – Stojanovic, Asanovic, Hoyt, Ram, Kaertner, H.I. Smith, Schmidt

Conclusions

- “No exponential is forever, but we can delay ‘forever.’”
- New materials: whoo!
- Electronic photonic architectures: whoo!