When (Low) Power Really Matters

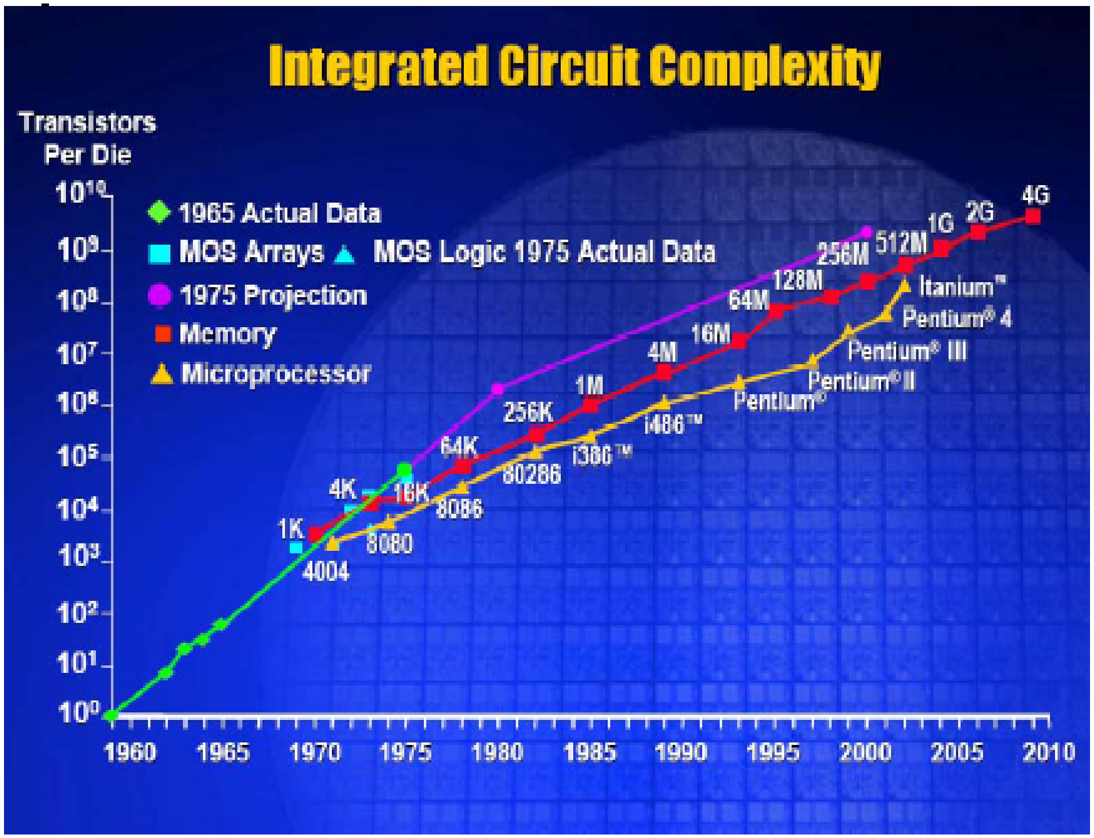
Yogesh K. Ramadass, AnanthaGroup

Microsystems Technology Laboratory

Outline

- **Introduction**
- **Voltage Scaling techniques**
- **Challenges with Low voltage operation**
- **System Examples**
- **Conclusion**

Moore's Law

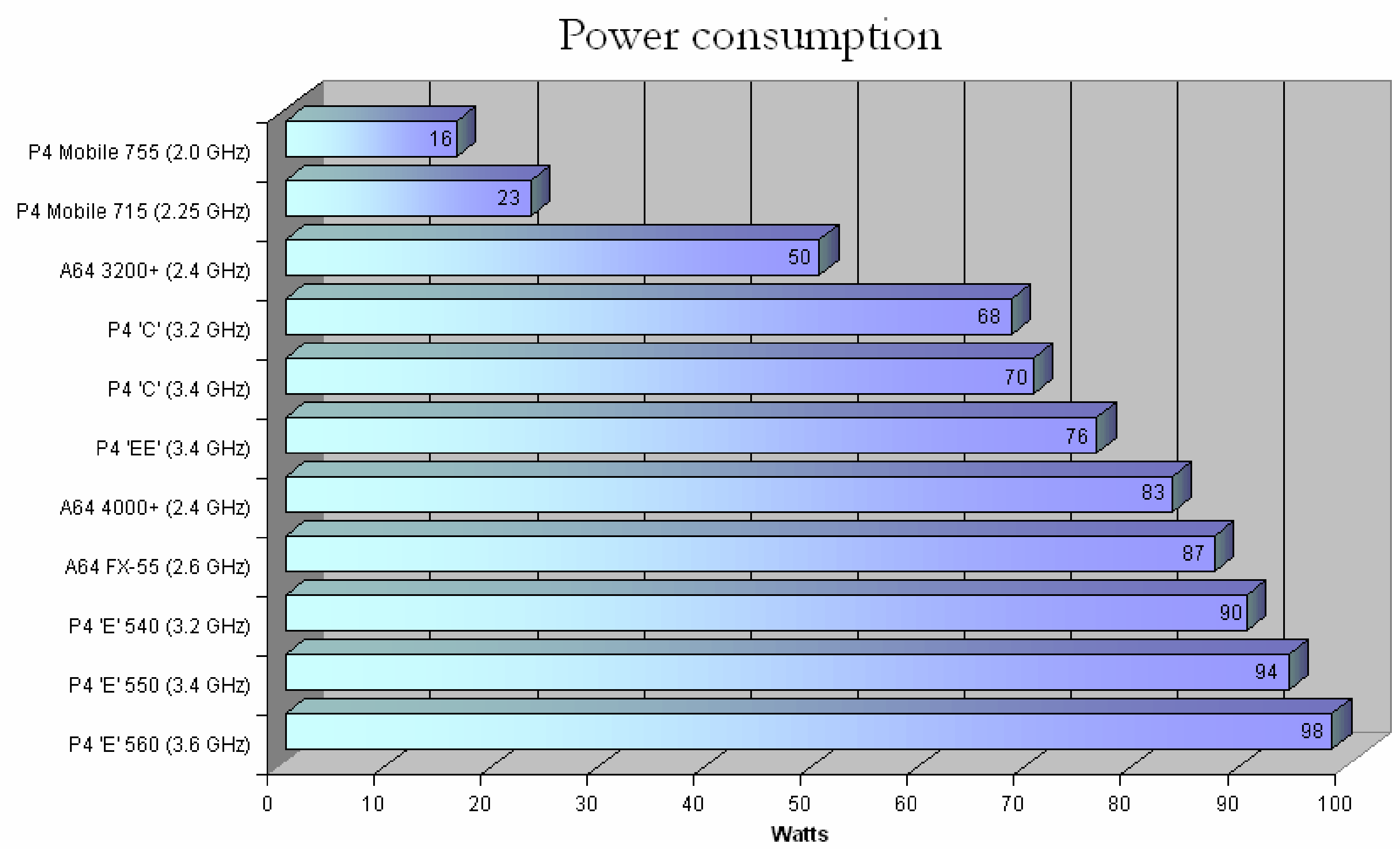


Gordon Moore

Co-founder, INTEL

- **No. of transistors doubles every two years**
- **Not a physical law, started of as a graphical observation**
- **Exponential increase in circuit complexity**

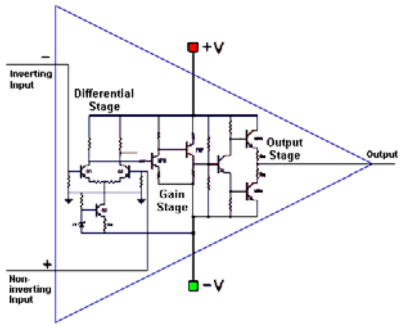
Processor Power Levels



- **More Speed → More Power**
- **More Processing → More Power**

So Where is the Power Lost?

- Analog Circuits – Opamps, ADC/DAC's, Current/Voltage references
  - Bias Currents
  - Switches



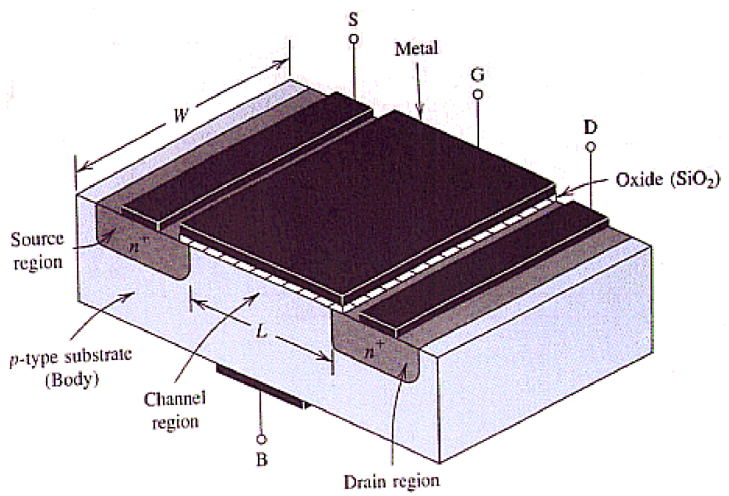
- Digital Circuits – Processors, Memory
  - Charging up capacitances

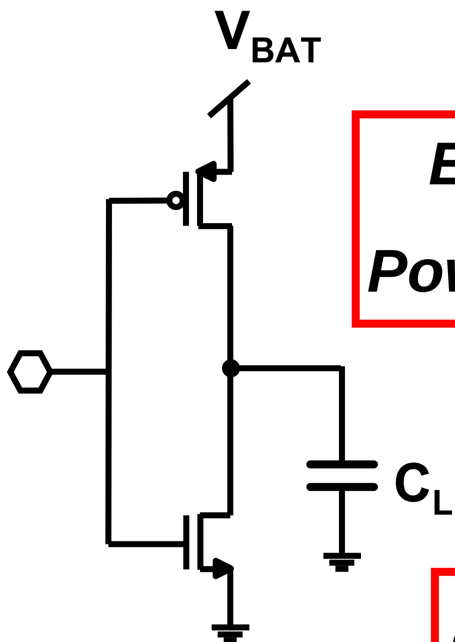
- Leakage!!
  - Imagine burning calories when sitting idle
  - 30% of total power in big microprocessors
  - More on this later

A simplistic view of process scaling

250, 180, 130, 90, 65, 45, 32, 22

Process Scaling enables Moore's Law





$$E_{cycle} = C_L V_{BAT}^2$$

$$Power = C_L V_{BAT}^2 . f_s$$

$$f_s \propto \frac{(V_{BAT} - V_T)^2}{C_L . V_{BAT}}$$

- Reduce C_L, reduce power
- Area reduces too!!
  - Area = Cost
- Faster switches
  - More processing
- Downside, switches don't turn off completely

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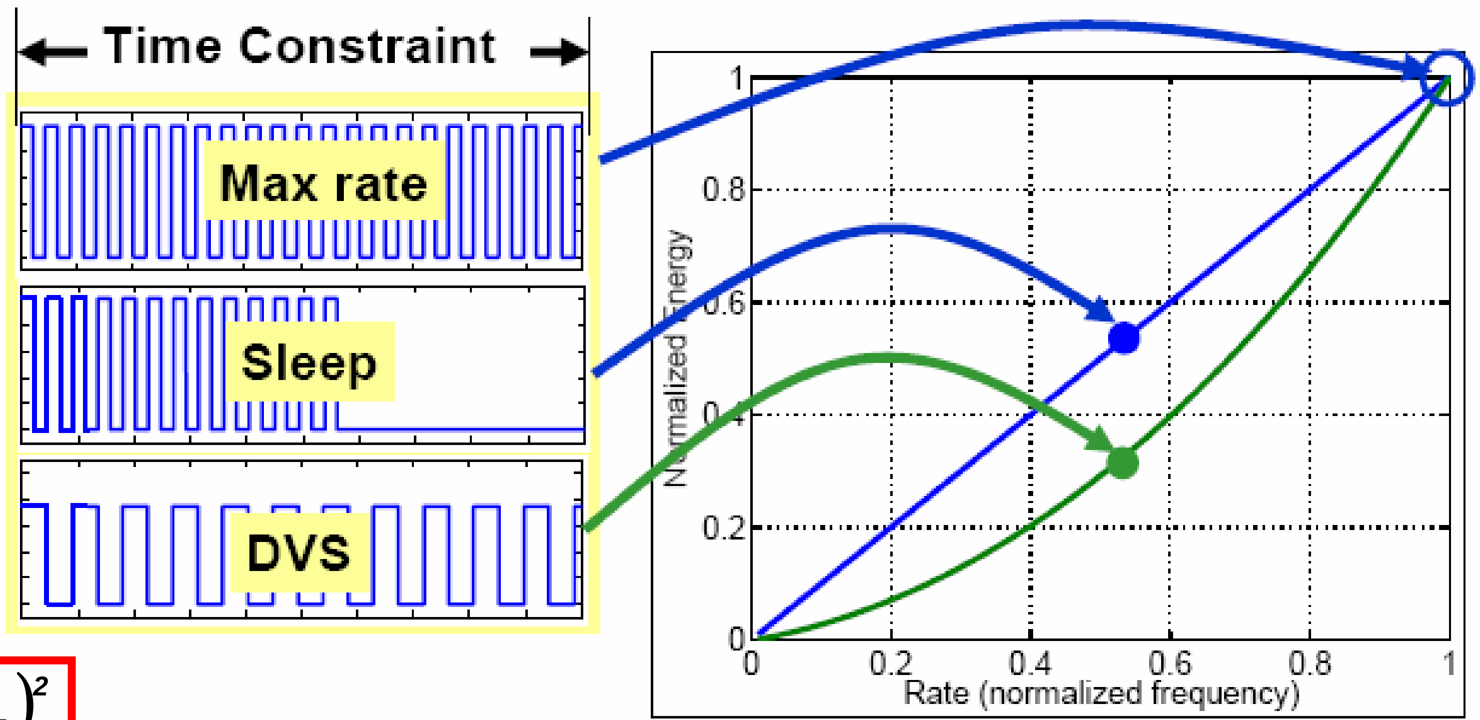
Dynamic Voltage Scaling



$$f_s \propto \frac{(V_{BAT} - V_T)^2}{C_L . V_{BAT}}$$

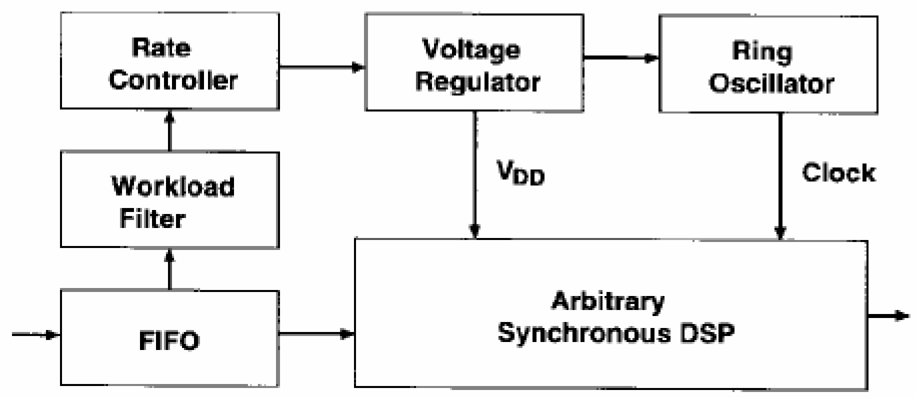
Dynamic Voltage Scaling with infinite levels saves energy per sample when the workload varies

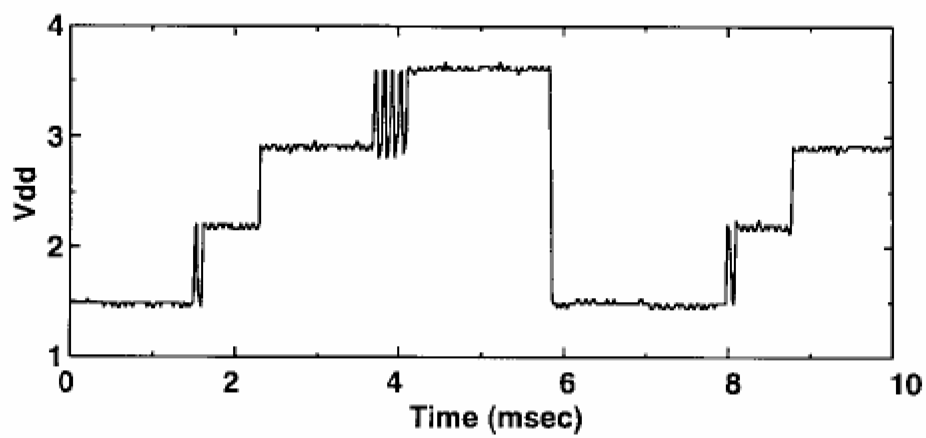
B. Calhoun

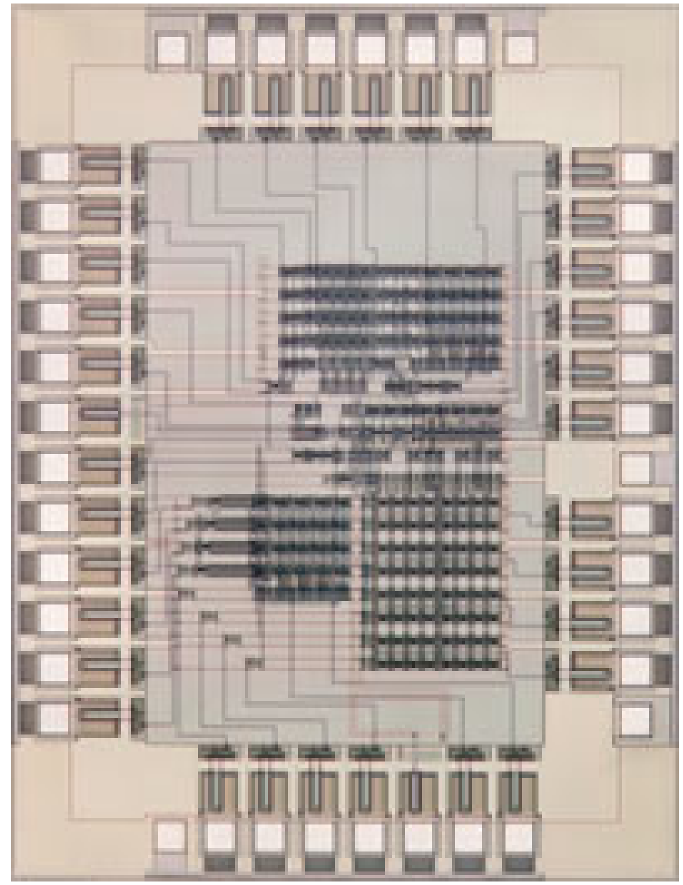
Goal: Operate Circuits at just enough voltage

Implementation of a DVS System

Change Voltage with change in workload



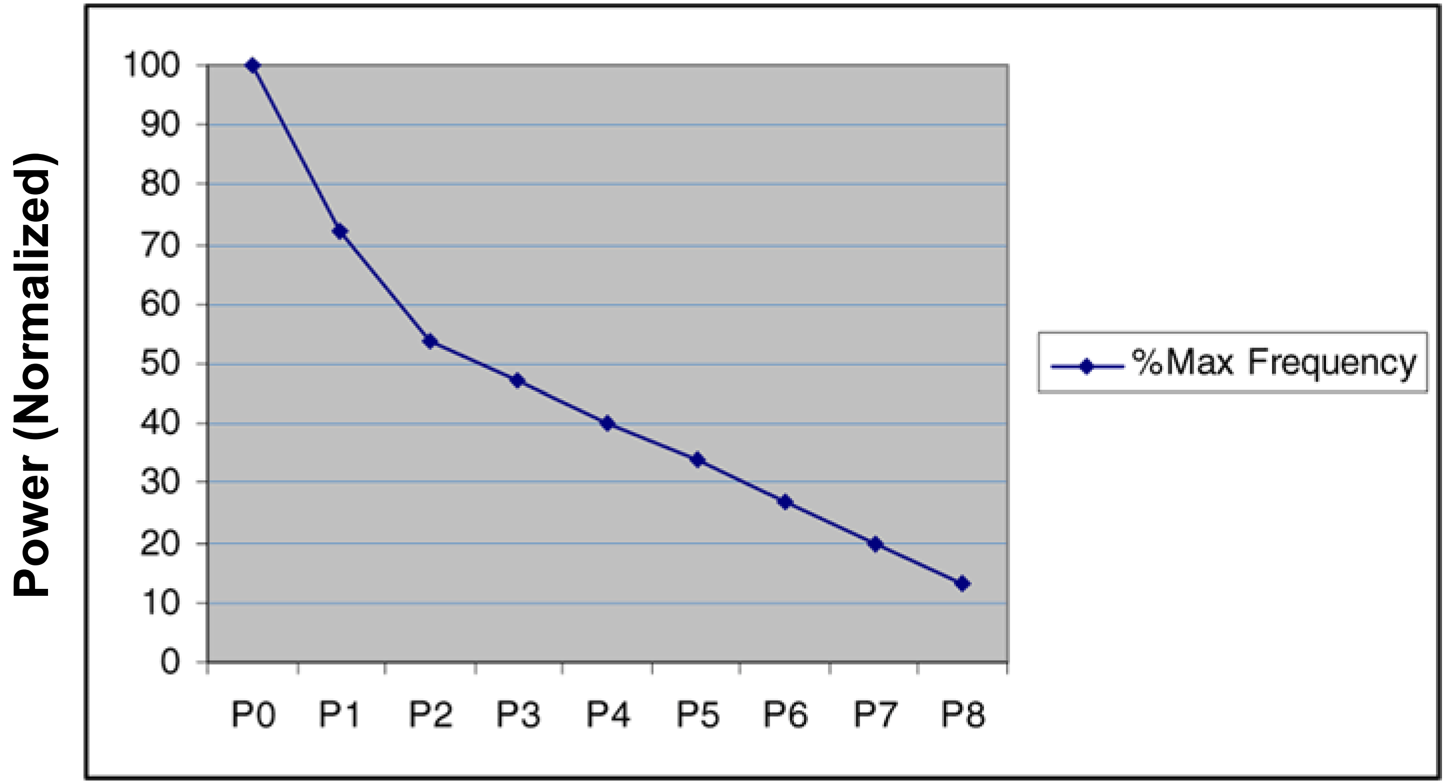




V. Gutnik
1996

Power Savings by DVS

Intel Core Duo Processor

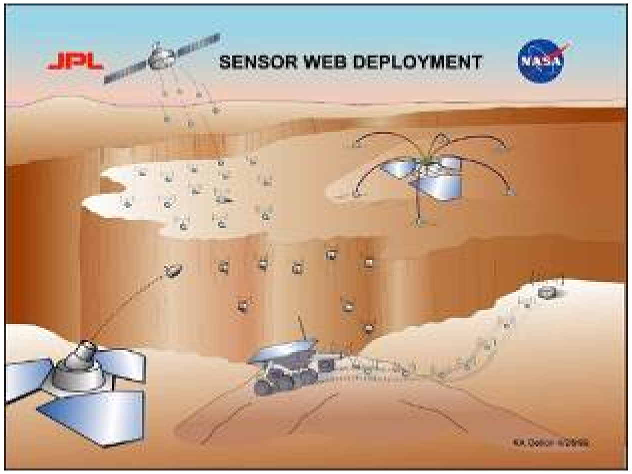


Courtesy : intel.com

- Exponential drop → both voltage and frequency scale
- Linear drop → only frequency scales, min. voltage

Energy Constrained Applications

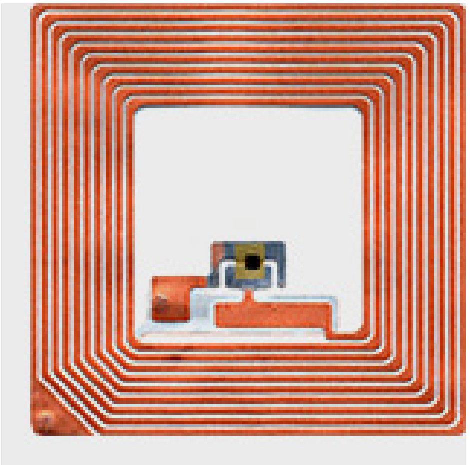
Micro-sensor networks



Medical devices

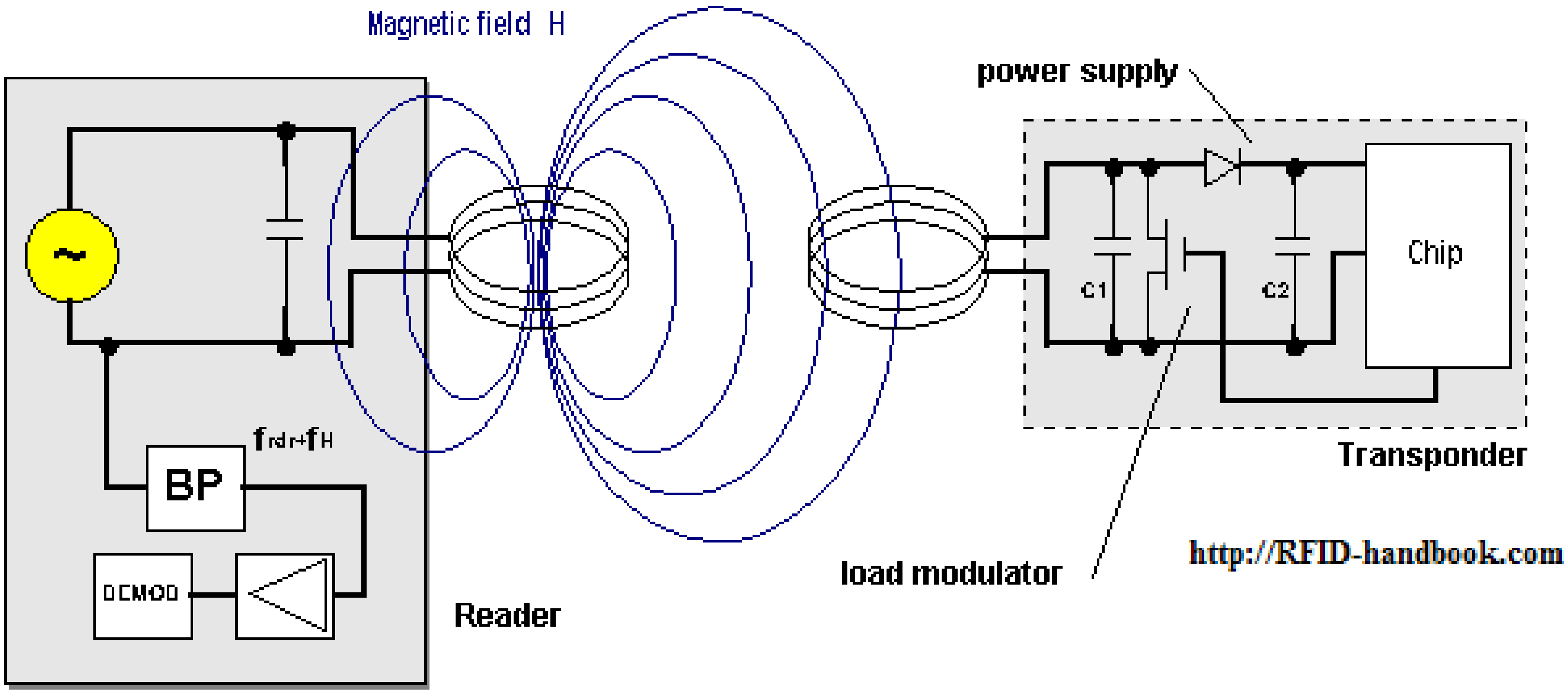
Target Tracking & Detection (Courtesy of ARL)

RFID Tags



Portable Electronics

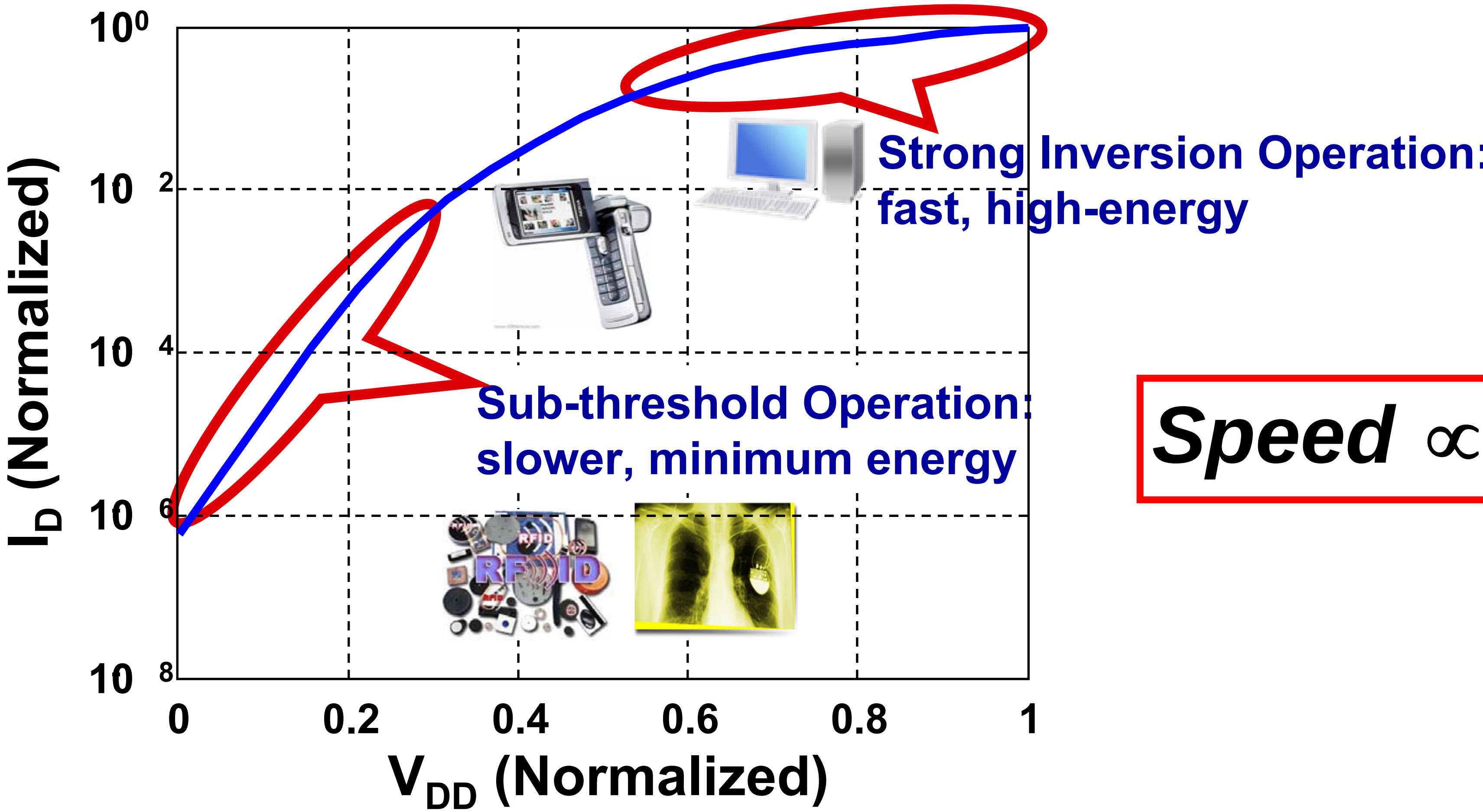
Inductive Link



- **Try to reduce power consumption to fit in energy budget**

Sub-threshold Operation

- Sub-threshold logic operates with $V_{DD} < V_T$
- Both *on* and *off* current are sub-threshold "leakage"

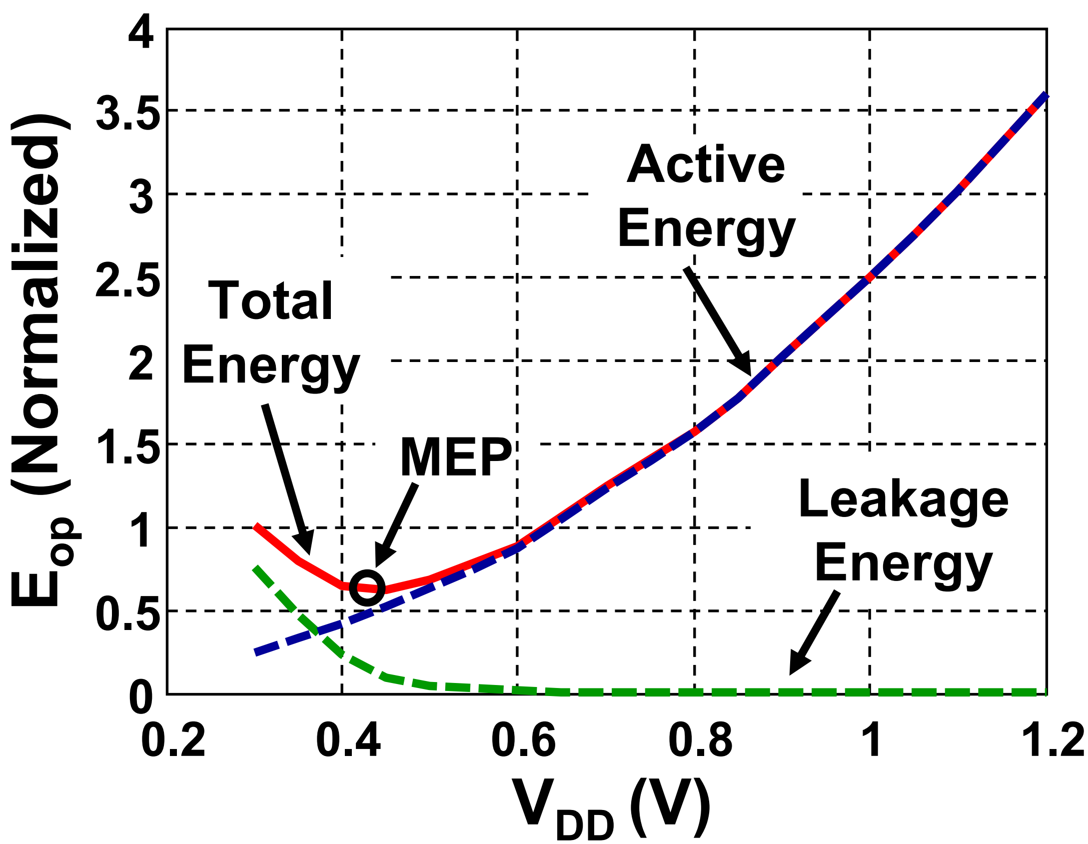


$$Speed \propto I_D$$

Minimum Energy Point (MEP)

$$E_{TOTAL} = E_{ACTIVE} + E_{LEAKAGE}$$

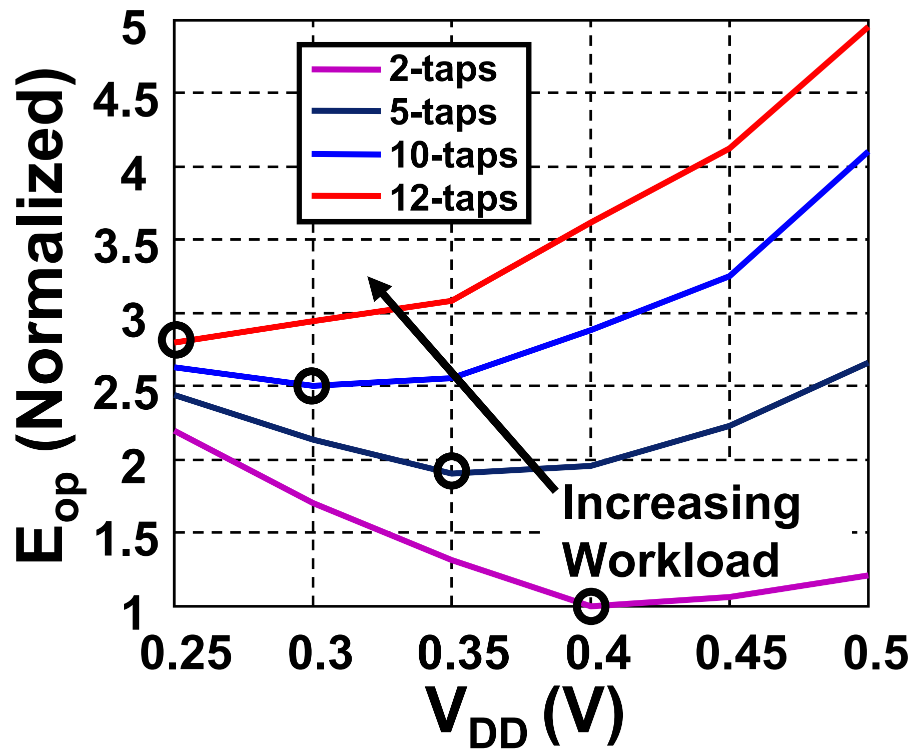
$$= CV_{DD}^{2} + I_{OFF}V_{D}T_{D} = V_{DD}^{2}\left(C_{eff} + L_{eff}e^{\frac{-V_{DD}}{nV_{th}}}\right)$$



65nm simulation for 7-tap FIR filter showing minimum energy operation

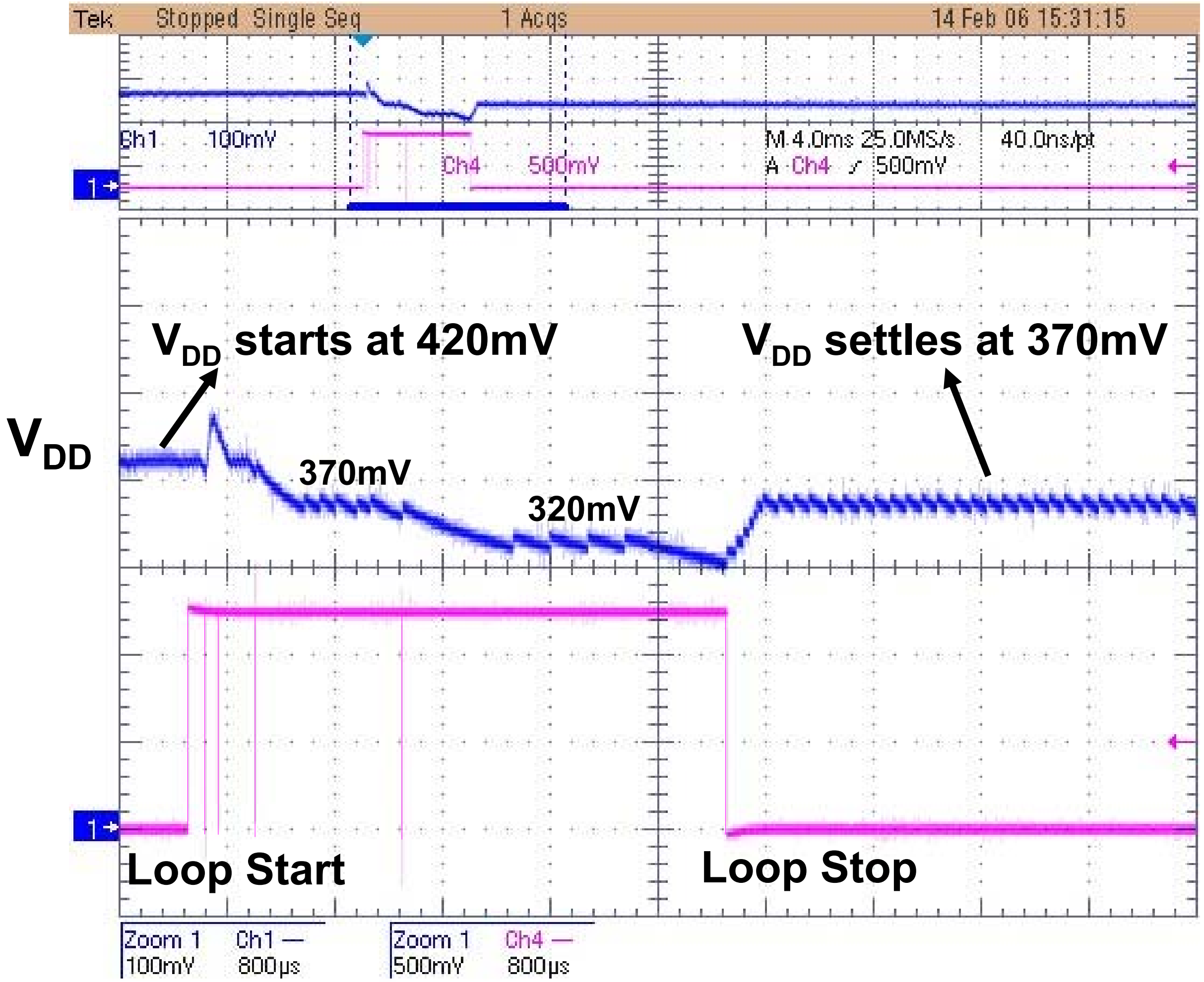
Motivation – Minimum Energy Tracking

Workload, Activity ↑	E_{ACTIVE} ↑	V_{MEP} ↓
Temperature, Duration of Leakage ↑	$E_{LEAKAGE}$ ↑	V_{MEP} ↑

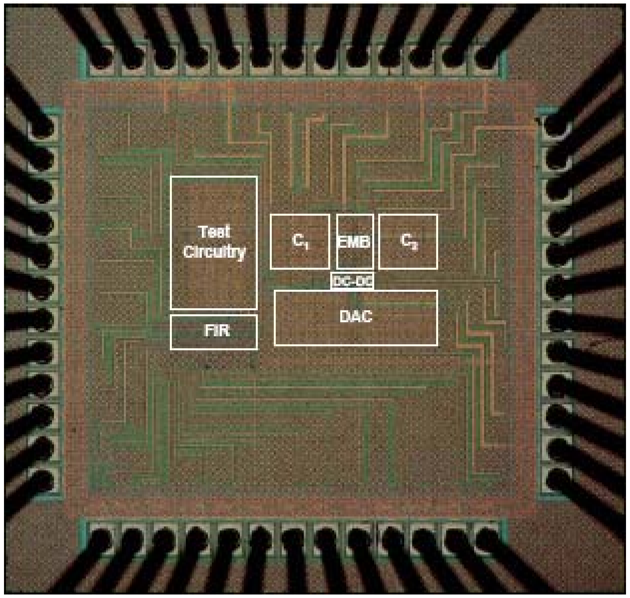


- Minimum Energy Point (MEP) varies with workload and temperature
- MEP moves when ratio of active to leakage energy changes
- Tracking the MEP : **0.5X – 1.5X** energy savings

Operation of the Energy Minimizing Loop



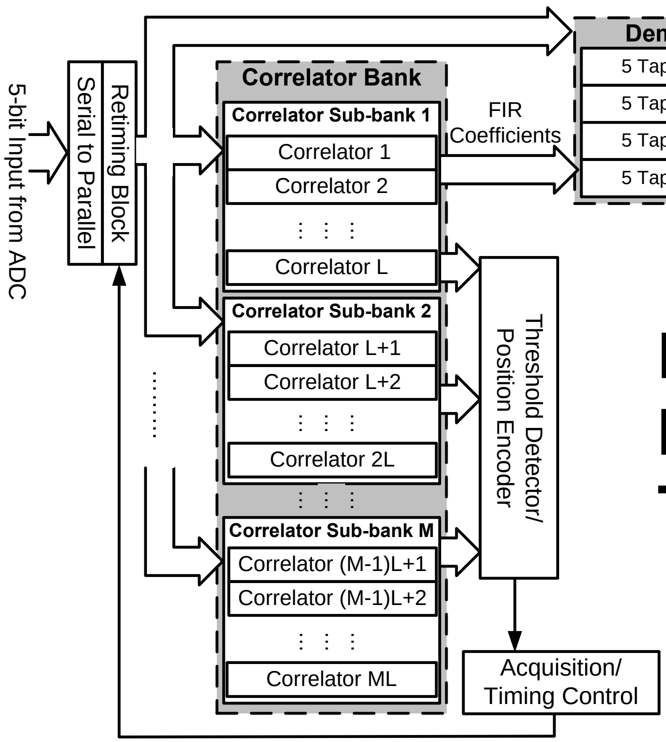
Y. Ramadass



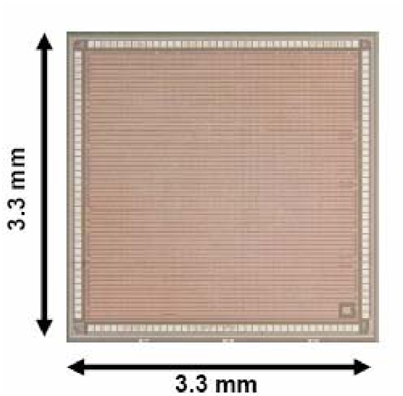
Parallelism

- Reduce Voltage → Slower Operation
- Parallel banks → Recover Performance
- Low power, with good performance (best of both worlds)

400mV 100Mbps baseband processor



L = 20
M = 31
Total # of correlators = 620



V. Sze

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- **Challenges with Low voltage operation**
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A Typical System

Extreme Voltage Scaling:
Sub-threshold Operation

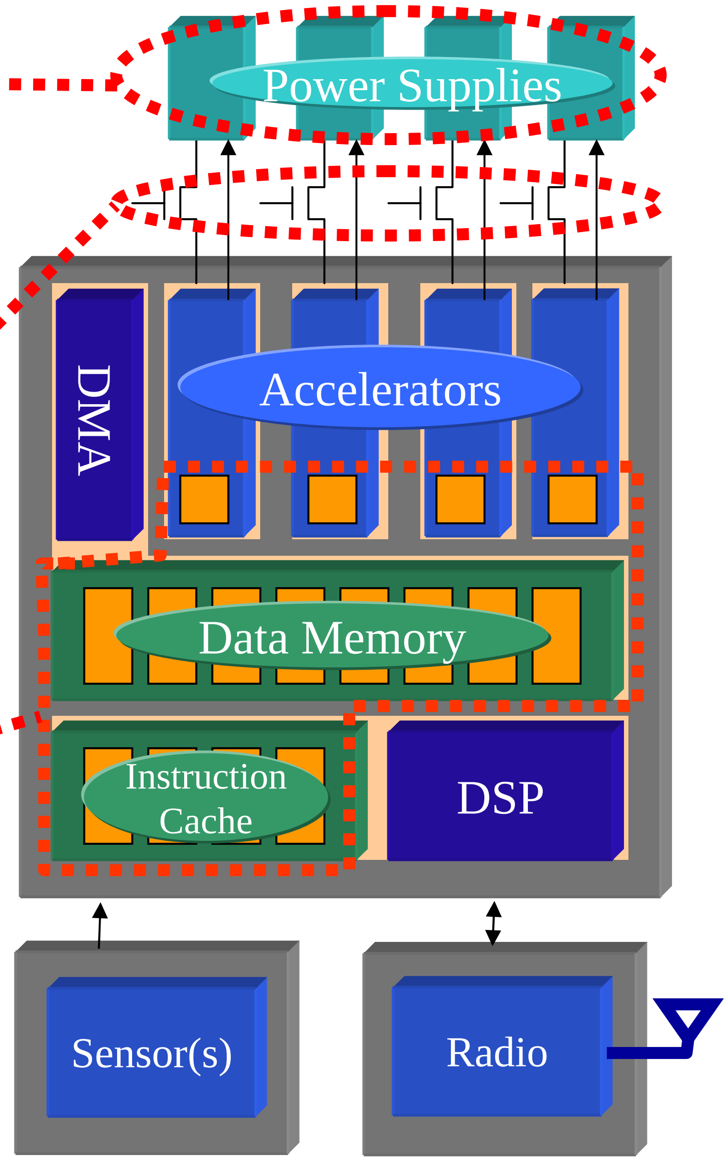
Modeling and Theory

$$E_{Total} = C_{eff} V_{DD}^2 + W_{eff} L_{DP} K C_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}$$

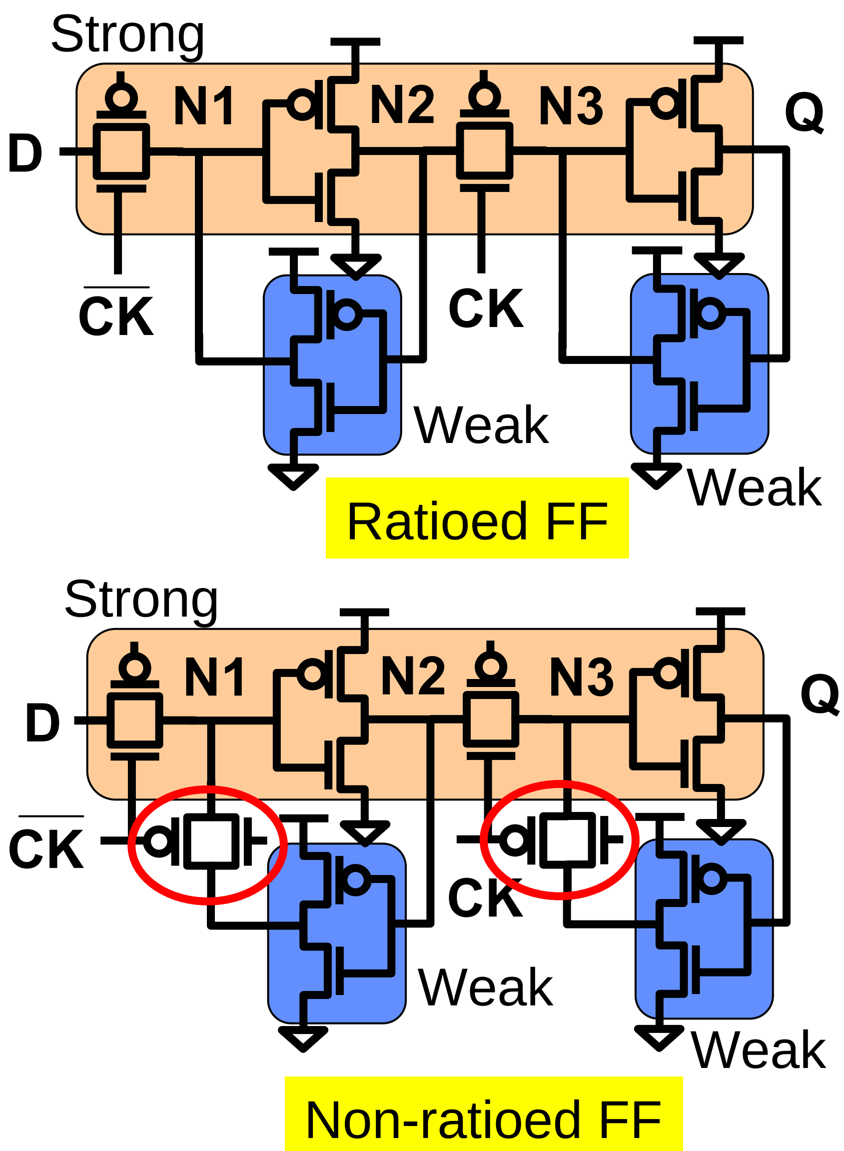
Standby Power Reduction
- Fine-grained power down
- Standby voltage scaling

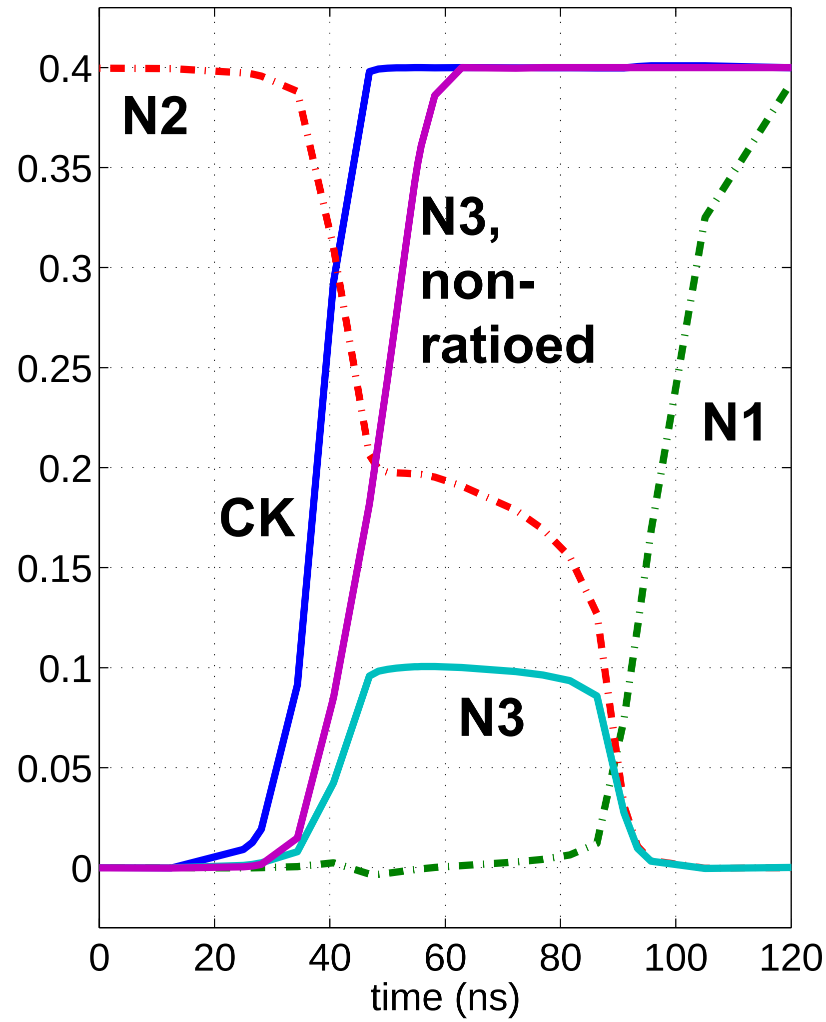
Sub-V_T Memory

Ultra-Dynamic Voltage Scaling



Challenges with sub-threshold logic



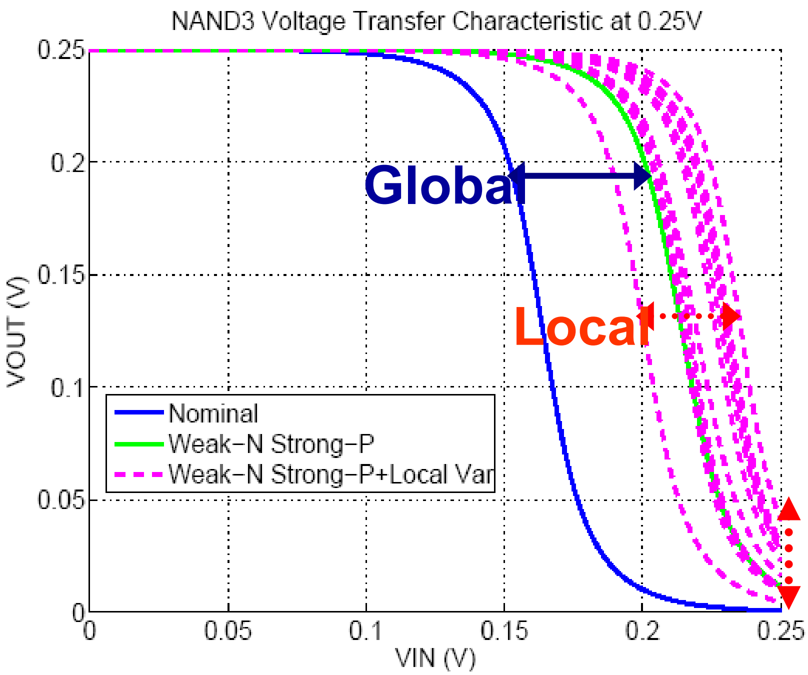


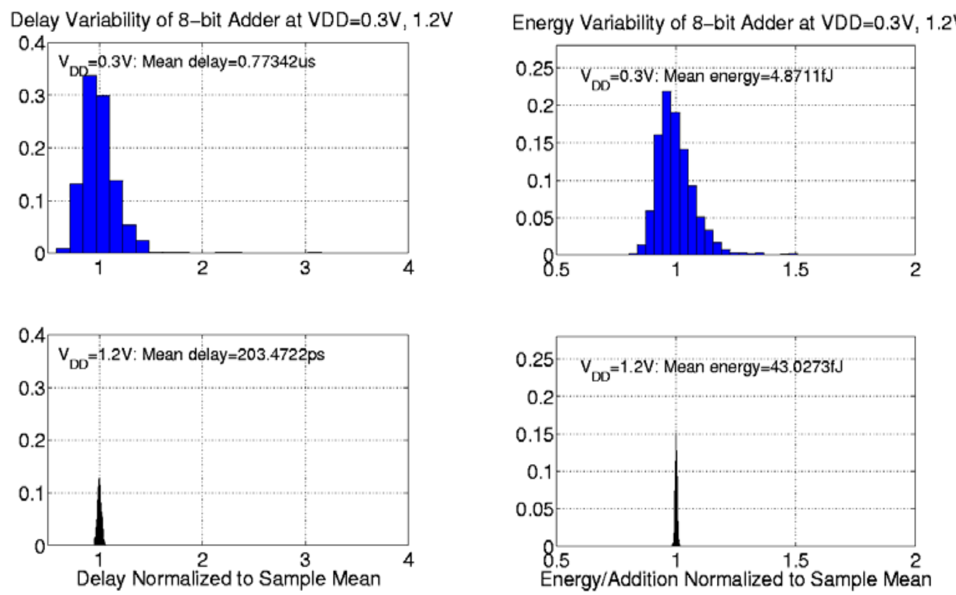
Ratioed FF fails to write a 1 at strong N, weak P corner at 400mV

Challenges with sub-threshold logic

Order of Magnitude Higher Variability in Sub-V_T

Functionality | **Performance**

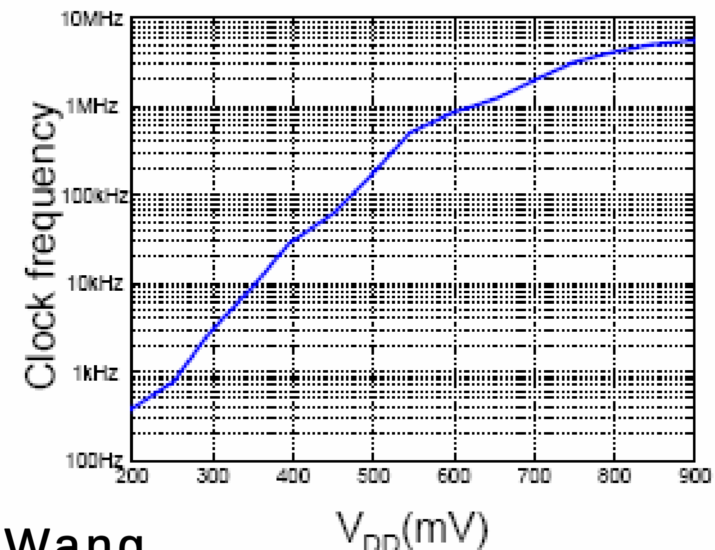


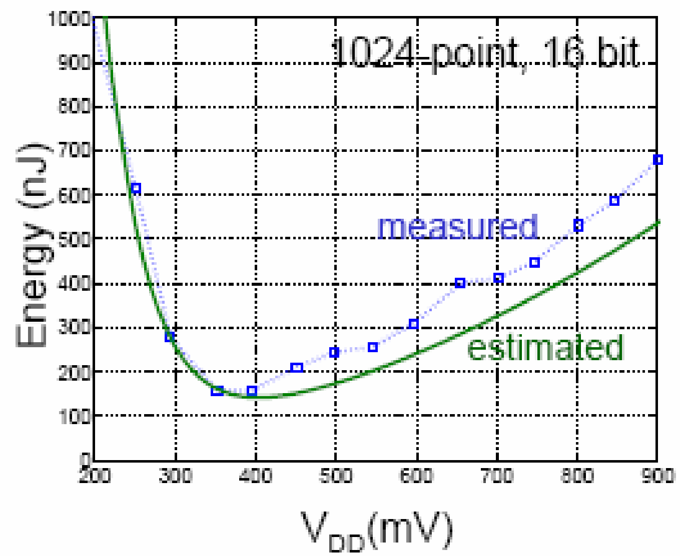


J.Kwong

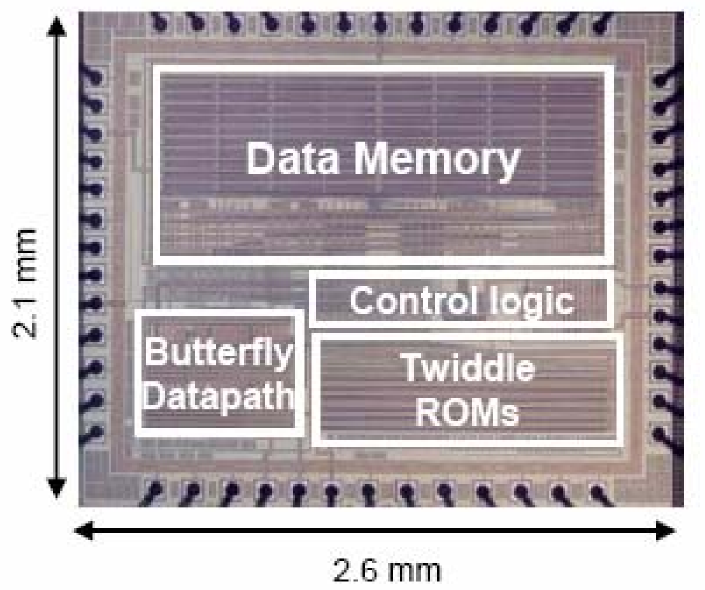
- **Local V_T variation → large spread in voltage swing, delay, energy**
  - **Errors due to degraded noise margins and timing violations**
- **Variation-tolerant circuits (e.g. asynchronous logic, soft error correction)**

A 180mV FFT Processor





A. Wang



- **FFT – Fast Fourier Transform**
- **Operates down to 180mV!!!**
- **5X savings in energy at the minimum energy point**

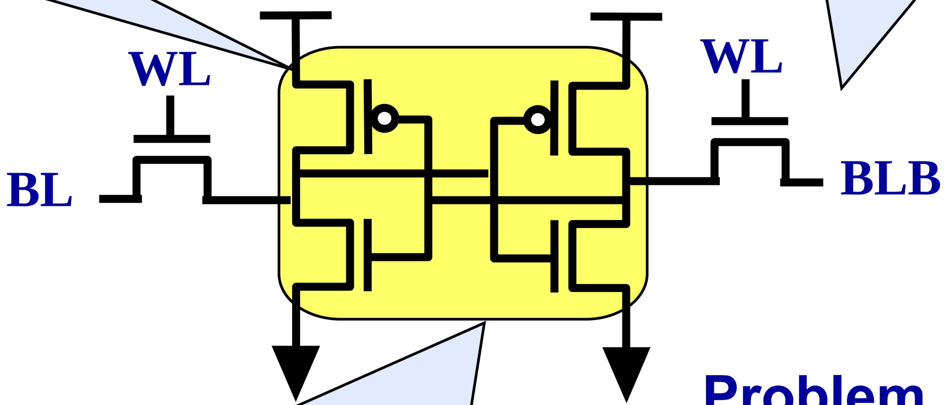
SRAM Challenges

Problem #1

Feedback too strong:
Cannot write new data!!

Problem 2

Bitline leakage impacts read value:
Cannot read correctly!!

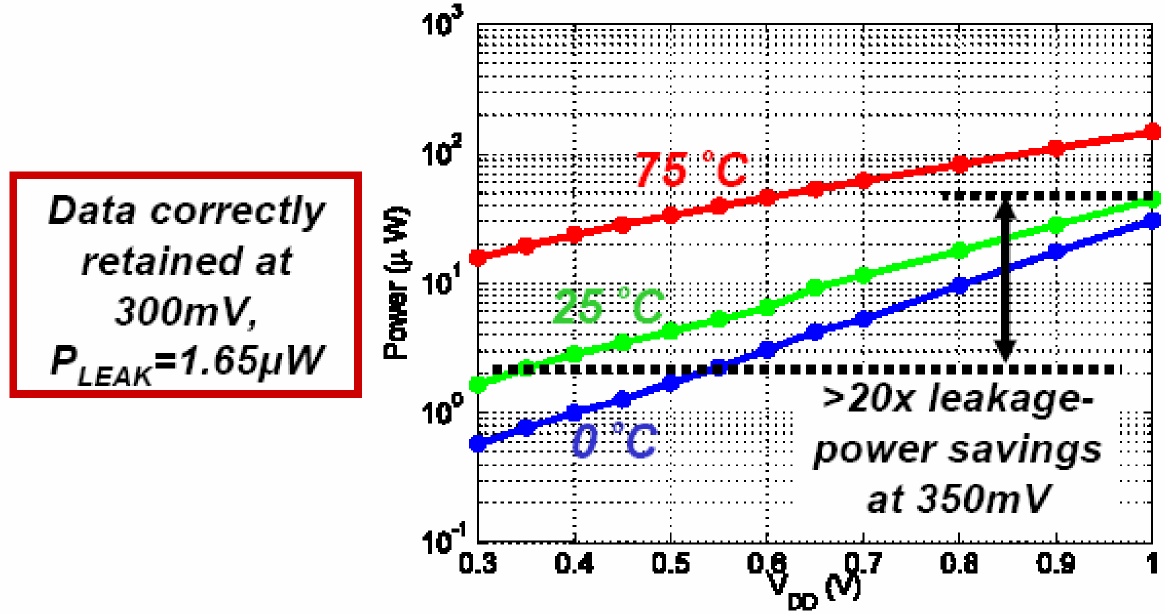


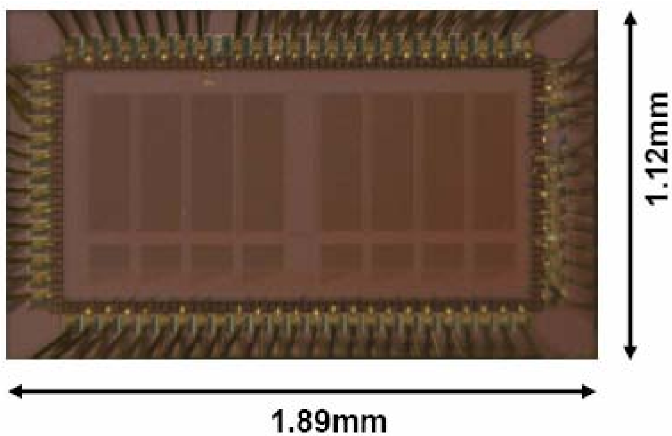
Problem 3

Static Noise Margin (SNM) degraded by variation:
Cannot hold data during read!!

- **Lowest previous demonstrated SRAM in 65nm is 0.7V**

Sub-threshold SRAM design





N. Verma

- **8-transistor SRAM cell**
- **Operates down to 350mV!!!**
- **20X leakage power savings**

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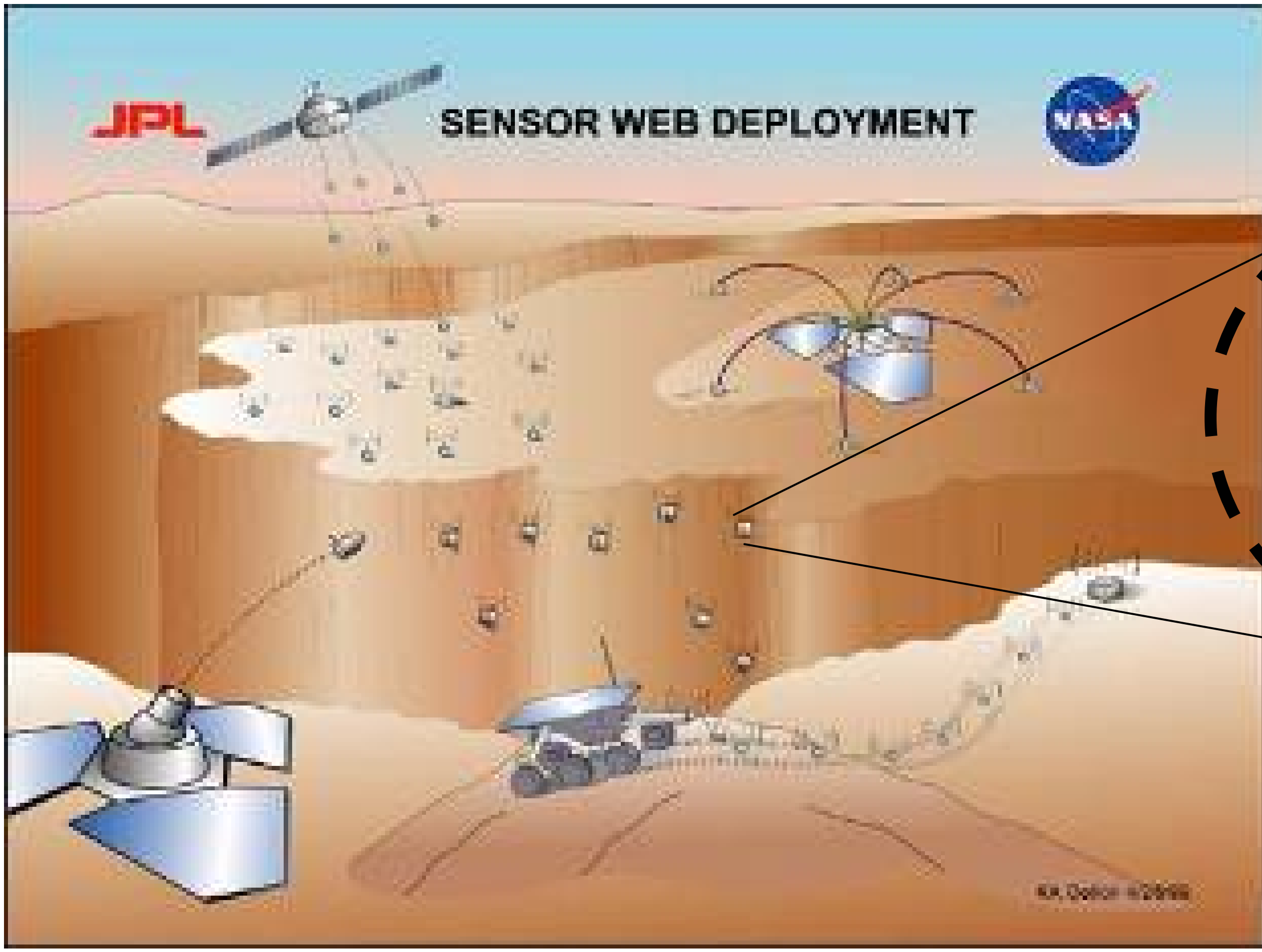
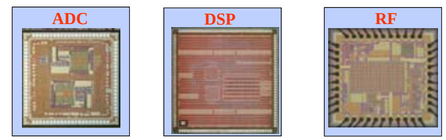
Wireless Sensor Networks





ADC
- Scalable rate (0-100KS/s) and precision (12b & 8b)
- **25mW at 100kS/s**

[N. Verma]

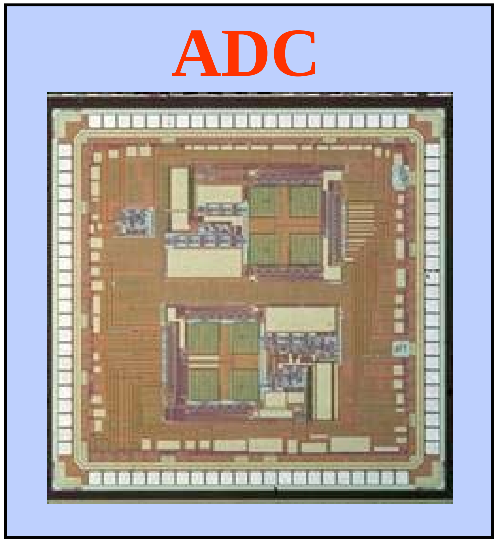
Sensor DSP
- 16-bit DSP with FFT (128-1024 points)
- **10pJ/instuction**

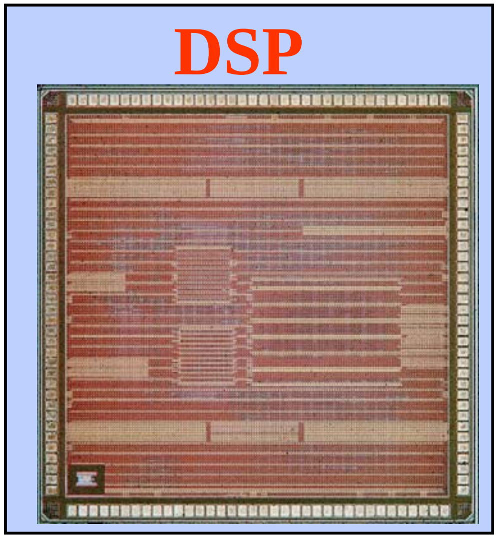
[D. Finchelstein and N. Ickes]

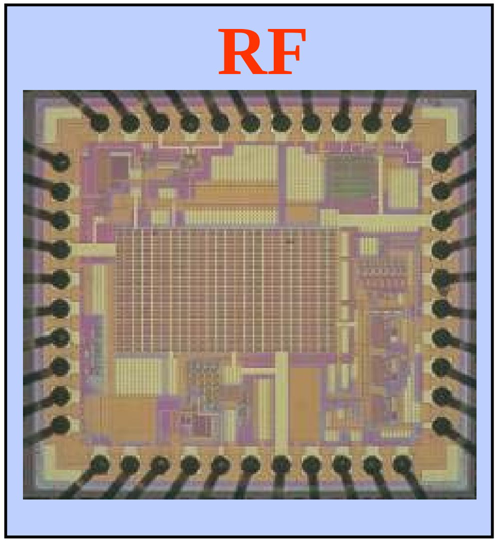
Low-Rate RF
- On-Off Keying using a rectification based receiver
- **Rx Energy: 1-3 nJ/bit**

[D. Daly]

Wireless Sensor Networks







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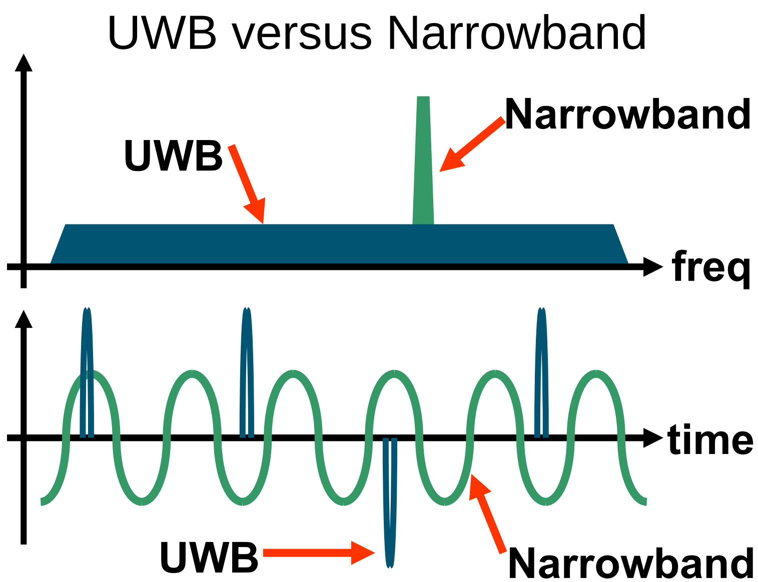
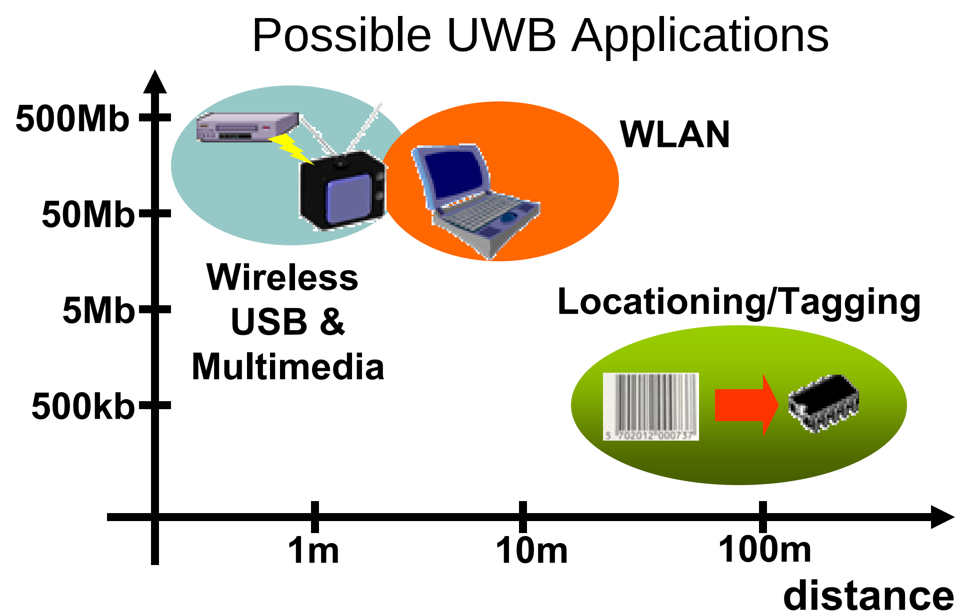
[D. Daly]

Ultra-wideband (UWB) Radio

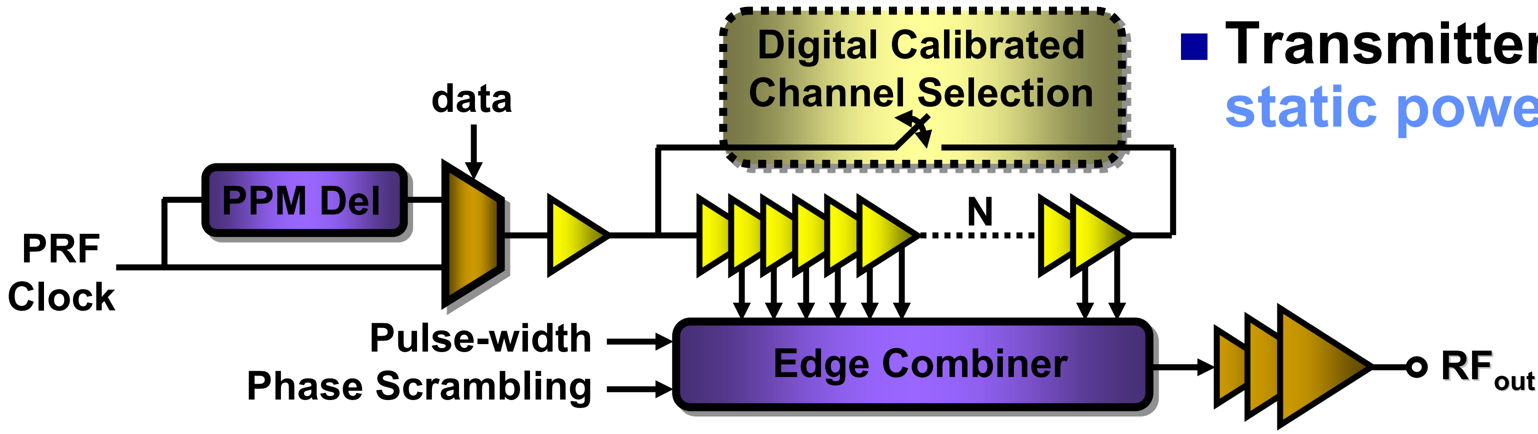




- **Advantages of UWB communications include**
  - **High Data Rate**
  - **Low Interference**
- **Integrate UWB radios on battery operated devices**
- **<u>Need an energy efficient UWB System</u>**

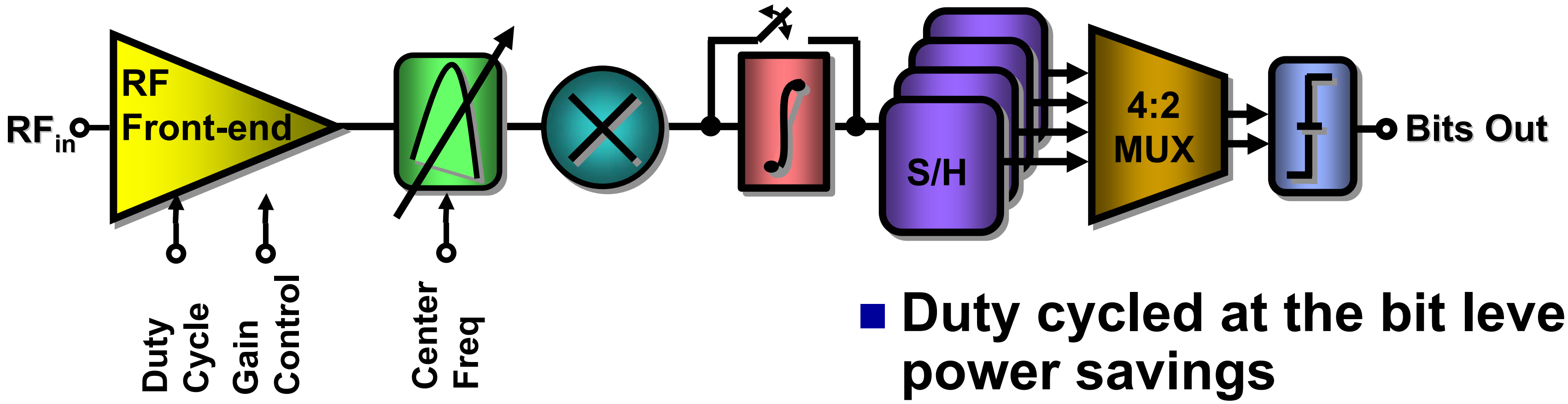
Ultra-low-Power Low Rate UWB

Transmitter



- Transmitter uses **no static power**

Receiver

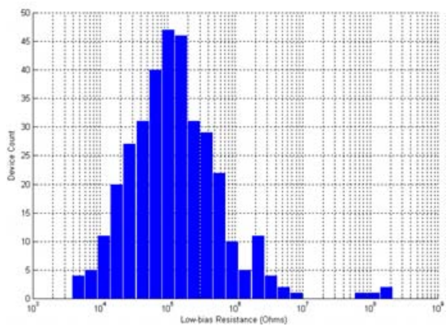


- Duty cycled at the bit level for power savings

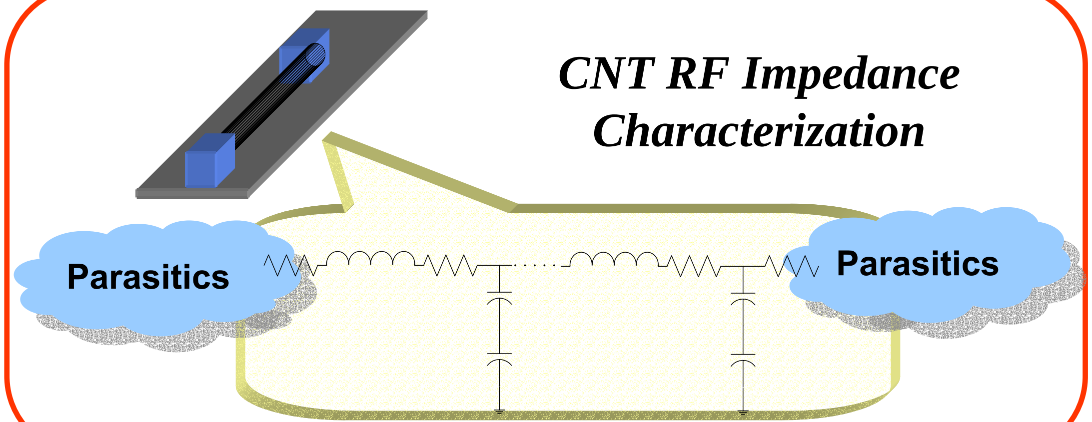
D. Wentzloff and F. Lee

Hybrid CMOS/Carbon Nanotube Systems

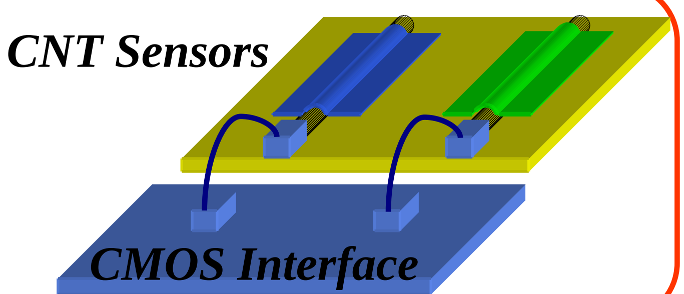
Carbon Nanotube Characterization



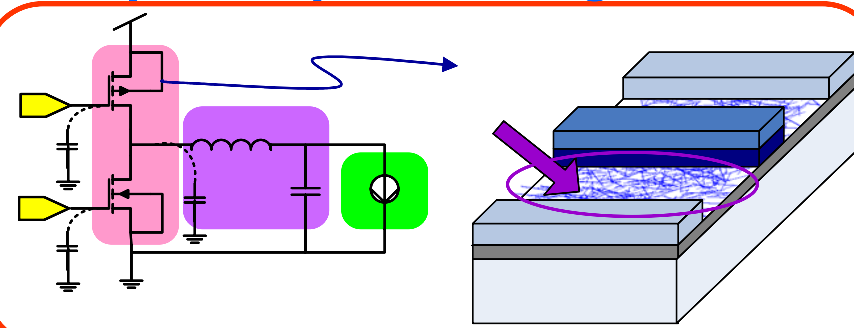
CNT DC Impedance Characterization



Carbon Nanotube – CMOS Hybrid System Design



Chemical Sensor System

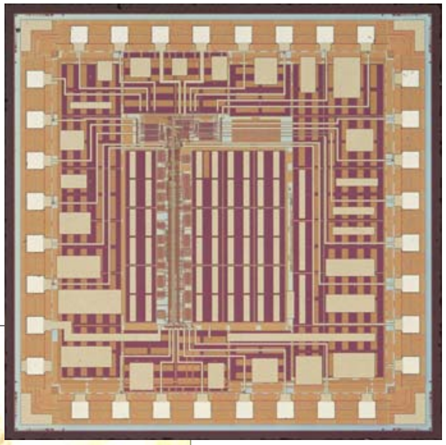


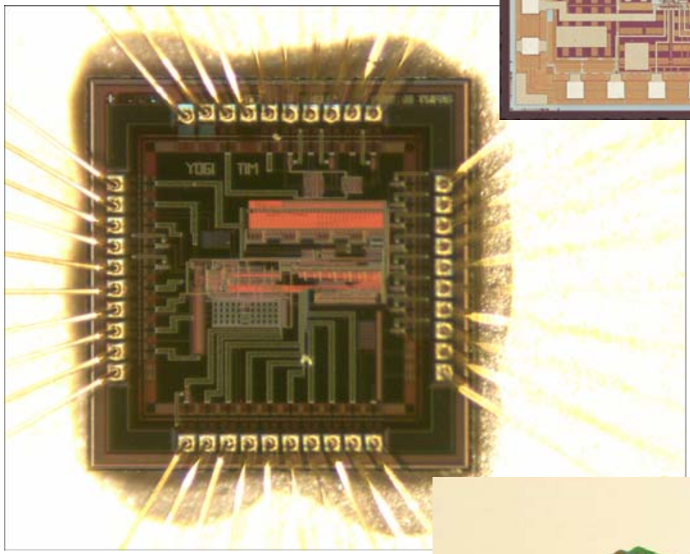
CNT Power Transistor Design

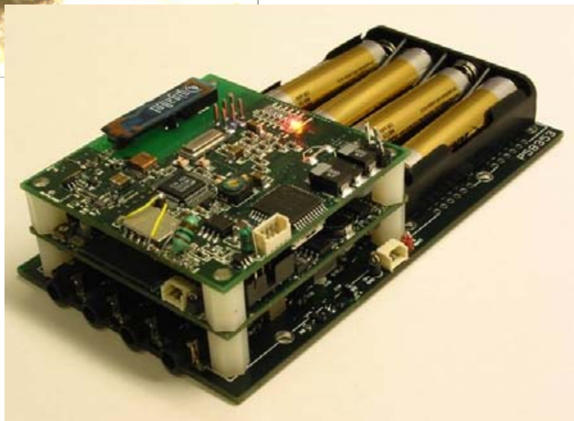
T. Cho, K. Lee, T. Pan (Prof. J. Kong)

Chip Design Flow

- **Specifications**
- **Design (4-5 months)**
  - **Cadence**
  - **Verilog (Synopsys tools, Astro…)**
  - **Spice**
- **Layout (1-2 months)**
- **Long Wait…(3-6 months, Prof. asks you to start next design)**
- **Chip comes back**
  - **Package**
  - **PCB (test board)**
  - **Test**
- **Write paper (hopefully the chip has worked)**

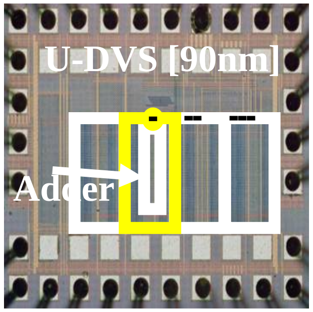




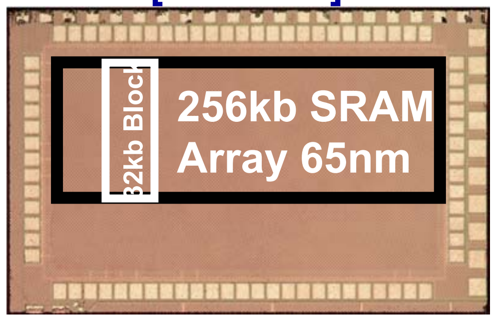


Sub-Threshold ICs

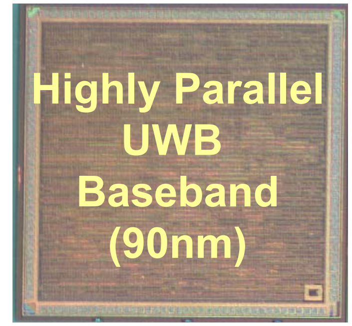
[ISSCC05]



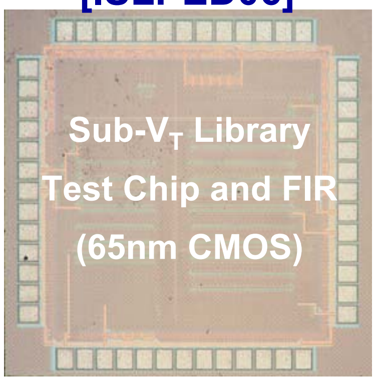
[ISSCC06]



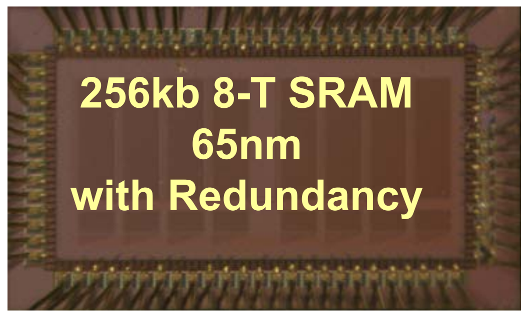
[ICASSP06 and ISSCC07]



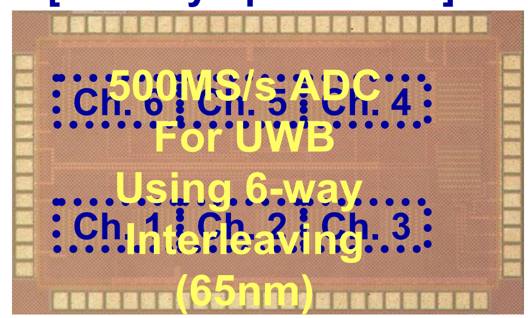
[ISLPED06]



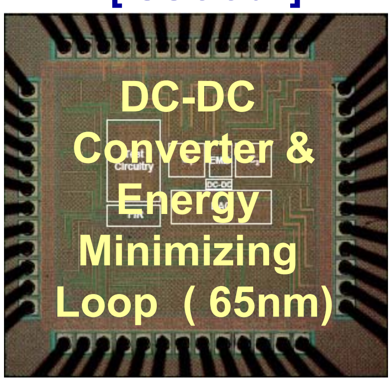
[ISSCC07]



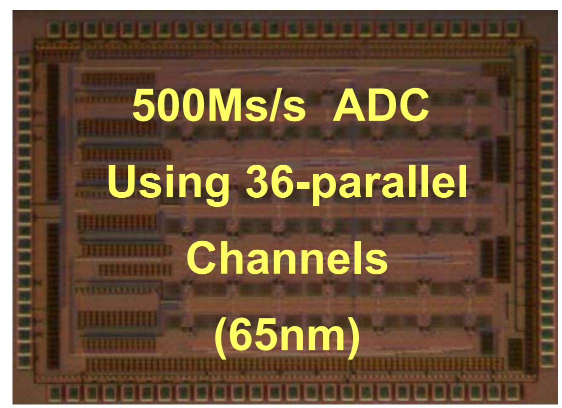
[VLSI Symposium 06]



[ISSCC07]



[PESC07]



Helpful Classes

- **Circuits – 6.002, 6.301, 6.374, 6.376, 6.775, 6.776, 6.334**
- **Devices – 6.012, 6.728, 6.730, 6.774**
- **Control Theory – 6.302, 6.331**
- **Signal/Image Processing – 6.003, 6.341, 6.344**
- **Communication – 6.450, 6.451**

Groups at MIT

- **Circuit Design**
  - **Prof. Anantha Chandrakasan**
  - **Prof. Joel Dawson**
  - **Prof. Hae-Seung Lee**
  - **Prof. David Perreault**
  - **Prof. Michael Perrott**
  - **Prof. Rahul Sarpeshkar**
  - **Prof. Charles Sodini**
  - **Prof. Vladimir Stojanovic**

A Sample of Microelectronics Companies

- **Intel**
- **Texas Instruments**
- **IBM**
- **Analog Devices**
- **National Semiconductor**
- **Infineon**
- **Philips**
- **ST Microelectronics**

Conclusions

- Low Power Operation is crucial for continued success of portable electronics
- Lots of new circuit design challenges ahead
- Energy scavenged electronics has a huge potential
- Exciting field to work on, direct relevance to industry