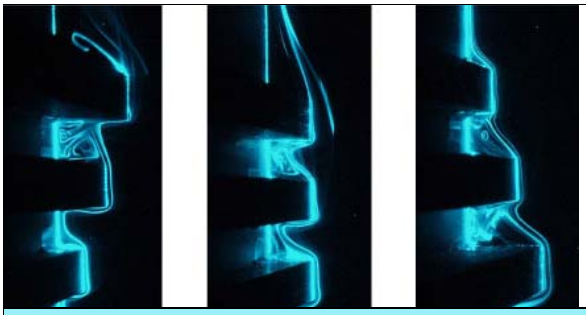

Electronic Cooling/Packaging Seminar Series

Dr. David Copeland
Thermal Engineering
Sun Microsystems

David Copeland works in Packaging Technology in Sun's Microelectronics Group, developing packaging and cooling technology for UltraSPARC processors and the systems which use them. Areas of development include thermal interfaces, heat spreading materials, single-phase and phase-change liquids, and data center cooling. He received his BS from Massachusetts Institute of Technology, MS from Stanford University and DrEng from Tokyo Institute of Technology, all in Mechanical Engineering. Before coming to Sun in 2005, he worked in packaging and cooling at IBM, Hitachi and Fujitsu, and in heatsink development and design at Intricast, Sumitomo and Showa Aluminum. David belongs to ASME, IEEE and IMAPS, and is a frequent participant at conferences on electronics cooling.

Nonuniform and Temperature-Dependent Power in Microprocessors

Recent developments in microprocessors have resulted in as many as eight processor cores, soon to be followed by sixteen. These cores have average power dissipation twice that of chip average, and some regions of the chip have power density below 3% of the average. This results in a higher package thermal resistance than that of a uniformly powered chip, with the ratio of nonuniform to uniform thermal resistance strongly dependent on packaging and cooling technology. Leakage current, once a negligible component of power dissipation, has increased as lithography technology has progressed through 90, 65 and 45 nanometers and should continue through 32 and 22 nm. The reduction in chip power per degree will soon be 1% and will increase in the future. Such power reduction justifies advanced cooling solutions in terms of not only energy minimization, but in some cases also in terms of total packaging and cooling cost.

Date: December 7

Rm: 1-390 at 11am

Hosted by: ME MLK Visiting Prof. Agonafer

MIT Department of Mechanical Engineering