EECS311, Fall 2002

Laboratory Report #6:
Multi-Stage Amplifier Design Project
Due: Wed 12/11/02

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I have neither given nor received aid on this homework, nor have I concealed any violations of the honor code.

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Index

Introduction

The purpose of this project is to design, build and test a multi-stage amplifier circuit that might be used for audio amplification. Audio equipment is one of the most important uses of analog circuit design.

The design has to meet several specifications that a real audio amplifier might be required to have. Its frequency response should be limited to what is audible to the human ear (50Hz-23kHz), must have a gain of 3500, power consumption should be less than 300mW while providing an output of 2V peak-to-peak, input impedance should be at least 100kΩ and the output impedance should be less than 25Ω.

As we have seen in the previous project, performances of single stage amplifiers are severely limited and real life applications almost always require multi-stage designs. For this design a three-stage layout using four NPN type 2N2904 transistors were used, using same transistors makes design calculations a little easier and reduces the number of steps required for solid state integrated circuit production.

The first stage is a Darlington pair that provides very high input impedance and most of the voltage gain. Second stage is a single transistor used in common emitter with degeneracy configuration, it provides some gain and gives us the high cut-off frequency we need. The third and final stage is an emitter follower to provide low output impedance, so our circuit can provide a lot of current to the load.

Since we were concerned only with the small signal response, both the input and output are AC coupled. Another coupling capacitor used between the first and second stages so we can have both stages at the desired biasing points without worrying about the other.

Design Strategy

Design Order

There are multiple difficulties inherent in this design that made the design process difficult to carry out in a completely linear fashion. With only five capacitors to use, some stages need to be DC coupled, so DC bias design cannot be completely separated into stages. Also, the amplification of each stage depends on the input and output resistances of the preceding and following stages, so the AC analysis is difficult to separate. The work required to derive a transfer equation for the entire four-transistor amplifier by hand is rather large. Therefore, we chose to follow a non-linear design approach similar to the one suggested in the lab manual where we use Accusim simultaneously with hand design to verify and check our results and equations. Using this method, we setup our DC bias equations by hand and then checked if they were valid in Accusim. Next we could hand design for gain and return to Accusim to check the validity of our gain equations. Using this segmented design strategy, we were sure that our hand design calculations were valid.

Initial Design

For our first design, we chose to follow the architecture suggested in the lab manual and to use DC coupling between all stages. The architecture recommended was: emitter follower, common emitter, common emitter with degeneracy, and emitter follower. Although DC

coupling makes the bias point selection more difficult, it does reduce the number of components needed by using only one resistor bias ladder. By eliminating extra bias ladders, we also can theoretically increase gain, as signal would normally be attenuated in these chains. DC coupling also allows us to use the five capacitors wherever we need elsewhere in the circuit, such as for bypass and input/output coupling.
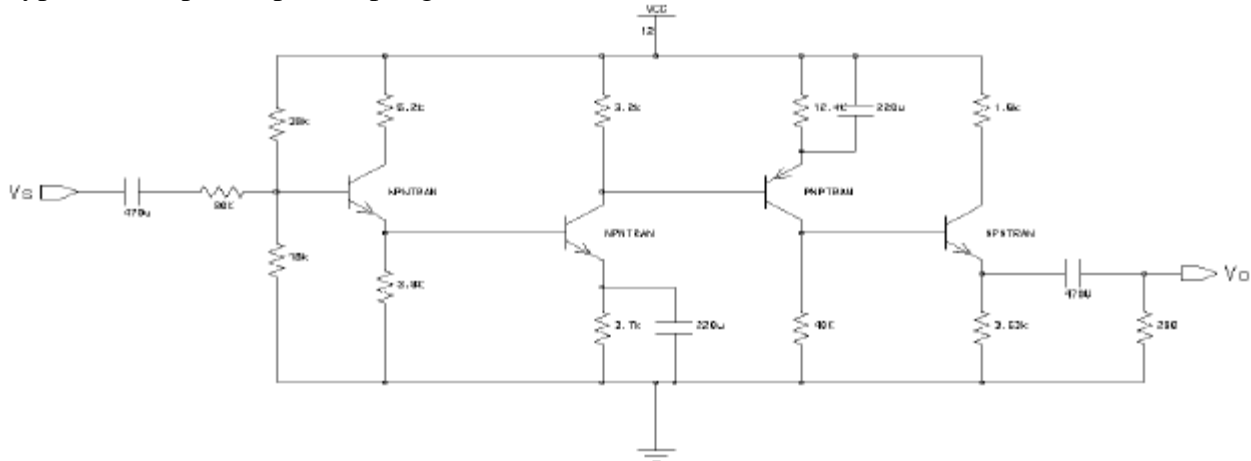
Design Trial 1

Because the DC and AC parameters are linked across the stages, we found it advantageous to use a computer spreadsheet program (Microsoft Excel) to help us select resistor values. We could then easily change one single value and have it propagate through all the equations saving hours of manual hand calculations. We also wrote the spreadsheet to easily calculate the small signal parameters (g_m, r_p, r_o) for each transistor as well.

In the first trial, the required bias ladder on the input pulled the input resistance low, so a series input resistor was added. Although this simplified meeting the input resistance specification, it severely attenuated the signal, so we eliminated the use of emitter degeneracy on the third stage. Other problems we had included very high output resistance, and some significant sensitivity to current gain parameters of the transistors.

Alternate Architecture – The Darlington Pair

What we really wanted to do was to simplify the analysis by separating the sections with a coupling capacitor. The ideal place to break the amplifier up is between the second and third stages (the amplification stages) because the gains of these two stages are closely tied to the DC bias conditions. The first stage existed only to provide a high input resistance mainly through emitter resistance multiplication. However, the collector current and therefore base current had to be small in order to meet the conflicting requirements for beta insensitivity and high bias resistance. This was especially important because we didn't want to use and input series resistance to artificially increase R_{IN}. If I_{C1} decreases and R_{E1} increases significantly, the problems with input resistance and losing signal are eliminated in the first stage but the output resistance is driven abnormally high and the base current of the second stage cannot be maintained.

However, if the emitter of the first stage is connected directly to the base of the second stage, this eliminates the problems with output resistance and DC bias point. If we finally connect the two collectors together, we have created a Darlington pair. A Darlington pair can be treated as one transistor with a current gain that is the product of the current gains of two

transistors. The composite small signal parameters are also easy to derive. By using the Darlington pair as a composite first stage in the amplifier, the total number of stages is reduced to three. The because of the extremely high effective current gain of the pair, a nominal collector current can require only a very small base current and therefore a high resistance bias ladder. Furthermore, with the arrangement yields a very high input impedance because the emitter multiplication factor is applied twice. Even with no emitter degeneracy the r_{p2} resistance is still multiplied by Q_1 and with I_{C1} so small, r_{p1} is very high. Therefore, the composite stage is operated as a common emitter amplifier with extremely high input resistance.
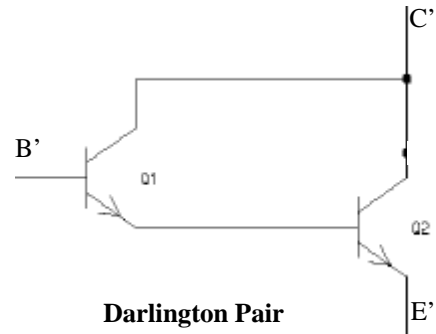

Darlington Pair

With the bias constraints of the first stage removed from the rest of the circuit, we focused on the final gain and output stages (2 & 3). It seemed that in order to get maximum output swing and minimize output resistance, the collector resistor on the output emitter follower was unnecessary. We also chose to use all NPN transistors for consistency and because we no longer needed to worry about the DC bias point conditions between the two voltage amplifiers. By capacitively coupling the first and second stages, it was necessary to add a second bias ladder. However, we could use raw gain to overcome the loss in output signal due to the added loading on the first stage. Knowing we would probably have to reduce the gain slightly in the second stage, we included emitter degeneracy in the second stage using a split emitter resistor setup where $R_{E2}=R_{E2a}+R_{E2b}$. The final circuit diagram is on the following page.

Parameter Selections

With the new circuit architecture, the spreadsheet had to be rewritten, but it used basically the same techniques. Furthermore, we expanded the spreadsheet to include calculating the R_{IN}, R_{OUT} and A_V parameters of the amplifier. For the hand calculations and the simulations, we used current gain of 150 and 170 and an Early voltage of –171V. Because we are trying to design for reasonable bias stability and insensitivity to beta, it was felt that measuring beta for each transistor would be unnecessary if we designed our circuit correctly. We used a current gain of ß=170 for the transistor we reused from Lab 5 and ß=150 as an average of possible values for other transistors. The Early voltage is what we measured in Lab 5. The following table is a guide to pick values:

Parameter	Stage 1: CE	Stage 2: CE+D.	Stage 3: CC
Gain	~100	~40	~1
I_C	1mA	0.5mA	15mA
Input R	>1MO	>R_{OUT1}	>R_{OUT2}
Output Swing	50mV	~2V_{ppk}	2V_{ppk}

The circuit topology in the lab manual suggests using two gain stages with significantly different voltage gains. However, from our experience with Lab 5, making a common emitter amplifier with a very high or rather low gain is difficult because of the limitations of the circuit or the transistor. We felt it was better to aim for gains that were more middle-of-the-road. The collector current in the first stage was chosen to be a moderate value low enough to keep the bias ladder requirements low. The second stage has a low current for the same reason, to keep the
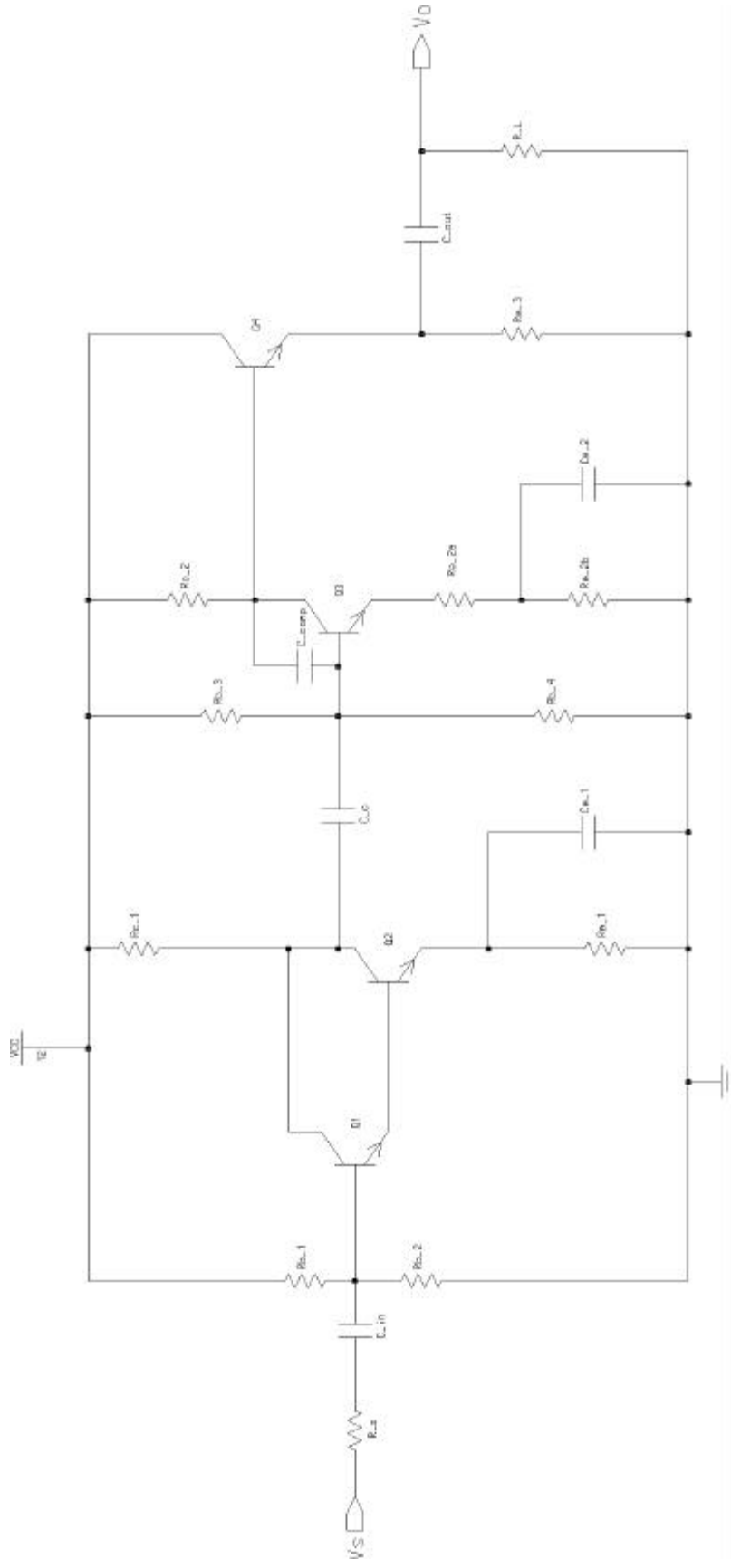
bias ladder resistance high. Stage 3 is only an emitter follower with a gain slightly less than one. Therefore, the $2V_{ppk}$ output voltage swing must be developed by stage 2. In order to meet the low output resistance and be able to drive a high capacitance load, the current in the last stage is relatively high and accounts for 90% of the power supply current draw. In order not to lose too much of our signal from impedance mismatch, we chose the input resistance of each stage to be greater than or equal to the output resistance of the preceding stage.

Also of concern to the design are the collector to emitter and the emitter voltages. We found in Lab 5 that having an emitter voltage between about 1.6V to 2V was a good range for reducing sensitivity to changes in current gain. We also found from our hand calculations that the raw voltage gain of a common emitter amplifier was dependent on the voltage over the collector resistor, or therefore inversely proportional to V_{CE}. In Lab 5, we used a V_{CE} of 2V for a gain of 160. Therefore, we choose V_{CE2}~5V and V_{CE3}~6V as a starting point to look at for the two voltage amplifier stages. V_{CE2} has to be high anyway to keep Q_1 properly biased in the Darlington Pair

The AC Analysis of the three stage amplifier is much more complex than a single stage amplifier. For determining the upper and lower cutoff frequencies, the Open Circuit Time Constant and Short Circuit Time Constant methods could be used. However, these require pages and pages of calculations. A less rigorous approach may not be as accurate, but it will be faster to get to simulation. Then in simulation, any errors can be corrected.

For the high frequency cutoff frequency, we will assume that the compensation capacitor and $C_{\mu3}$ is the dominant pole. However, in simulation we saw that our first estimation of the cutoff frequency was about half of the simulated cutoff frequency so we reincorporated this factor into our hand calculation equation.   For the low frequency cutoff, we also used an estimation technique to meet the requirement. Instead of calculating the SCTC frequency, we tried to make the capacitive reactance at the maximum f_L much smaller than the approximate resistance seen by the capacitor. By doing this, we can guarantee meeting the specifications, even if it doesn't calculate the exact lower cutoff frequency.

The last step was to check our peak output voltage swing. In this case, our second stage with Q3 is going to be our limiting stage, so we need to make sure that v_{p3} does not go over $10mV_{pk}$. By using the resistance reflection rule and the voltage gain of this stage, we were able to calculate the peak output voltage.

$$V_{BB_1} = \frac{V_{cc} \cdot R_{b_2}}{R_{b_1} + R_{b_2}} \qquad\qquad V_{BB_1} - V_{E_1} \cong 1.4v \qquad\qquad \text{Darlington Arrangement}$$

$$R_{BB_1} = R_{b_1} \parallel R_{b_2} = \frac{R_{b_1} R_{b_2}}{R_{b_1} + R_{b_2}} \qquad \underset{\text{approximate}}{KVL} \quad V_{BB} - I_{B_1} R_{BB_1} - 1.4v - B_1 B_2 I_{B_1} R_{E_1} = 0$$

$$I_{B_1} = \frac{V_{BB_1} - 1.4v}{R_{BB_1} + R_1 B_2 R_E} > 0 \; ; \quad I_c' = I_{c_1} + I_{c_2} \cong B_1 B_2 I_{B_1}$$

$$V_{E_1} \cong I_e' R_{E_1} \qquad V_{c_1} = V_{cc} + V_{E_1} \qquad \frac{V_{cc} - V_{c_1}}{I_{c_1}} = R_{c_1}$$

$$g_{m_1}' = \frac{g_{m_2}}{2} = \frac{I_{c_2}}{2V_T} \cong 20 B_2 (B_1 + 1) I_{B_1}$$

$$r_{\pi}' = r_{\pi_1} + r_{\pi_2}(1 + B_1) = \frac{1}{40 I_{c_1}} + \frac{B+1}{40 I_{c_1}(B+1)} = \frac{1}{20 I_{B_1}}$$

$$r_0' = r_{0_2} = \frac{V_A + V_{CE}}{B_1 B_2 I_{B_1}} \cong \frac{V_A + V_{CE_2}}{I_c'} \cdot \frac{2}{3}$$

$$\left.\begin{array}{c}\\ \\ \\ \\ \\ \\ \end{array}\right\} \text{ small sig parameter for Darlington Pair}$$

$$V_{BB_2} = \frac{V_{cc} \cdot R_{b_4}}{R_{b_3} + R_{b_4}} \qquad R_{BB_2} = \frac{R_{b_3} R_{b_4}}{R_{b_3} + R_{b_4}} \qquad I_{B_2} = \frac{V_{BB_2} - 0.7}{R_{BB_2} + (1+B_3)R_{E_2}} \qquad I_{c_2} = B_2 I_{B_2}$$

$$V_{BB_2} - 0.7 \cong V_{E_2}, \qquad (1 + B_3) I_{B_2} \cdot R_{E_2} = V_E$$

$$\frac{I_{c_2}}{R_{c_2}} = V_{c_2} - V_{B_4} = V_{E_4} + 0.7$$

$$I_{e_{3E_{\cong 4}}} = \frac{V_{E_{e4}}}{R_{e_3}}$$

$$g_{m_3} = 40 I_{e_3} \qquad r_{\pi_3} = \frac{B_3}{I_{e_3}} \qquad r_{0_3} = \frac{V_A + V_{CE_3}}{I_{c_3}}$$

$$g_{m_4} = 40 I_{c_4} \qquad r_{\pi_4} = \frac{B_4}{I_{c_4}} \qquad r_{0_4} = \frac{V_A + V_{CE_4}}{I_{c_4}}$$

$$r_{e_4} = \frac{1}{g_{m_4}} \quad \longrightarrow \quad R_{OUT} = R_{E_4} \parallel \left(r_{e_4} + \frac{R_{out_3}}{B+1} \right)$$

$$\left.\begin{array}{c}\\ \\ \\ \\ \end{array}\right\} \text{ small sig para for Q3 \& Q4}$$

$$I_{BAS_1} = \frac{V_{cc}}{R_{b_1} + R_{b_2}} \qquad I_{BAS_2} = \frac{V_{cc}}{R_{b_3} + R_{b_4}}$$

$$I_{PWR} = I_e' + I_{c_3} + I_{c_4} + I_{BAS_1} + I_{BAS_2}$$

$$R_{in} = R_{BB_1} \parallel R_{in_1}^{a_2} = R_{BB_1} \parallel r_{\pi}'$$

$$R_{OUT} = \frac{1}{g_{m_4}} + \frac{R_{4(input)}}{B_4 + 1}$$

Lab 6: Bias Point Matrix *FINAL ITERATION W/ DARLINGTON PAIR*

Q-Point Choices		Bias Points		Small Sig Params		Amplifier Params	

Vcc:	12 V
R_Load	200 O
R_source	4.00E+03 O

Q' (Q1 & Q2)   **NPN - CE Darlington Stage**   For Voltage gain and high input impedance

Beta 1:	174	V_BB1~	3.2			Vth:	9.90E-01	**GAIN**	3.79E+03
V_A1:	171	R_B1~	1.46E+06	gm':	0.020115	Rth:	3.96E+03	**R_IN**	3.10E+05
Beta 2:	174	R_B2~	5.32E+05	r_pi'	1.51E+06			**R_OUT**	48.45
V_A2:	171	I_Bias1:	6.02E-06	r_o'	1.17E+05	RL2':	3.53E+03 ro2//RC1//RBB2/RIN3		
		I_B1~	3.303E-08					**I_PWR**	1.55E-02
V_CE2:	5 V	R_E1~	1.80E+03			RIN'	1.51E+06		
I_C2:	1.00E-03 A	R_C1~	5.20E+03			ROUT'	4.98E+03	**V_OPPK**	-2.06E+00
R_BB1:	3.90E+05 O					AVth'	-7.10E+01		
V_E':	1.8 V								

Q3:   **NPN - CE with possible deger** For Voltage Gain and DC bias for Q4

Beta 3:	150	V_BB2~	2.5					
V_A3:	171	R_B3~	2.47E+05	gm3:	1.80E-02	RL2':	5.71E+03 ro3//RC2//RIN4	
		R_B4~	6.51E+04	r_pi3:	8.33E+03	Rth2':	4.54E+03 ROUT2//RBB2	
V_CE3:	xxxxxxxx	I_Bias2:	3.84E-05	r_o3:	3.94E+05			
I_C3:	4.50E-04 A	I_B3~	3.00E-06			RIN2:	1.59E+04	
V_E3:	1.62 V	R_E2~	3.60E+03			AVth2:	-5.41E+01	
R_BB2:	5.15E+04 O	R_E2a:	5.00E+01 pick to decrease gain			ROUT2:	7.83E+03	

Q4:   **NPN - CC**   For driving output

Beta 4:	150	R_E3:	5.00E+02			RL3':	1.41E+02 ro4//R_L//RE4
V_A4:	171	V_CE4:	5	gm4:	5.60E-01	Rth3':	7.83E+03 ROUT3
		V_B4=V_C3:	7.7	r_pi4:	2.68E+02		
I_C4:	1.40E-02 A	I_B4:	9.33E-05	r_o4:	1.26E+04	RIN3	2.16E+04
V_E4:	7 V			r_e4:	1.79E+00	AVth3	9.88E-01
		V_CE3:	6.08			re+Rout2/(B+1)	5.36E+01
Vpi_lin_limit	1.00E-02 Vpk	I_R_C3:	5.43E-04			ROUT3:	4.84E+01
		R_C2:	7.91E+03				

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	Lab 6: Bias Point Matrix					*FINAL ITERATION W/ DARLINGTON PAIR*											
2						SHOWING EQUATIONS											
3	Q-Point Choices				Bias Points			Small Sig Params			Amplifier Params						
4																	
5	Vcc:	12	V														
6	R_Load	200	O														
7	R_source	4.00E+03	O														
8																	
9	Q' (Q1 & Q2)	NPN - CE Darlington Stage				For Voltage gain and high input impedance											
10	Beta 1:	174			V_BB1~	=B18+1.4					Vth:	=B17/(B7+B17)			GAIN	=L17*L26*L34	
11	V_A1:	171			R_B1~	=B17*B5/F10		gm':	=20*B12*(B10+1)*F14		Rth:	=(B7*B17)/(B7+B17)			R_IN	=L15*B17/(B17+L15)	
12	Beta 2:	174			R_B2~	=1/((F11/B17-1)/F11)		r_pi'	=1/(20*F14)						R_OUT	=L36	
13	V_A2:	171			I_Bias1:	=B5/(F11+F12)		r_o'	=(B13+B15)*2/(3*B16)		RL2':	=1/(1/I13+1/F16+1/B27+1/L25)					
14					I_B1~	=B16/(B10*B12)									I_PWR	=(F13+F24+B16+B25+B33)	
15	V_CE2:	5	V		R_E1~	=B18/B16					RIN'	=I12					
16	I_C2:	1.00E-03	A		R_C1~	=(B5-B18-B15)/(B16)					ROUT'	=1/(1/I13+1/F16)			V_OPPK		
17	R_BB1:	3.90E+05	O								AVth'	=-I11*L13			=-2*L26*B36*(I23+(B21+1)*F27)/I23		
18	V_E':	1.8	V														
19																	
20	Q3:	NPN - CE with possible degen.				For Voltage Gain and DC bias for Q4											
21	Beta 3:	150			V_BB2~	=2.5											
22	V_A3:	171			R_B3~	=B27*B5/F21		gm3:	=40*B25		RL2':	=1/(1/I24+1/F37+1/L33)					
23					R_B4~	=1/((F22/B27-1)/F22)		r_pi3:	=B21/I22		Rth2':	=1/(1/L16+1/B27)					
24	V_CE3:	xxxxxxxx			I_Bias2:	=B5/(F22+F23)		r_o3:	=(B22+F35)/B25								
25	I_C3:	4.50E-04	A		I_B3~	=B25/B21					RIN2:	=I23+(B21+1)*F27					
26	V_E3:	1.62	V		R_E2~	=B26/B25					AVth2:	=-I22*L22/(1+I22*F27)					
27	R_BB2:	5.15E+04	O		R_E2a:	5.00E+01	pick to decrease gain				ROUT2:	=1/(1/(I24*(1+I22*F27))+1/F37)					
28																	
29	Q4:	NPN - CC				For driving output											
30	Beta 4:	150			R_E3:	=B34/B33					RL3':	=1/(1/I33+1/F30+1/B6)					
31	V_A4:	171			V_CE4:	=(B5-B34)		gm4:	=40*B33		Rth3':	=L27					
32					V_B4=V_C3:	=B34+0.7		r_pi4:	=B30/I31								
33	I_C4:	1.40E-02	A		I_B4:	=B33/B30		r_o4:	=(B31+F31)/B33		RIN3	=I32+(B30+1)*L30					
34	V_E4:	7	V					r_e4:	=1/I31		AVth3	=I31*L30/(1+I31*L30)					
35					V_CE3:	=F32-B26					re+Rout2/(B+1)	=I34+L27/(B30+1)					
36	Vpi_lin_limit	1.00E-02	Vpk		I_R_C3:	=(F33+B25)					ROUT3:	=L35*F30/(L35+F30)					
37					R_C2:	=(B5-F32)/F36											
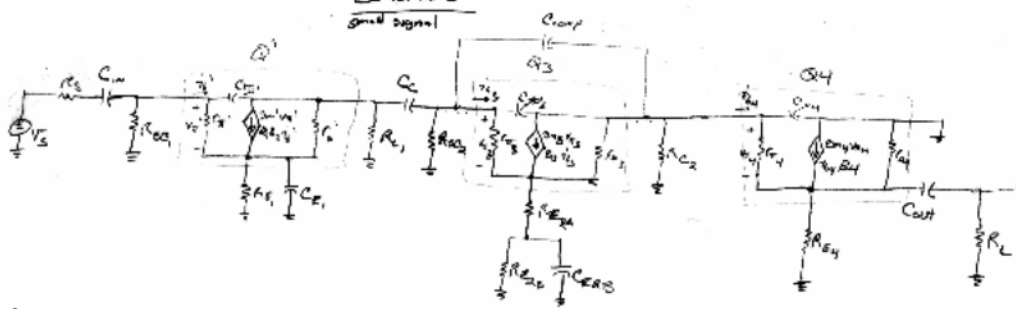
AC Analysis : High Frequency Cutoff

- Assume C_{comp} is dominant pole (in // with $C_{\pi3}$) but not only high frequency effect

  → Why? needs to validate your assumption.

$$R_{TH} = R_{B3_2} // R_1 // r_0'$$

$$R_L' = R_{e_2} // R_{iN4}$$
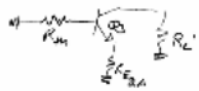
Use eqn 17.110 from book when ignore r_{0_3}

$$R_o = R_L' + R_{TH} // (r_{\pi_3} + (\beta_3) R_{E2A})\left(1 + \frac{\beta_3 R_L'}{r_{\pi_3} + (\beta_3 + 1) R_E}\right)$$

assume $\beta_3 >> 1$

because of simplifications, we expect this to underestimate f_H

as assume OCTC → $w_H = \frac{1}{R_1 C_1 + R_2 C_2 \cdots}$ and this is only taking into account one pole.

We arbitrarily assume our simplifications overestimates f_H a factor of 2.

so

$$f_H = \left[\pi\left(C_{comp} + C_\mu\right)\left(R_L' + R_{TH_3}//r_{\pi_3} + \beta R_E\right)\left(1 + \frac{3R_L'}{r_{\pi_3} + \beta R_E}\right)\right]^{-1}$$

AC Analysis: Low Freq Cutoff

- Could do SCTC method
- instead use equivalent capacitor resistance where

$$X_c = \frac{1}{2\pi f_L C}$$

So make $X_c << R_{x_n}$ where R_x is approximate resistance of circuit and select f_L at desired low frequency cutoff

or approximately

$$C_n > \frac{1}{2\pi f_L X_{e_n}}$$

HF: $R_{th} = 4.54 k$, $R_L' = 5.79 k$ $R_p = 575.36 k$

$C_{comp} = 20 pF$, $C_0 = 4 pF \rightarrow C_c = 24 pF$

$$f_H = \frac{1}{\pi (575.36k)(24pF)} = 23.05 \, kHz$$

LF: all resistances are in the range of $k\Omega$ to 100s of $k\Omega$
want $X_c < 10\Omega$ @ $f_L = 50 Hz$

$$C_n > \frac{1}{2\pi(50Hz)10\Omega} \quad \text{so} \quad C_n > 318 \, \mu F$$

choose $C = 470 \mu F$ so $X_c \approx 6.8 \Omega$

V_{opk}: limit will be due to Q_3, limit is $V_\pi \leq 10 m V_{pk}$
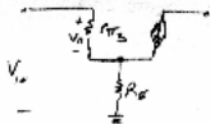
$V_\pi \leq 10 m V_{pk}$, $R_E = 50\Omega$, $r_{\pi_3} = 8.33k$

$$V_\pi = V_{in} \frac{r_{\pi_3}}{r_{\pi_3} + (\beta+1)R_E} = V_{in} \frac{8.33k}{8.33k + 7.55k}$$

$V_{IN} \leq 19 m V_{pk}$

Gain of Q_3 stage is -54.1

$V_{out} = 1.0279 V_{pk} = 2.06 V_{ppk}$

supply voltage rail should be taken into account.

Discussion on Hand Design Values
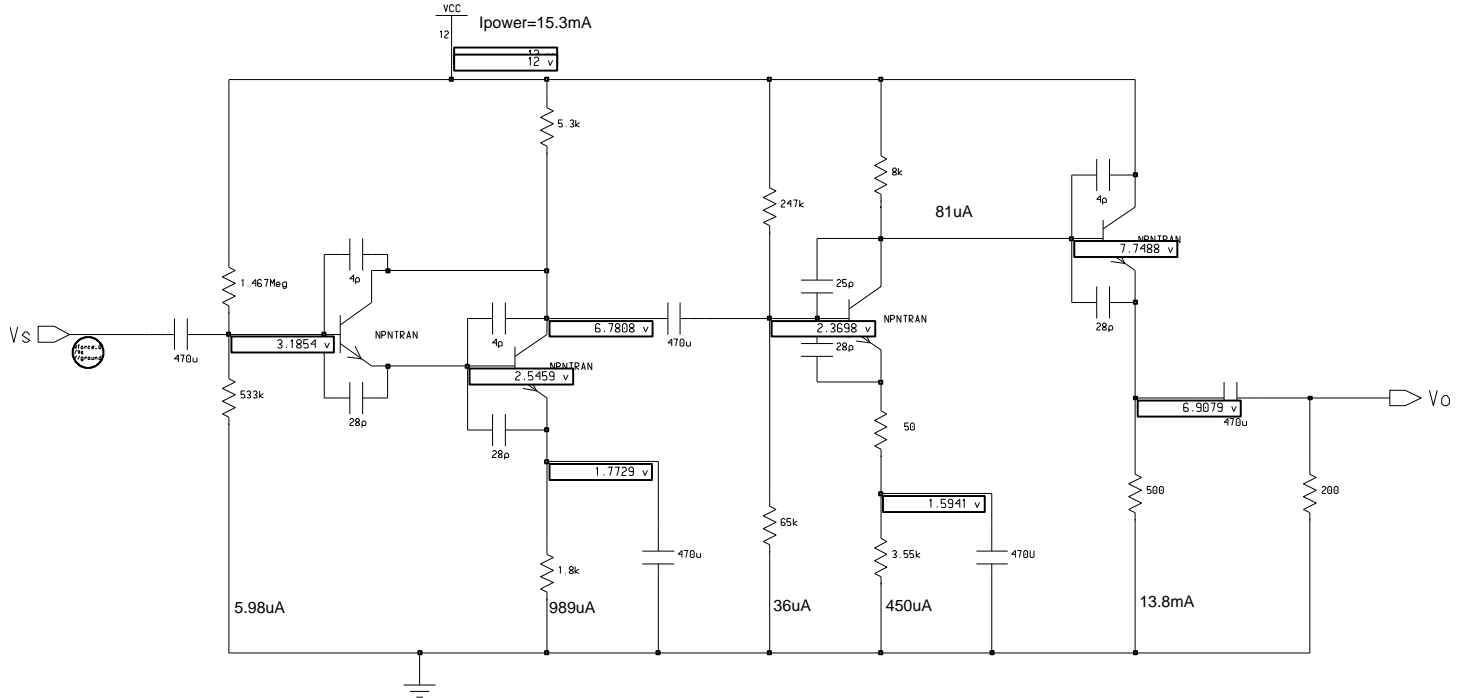
DC Bias conditions

We found that using the spreadsheet definitely decreased the time needed to do one design iteration. It also increased our understanding of the of the material and effects each component had on the rest of the circuit because changes to one part of the circuit were easily propagated to the rest of the circuit.

We followed our design strategy pretty closely using the Darlington stage to guarantee a high input resistance. Then we worried about getting the output swing requirements on the output while ignoring the emitter degeneracy in Q3 to overshoot gain. Because R_{E2a} affects the gain input resistance of the second stage, it has a significant effect on the thevenin equivalent gain of both the first and second stages. At this point, the total amplifier gain was nearly 6000 and the second stage had a higher gain than the first. We slowly increased R_{E2a} while keeping R_{E2} constant until the total gain was brought within the specification and the gain distribution was nearer to our parameter guide.
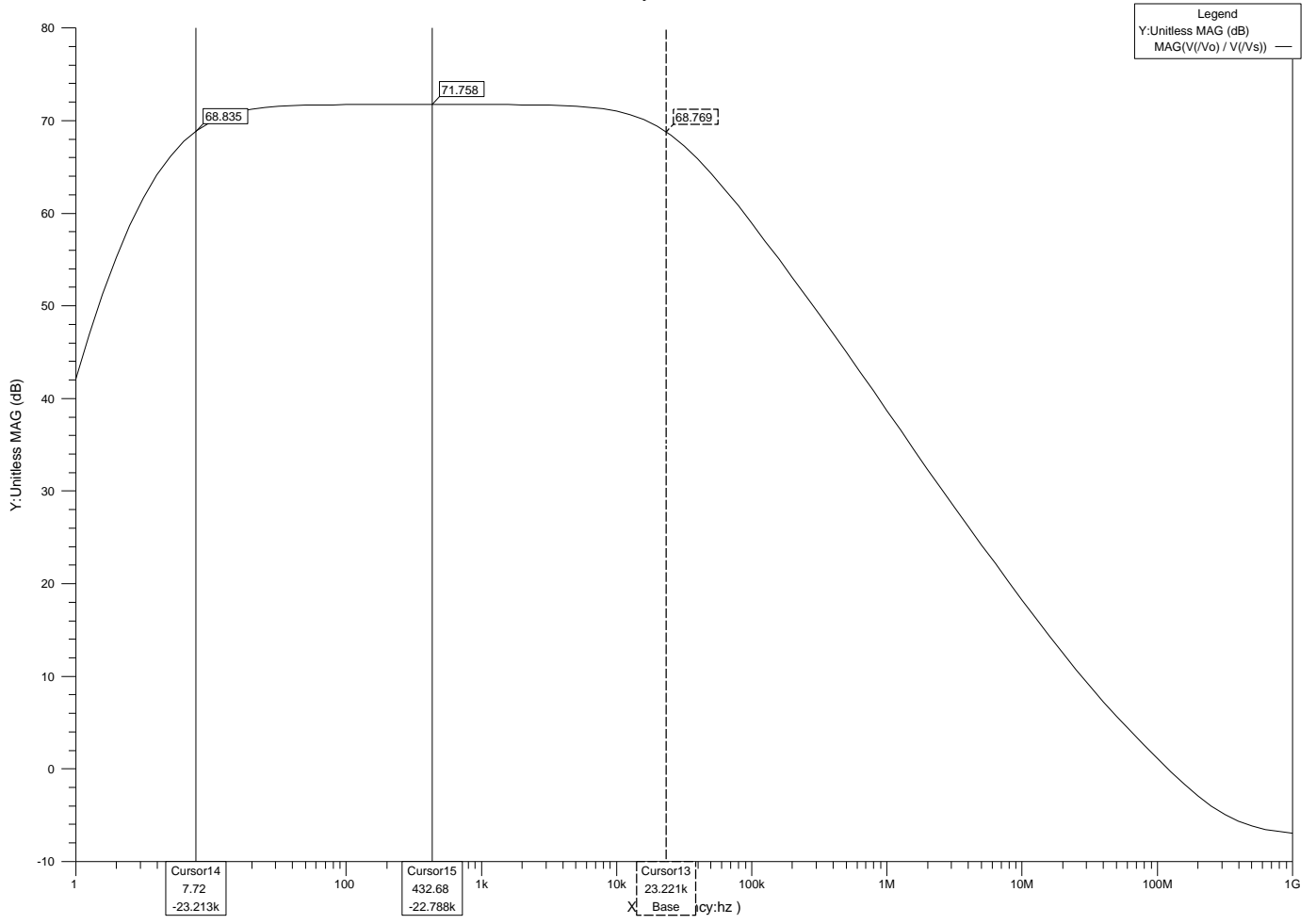
Next we picked the values of the large bypass and coupling caps to have a near zero resistance at our maximum lower cutoff frequency. From Lab 4 we learned that capacitances around 200 to 500μF are needed. Using the formula for capacitive reactance, where $X_c = 1/(2 \pi f C)$, a 470μF capacitor has a resistance of 6.8O at 50Hz. This is negligible compared to the other resistances in the circuit, so we can be sure that our lower frequency limit is below 50Hz. For the compensation capacitor, we assumed that it caused the dominant pole in the frequency response so we ignored other capacitances. Using the technique developed by comparison with Accusim, we selected a capacitor of 24pF. When we subtract the estimated C_μ, we get a value of the compensation capacitor of 20pF.

The last step of hand calculation was to run though and check to see if we had met all the specifications. Although we were able to meet almost all of them, it turned out that we had designed for too high an output resistance. However, with a design that met all the rest of the specifications both by hand and Accusim, we felt that the design was adequate.

ACCUSIM simulation results of DC-Bias conditions (with assumed B=150)

DarTry1:Bode

Y:Unitless MAG (dB)

80

70
71.758

68.835
68.769

60

50

40

30

20

10

0

-10

1   100   1k   10k   100k   1M   10M   100M   1G

Legend
Y:Unitless MAG (dB)
MAG(V(/Vo) / V(/Vs))

Cursor14
7.72
-23.213k

Cursor15
432.68
-22.788k

Cursor13
23.221k

X__Base__cy:hz)

Vout Swing and Rin
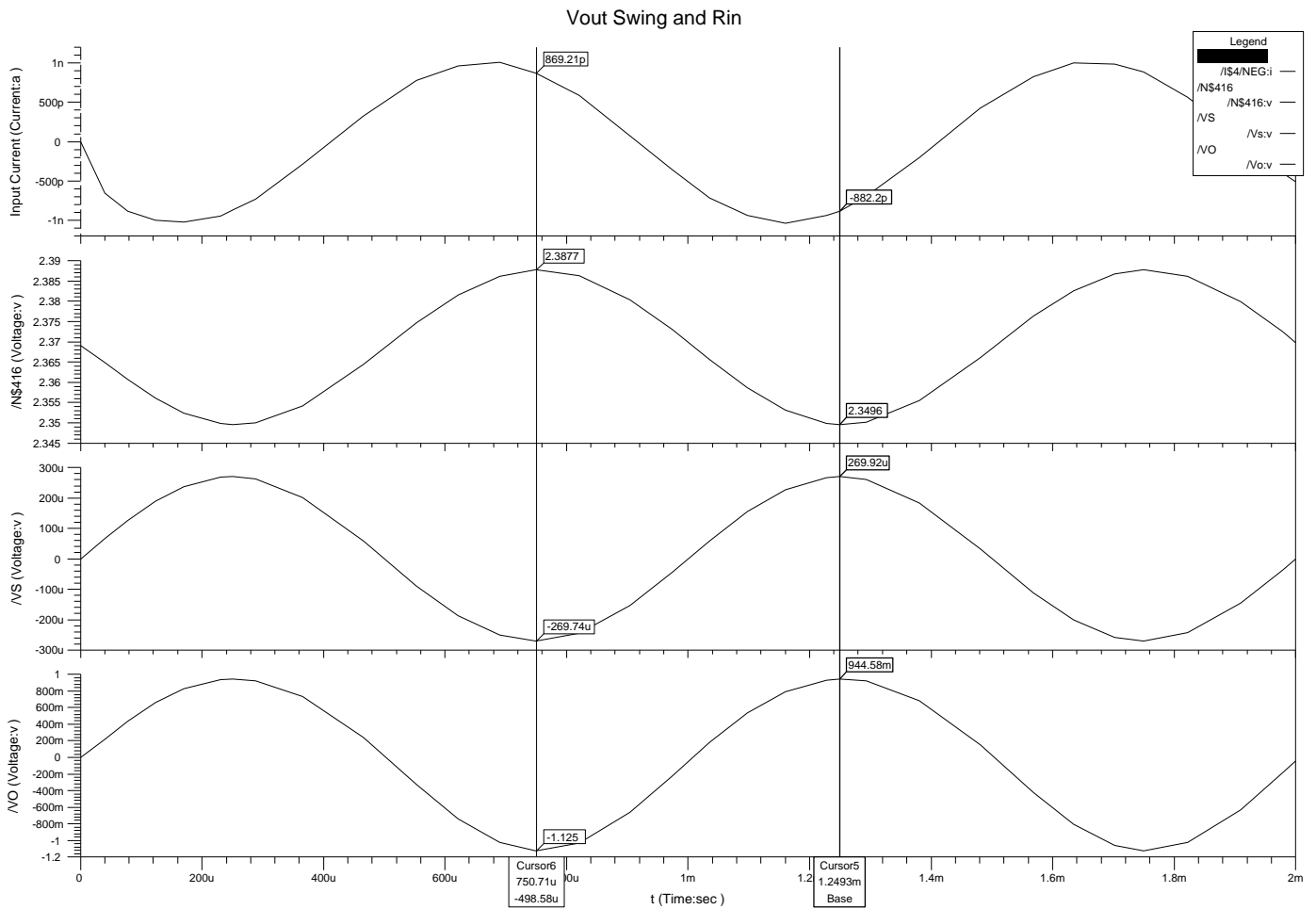
Vout=(994.58m+1.125)=2.0697Vppk

Rin = Vin/Iin = 269.92uV/882.2pA = 305.9kohms

Gain of First stage: Av1=(2.3496-2.3877)/(269.92u+269.74u)=70.6
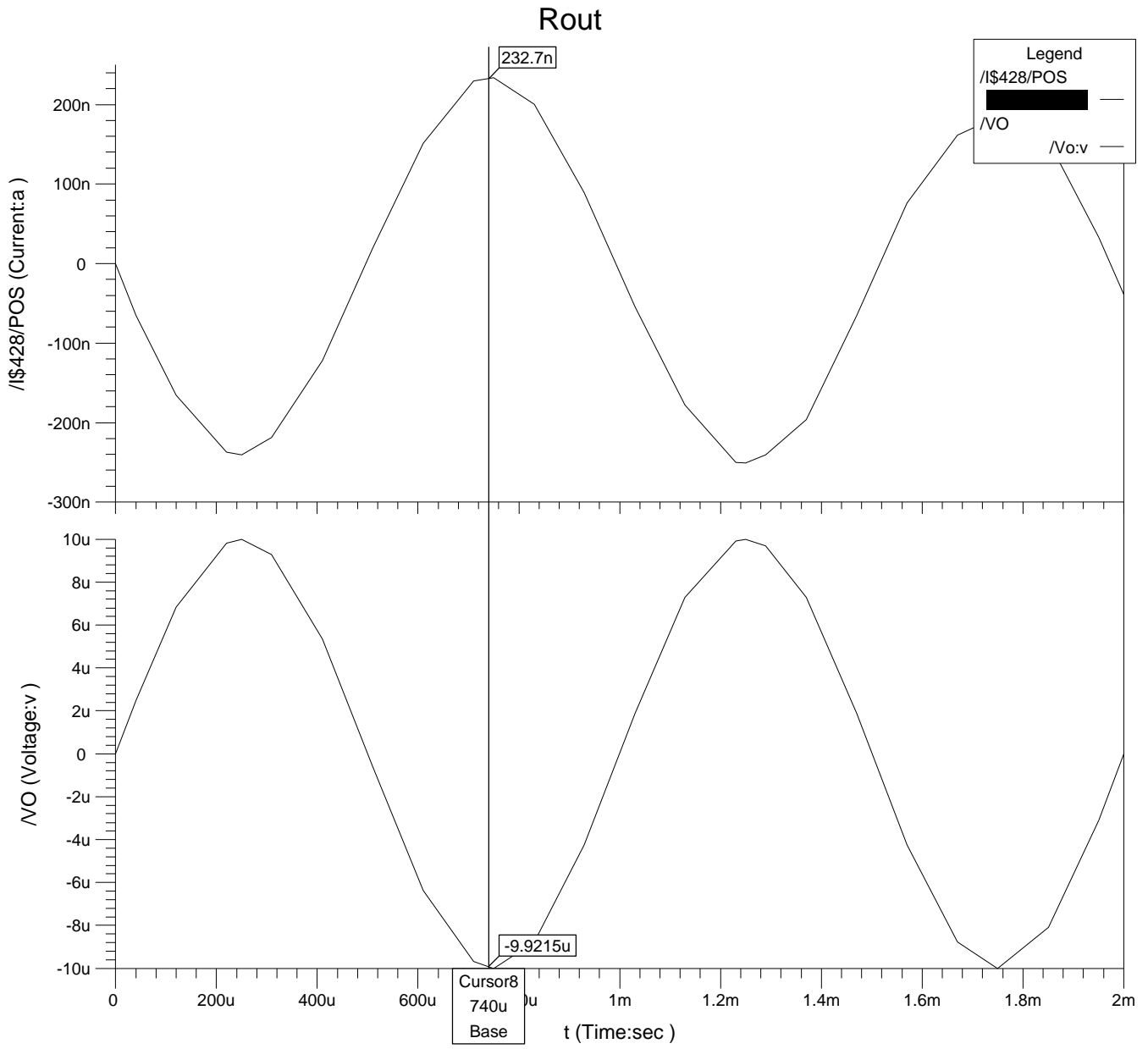
Rout

Rout = Vout/Iout = 9.9215uV/232.7nA = 42.6ohm

In lab value measurements (Voltage, Current & Components)

15.07mA = Total Power
Supply Current Draw
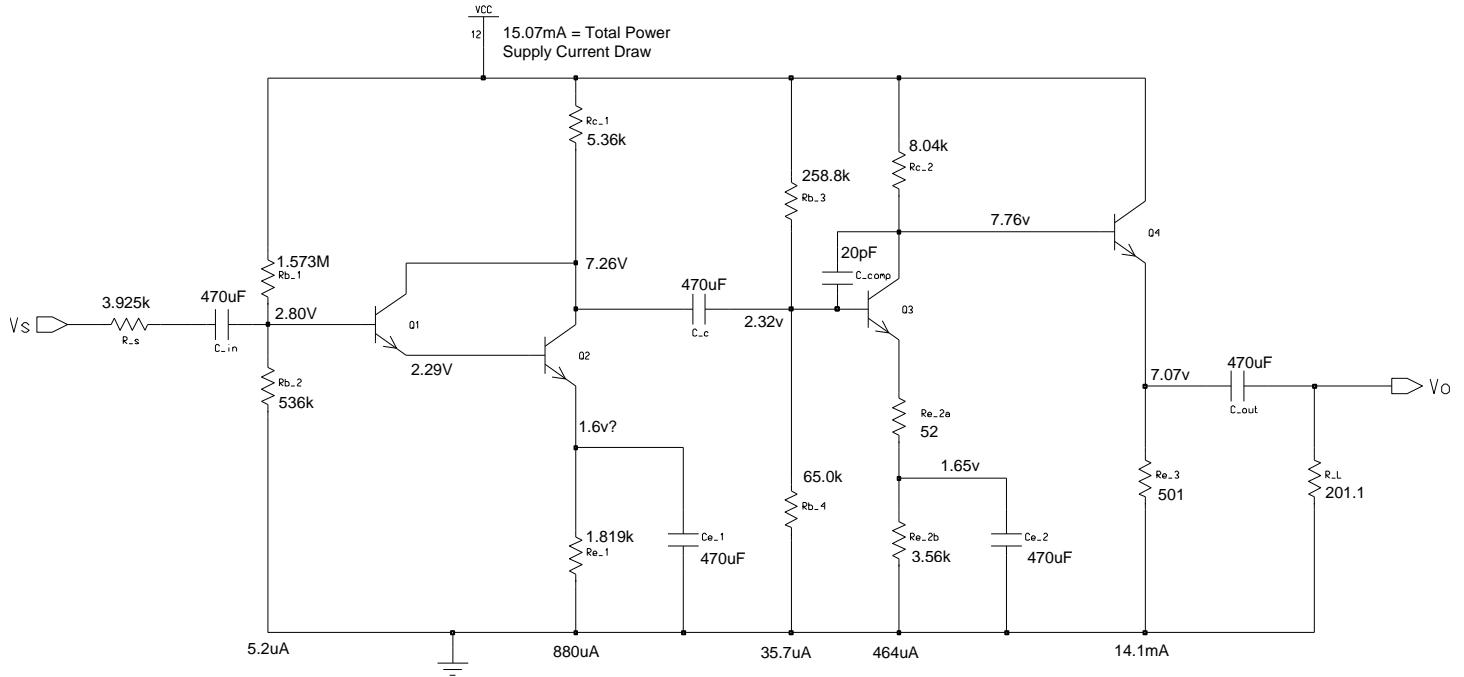
Currents are
calculated from I=V/R

Frequency Response of circuit

5c)

Gain - Mid Band Gain

1 100mV/   2 200mV/   0.00s 500µ/   AV   E RUN

V_A

V_O

Freq(1)=997.5 Hz   Vp-p(1)=100.0mV   Vp-p(2)=462.5mV

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	100.0mV	171.9mV	ac	off	off	10:1
2	on	200.0mV	-400.0mV	ac	off	off	10:1

Horizontal	Mode	Main s/div	Delay	Reference
	main	500.0us	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	extern	0.000 V	+	dc	off	off	200.0ns

Display	Mode
	average: 4

$$A_{V_{mo}} = \frac{462.5mv}{100.0mv} \cdot .926 = -4.283$$

Attenuation

$$V_A \quad \frac{10.6k + 9.81k}{10.6} = 926 \, V_s$$

5d) f_L - low frequency pole

1 ⇃100m/   **2** ⇃200m/   ⌐ 0.00s 20.0m/ 🅰🅴   ⨏E **RUN**

Freq(1)=7.943 Hz   Vp-p(1)=96.87mV   Vp-p(2)=325.0mV

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	100.0mV	171.9mV	ac	off	off	10:1
2	on	200.0mV	-400.0mV	ac	off	off	10:1

Horizontal	Mode	Main s/div	Delay	Reference
	main	20.00ms	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
	edge	extern	3.492 V	+	dc	off	off	200.0ns

Display	Mode
	average: 4

5 e) f_H - High frequency pole

HP54645A System A.02.06   21:10:35 Tue Dec 3, 2002
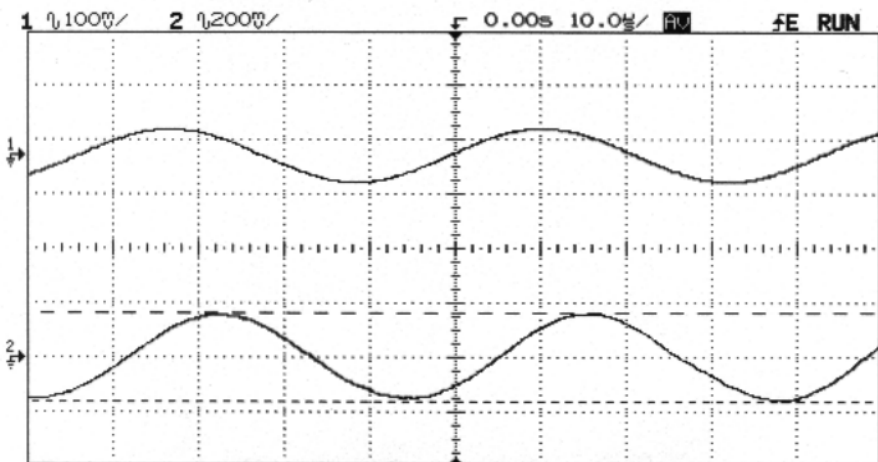
```
1 ↕100m/   2 ↕200m/          ┌ 0.00s 10.0↕/ AV      ƒE  RUN
```

```
Freq(1)=23.01kHz      Vp-p(1)=96.87mV        Vp-p(2)=325.0mV
```

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	100.0mV	171.9mV	ac	off	off	10:1
2	on	200.0mV	-400.0mV	ac	off	off	10:1

Horizontal	Mode	Main s/div	Delay	Reference
	main	10.00us	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	extern	3.492 V	+	dc	off	off	200.0ns

Display	Mode
	average: 4

22

5f)

Output voltage Swing

HP54645A System A.02.06   21:29:59 Tue Dec 3, 2002

```
1  200V/   2  1.00V/          0.00s 200s/   HV      fE RUN
```
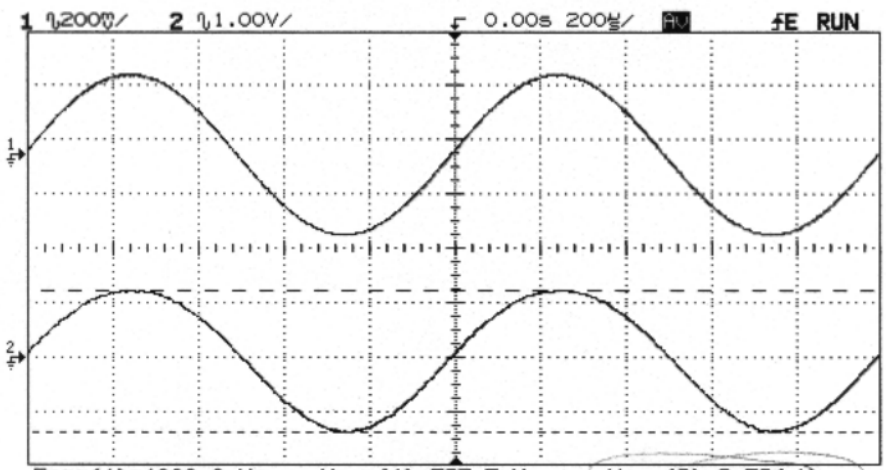
Freq(1)=1000.0 Hz   Vp-p(1)=587.5mV   Vp-p(2)=2.594 V

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	200.0mV	343.7mV	ac	off	off	10:1
2	on	1.000 V	-2.000 V	ac	off	off	10:1

Horizontal	Mode	Main s/div	Delay	Reference
	main	200.0us	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	extern	1.195 V	+	dc	off	on	200.0ns

Display	Mode
	average: 4

Discussion on Experimental Results

Primary Results

      Upon initial power up, we had to wait a very long time for the circuit to reach near its specified DC bias points. This "warm-up" period is to the time constant of the coupling and bypass capacitors, most notably the input coupling capacitor C_{in}. The equivalent resistance that C_{in} sees is approximately $R_{b1}//R_{b2} \sim 400kO$. The time constant of an RC circuit is $t=RC=400k?470\mu=188$ seconds, which corresponds to the capacitor charging to 63% of its steady state value. An RC circuit takes about 5 time constants to reach 99% of its steady state value and this corresponds to approximately 16 minutes. Disconnecting power or the input source resulted in the capacitor discharging. This made measurements in lab someone time consuming.

      Once the circuit had reached approximately steady state, the measured amplifier parameters matched very well with both hand calculations and computer simulations. The equation $\%err = 100 \cdot |LabValue - AccusimValue|/AccusimValue$ is used to evaluate percent error deviation of lab measurements with respect to the simulated values. The only two measurements that were significantly off were mid-band gain and output peak voltage. They were still within specification but higher than simulations by 10% and 25% respectively. All the other parameter measurements were well within 2% of the Accusim simulations. Furthermore, the DC bias measurements were also well matched to simulation. In the second and third stages, all the voltage and current measurements agree within 3% of each other. However, in the first Darlington stage, there is slightly more variation, up to 12%, caused mainly by the current gain multiplication effects of the Darlington pair. It is rather remarkable that the values match this well, especially given that hand calculations and simulations assumed all transistors had uniform current gain and Early voltage. Two factors that helped achieve such good matching were the use of 1% tolerance RC55 series resistors for the biasing network, and a good design that was insensitive to moderate changes in individual transistor parameters.

Failure Modes

      Initially, we constructed in the circuit in the Student Projects Lab (SPLab) next door to the EECS 311 lab room due to a lack of available space. At this point the circuit was totally stable in all respects. However, moving the circuit into the EECS 311 lab room generated three distinct results that could be classified as failure modes. These failure modes were sporadic and intermittent. It seemed that the location of people, equipment and wiring in the lab significantly affected when and how the failure modes appeared. The first failure mode was a oscillation of the power supply current draw, which manifested itself in conjunction with the other failure modes. Normally, the circuit would draw 15mA, but in this failure mode the power supply current would ramp down to 0mA and then spike up to 25mA with an oscillation rate between 0.5 and 6 seconds. The circuit would not amplify any signal but would produce output spikes that corresponded with the supply current peaks and dips. In the second failure mode, the circuit would go into ultrasonic oscillation at around 15MHz and again not amplify any input signal. The last failure mode was significant low frequency oscillations with a frequency near 6Hz. Interestingly enough, the only way to prevent these failure modes, which only occurred in the EECS 311 lab, was to hold a voltmeter probe on the positive supply rail beside the last output stage.
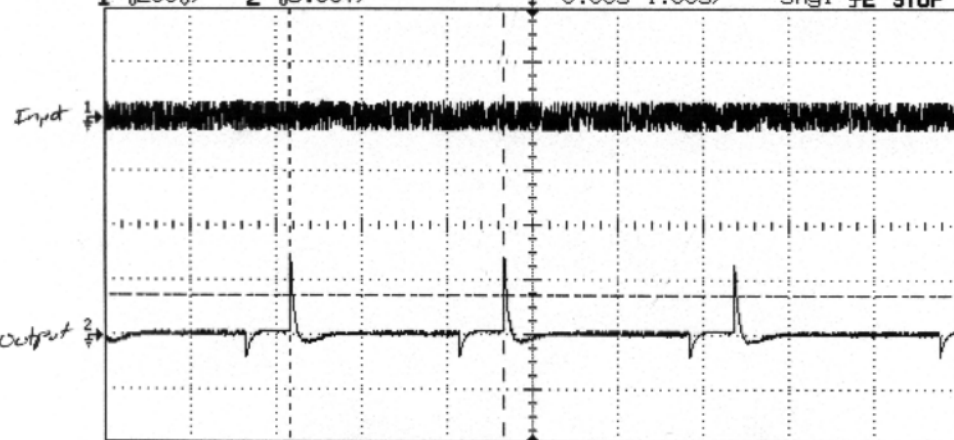
Failure mode

1 ⫸200�室/   2 ⫸5.00V/   ⌐ 0.00s 1.00s/   Sng1 ꜰE **STOP**

Input 1

Output 2

Freq(2)=400.0mHz

↳ spikes correspond
+ power supply fluctuation

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	200.0mV	393.8mV	ac	off	off	1:1 A
2	on	5.000 V	-10.16 V	ac	off	off	10:1 A

Horizontal	Mode	Main s/div	Delay	Reference
	main	1.000 s	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	extern	0.000 V	+	dc	off	off	200.0ns

Display	Mode
	normal

Failure Mode 1
Power supply current fluctuations

25

HF oscillation in Failure mode
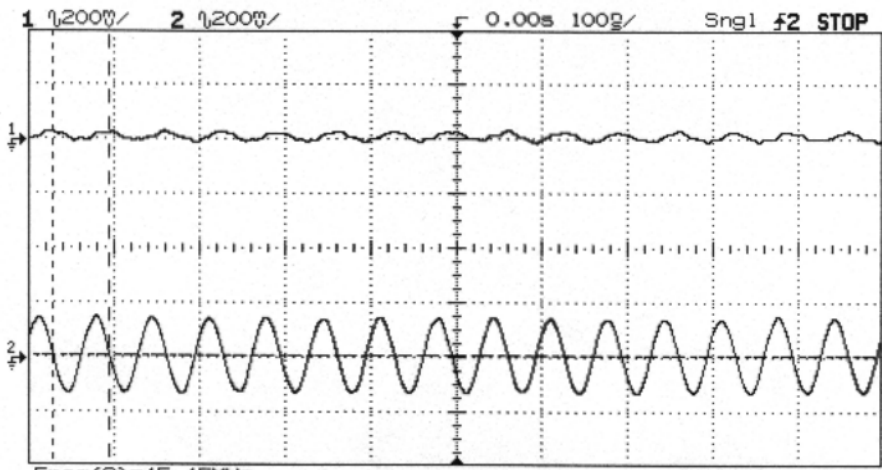
1 ↯200៣/   2 ↯200៣/   ⌐ 0.00s 100៣/   Sng1 ƒ2 **STOP**

Freq(2)=15.15MHz

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	200.0mV	393.8mV	ac	off	off	1:1 A
2	on	200.0mV	-406.2mV	ac	off	off	10:1 A

Horizontal	Mode	Main s/div	Delay	Reference
	main	100.0ns	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	2	0.000 V	+	dc	1f	on	200.0ns

Display	Mode
	normal

HF oscillation

Failure Mode 2
HF 15mHz oscillation

26

Failure mode low frequency oscillation
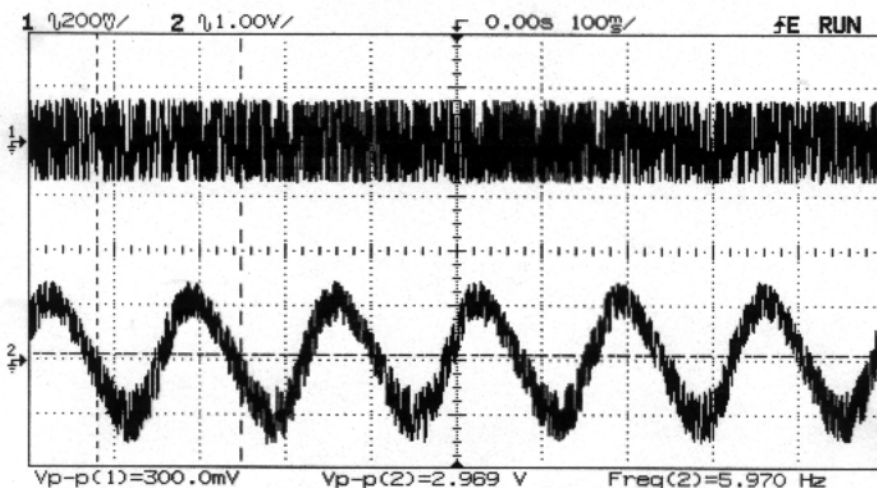
```
1 ↕200ⅴ/     2 ↕1.00V/            ⌐ 0.00s 100ᵐ/          �___E  RUN
```


Vp-p(1)=300.0mV   Vp-p(2)=2.969 V   Freq(2)=5.970 Hz

Vertical	State	Volts/div	Position	Coupling	BW limit	Invert	Probe
1	on	200.0mV	393.8mV	ac	off	off	1:1 A
2	on	1.000 V	-2.031 V	ac	off	off	10:1 A

Horizontal	Mode	Main s/div	Delay	Reference
	main	100.0ms	0.000 s	center

Trigger	Source	Level	Slope	Coupling	Rej	NoiseRej	Holdoff
edge	extern	0.000 V	+	dc	lf	on	500.2us

Display	Mode
	normal

Failure Mode 3

Low Frequency Oscillation

27

Summary

Summary of specifications for each stage of design:

Parameter	Requirement	Hand Calculations	ACCUSIM	Lab Measurement
A_{VMID}	2625 – 4375	3790	3872	4283
f_L	<50Hz	<<50Hz	7.72Hz	7.94Hz
f_H	21kHz – 25kHz	23.05kHz	23.221kHz	23.01kHz
R_{in}	>100kO	310kO	305.9kO	N/M
R_{out}	<25O	48.45O *	42.6O *	N/M
V_{oppk}	>2.0V_{ppk}	2.06V_{ppk}	>2.0697V_{ppk}	2.594V_{ppk}
I_{pwr}	<25mA	15.5mA	15.3mA	15.07mA
R_{Load}	200O	200O	200O	201.1O
R_s	4.00kO	4.00kO	4.00kO	3.925kO
# Transistors	<4	4	4	4
# Capacitors	<5	5	5	5
Bias Stability	βR_E>10R_B I_{bias}>10I_b	YES	YES	YES

*Did not meet specifications   N/M: Was not measured.

Conclusion

Our design met all the specifications except the output impedance. Since we were unable to measure the output impedance of the circuit in the laboratory, we do not know what the exact value of it was, but our hand calculations and ACCUSIM simulation gave a very high value, so we expect it to be higher than the specifications. The only way to decrease the output impedance is to decrease the equivalent resistance of the first two stages, requiring a completely new design. Given the time constraint, we decided not to redo everything.

In all other aspects our circuit performed much better than the given specifications; our output impedance is three times higher than the required minimum, undistorted swing is 60% larger than the required minimum, while power consumption is 37% less than the maximum, voltage gain is within the requirements, high frequency cut-off is right on target and the low frequency cut-off is about one sixth of the required maximum.

As seen on the table above; measured, simulated and calculated values are very close to each other. In fact other than the voltage gain, they are almost identical. The difference between the measured and simulated gains can be due to parasitic capacitances which were ignored or variances in device parameters, as we did not characterize each of the transistors.