Origin, Evolution, and Control of Sidewall Line Edge Roughness Transfer During Plasma Etching

By

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Abstract

For the pattrerning of sub 100 nm features, a clear understanding of the origin and control of line edge roughness (LER) is extremely desirable, both from a fundamental as well as a manufacturing perspective. Until recently LER studies have focused on the anlaysis of top-down SEM micrographs of post-developed photoresist lines. However the effect of plasma etch on sidewall roughness has not received sufficient attention. Plasma etching processes often roughen the feature sidewalls, leading to the formation of anisotropic striations. It is this post-etch sidewall roughness which will ultimately affect device performance.

In this thesis, I have attempted to provided a thorough investigation into sidewall roughness transfer occurring on a variety of industrially relevant systems and toolsets, and to identify potential mechanisms for improvement through processing and materials solutions. Additionally more fundamental work was performed on blanket samples though the identification of a novel polymer-induced roughening mechanism on low-k dielectric films. Finally a new apparatus was constructed and characterized that will allow the study of roughness and striation formation through a decoupling of plasma parameters that is impossible to achieve in a traditional plasma etcher.

Sidewall roughness transfer through all layers of a process stack (photoresist, ARC/hardmask, and oxide) was observed by cleaving dense line/space patterns parallel to the lines, and directly scanning the exposed sidewall with an atomic force microscope. This technique vividly highlighted the structural nature of the post–etch sidewall and allowed the extraction of quantitative roughness data as a function of depth.

Sidewall roughness transfer was observed during the ARC/HM open and subsequent oxide etch for 248 nm and 193 nm systems, with a wide variety of organic ARCs, hardmasks, Si-containing ARCs, and bilayers. The initial 248 nm lithography sidewall morphology was isotropic in nature with a 3-5 nm 1-σ RMS roughness, and was relatively constant as a function of depth. After the ARC/hardmask etch, however, and was relatively constant as a function of depth. After the ARC/hardmask etch, however, the sidewall morphology took on an anisotropic characteristic, with striations created by ion bombardment. During the subsequent oxide etch, these striations transfer into the oxide sidewall, the anisotropic topography created during the ARC/hardmask etch casting the morphology of the oxide layer beneath. While all resist systems were about equivalent from a roughness standpoint after the ARC/hardmask etch, they showed variation after oxide etch. On the 248 nm resist platforms, hardmask and Si containing ARC

samples allowed more roughness transfer during an aggressive oxide etch than organic ARC samples, perhaps due to the polymerizing nature of the Si ARC/hardmask open chemistry, or to compositional differences between these films as compared to the organic ARC. On the 193 nm resist platforms, a less aggressive (higher pressure, lower ion bombardment) oxide etch was required due to the lower etch resistance versus 248 nm systems. However this gentler oxide etch allowed the oxide to be opened relatively smoothly regardless of the resist type, leaving the post-etch oxide SWR comparable to that obtained with 248 nm organic resist/ARC. These results indicate that the SWR on the oxide substrate can be maintained within reasonable limits, as long as the increasing resist/ARC roughness does not extend to the oxide surface.

Mechanisms for sidewall roughness improvement via modulation of processing parameters (specifically the ARC/hardmask open) were demonstrated. By using a more "chemical" type ARC/HM etch, striations during the ARC/HM open were reduced, resulting in a smoother sidewall after oxide etch. The improvement was dramatic particularly on the hardmask samples, with a roughness reduction from 8 nm to 3.3 nm RMS at the oxide/hardmask interface.During a polysilicon gate etching process, polymerization during the hardmask open was shown to drive roughness formation during a subsequent gate etch. Excess polymerization filled in imperfections in the sidewall resulting in smoother gates, at the cost of increasing the critical dimension.

The effects of employing thin and/or fluorinated resists (needed for the advent of 157 nm resist systems and more generally "thin film imaging") on roughness transfer were investigated. Thin resists obviously present a potential problem due to the loss of masking material when etching deep trenches. Additionally the addition of fluorine to a resist structure can enhance the etching of the resist if the fluorine content exceeds a particular threshold, especially at the feature edges. These results have important implications for the success of 157 nm lithography. Because 157 nm resists are expected to be heavily fluorinated and extremely thin, it may become impossible to pattern certain levels using the conventional single layer resist/organic ARC approach that works well for 248 and 193 nm systems. These levels will require the use of alternative patterning schemes such as hardmask and/or bilayer approaches, which are expected to gain importance as the industry migrates to sub-70 nodes.

Polymer-induced micromasking was demonstrated as a roughening mechanism during fluorocarbon etching of low-k and porous low-k (OSG and MSQ) dielectric films. Micromasking occurs under certain etching conditions when regions of localized net polymerization form on the surface of the etched film. Porous low-k films seem especially prone to this localized polymerization, perhaps due to polymer diffusion and seeding into the pore structure. Once formed, etch selectivity between regions of net polymerization and net etching on the surface lead to roughening. Control of polymerization during the etch through the use of lower-polymerizing fluorocarbons or the addition of oxygen was shown to effectively control excessive roughening on solid films, while porous dielectrics remain challenging.

While these results present a plentiful display of etch-induced roughness encountered in common etching processes, a fundamental study of post-etch sidewall roughness remains due to the inherent experimental difficulties encountered. Sidewall roughening during etching depends on the plasma chemistry, ion bombardment energy, and ion incident angle. A true fundamental study requires independent control of all three parameters, impossible to obtain in a conventional etcher. To remedy these difficulties, an inductively-coupled plasma beam source was constructed that allows the exposure of a sample to a realistic ion and neutral flux, of any desired plasma chemistry, while allowing independent control of the ion bombardment energy

and incident angle. To simulate a sidewall, the sample was rotated to a near-glancing angle. The ion bombardment energy can be selected by DC biasing the plasma, which is isolated from the source chamber walls by a quartz or alulmina ceramic liner.

After fully characterizing the ion energy and beam uniformity in the new source, it was used to conduct our first preliminary investigation into a mechanism behind striation formation. Polysilicon samples (with a rough texture characterized by grain boundaries) and single crystal silicon samples (which are smooth) were placed in an HBr plasma beam at various angles and ion bombardment energies. Ion bombardment smoothed the high points on the polysilicon surface. Additionally, at near glancing angle striations formed on the polysilicon, which is explained via 1) previously measured angular etch yield curves that predict ion reflection at steep impingement angles, and 2) by shadowing of the incoming ion flux by the larger grain structures. The single crystal samples were smooth at all conditions. These results indicate that the initial surface topography can drive striation formation via ion reflection and shadowing.

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