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Heat Transfer at Small Dimensions

MICROSCALE THERMAL ENGINEERING OF ELECTRONIC SYSTEMS

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ABSTRACT

The electronics industry is encountering thermal challenges and opportunities with lengthscales comparable to or much less than one micrometer. Examples include nanoscale phonon hotspots in transistors and the increasing temperature rise in on-chip interconnects. Millimeter-scale hotspots on microprocessors, resulting from varying rates of power consumption, are being addressed using two-phase microchannel heat sinks. Nanoscale thermal data storage technology has received much attention recently. This paper provides an overview of these topics with a focus on related research at Stanford University.

INTRODUCTION

Thermal management has been an important concern for the electronics industry for several decades, and it has grown more critical in the past few years owing to increases in the total heat generation rate, and the heat generation rate per unit area, of modern micrporcessors. This trend has been accompanied by an extension of the dimensions of many challenging problems down to deep sub-micrometer lengthscales. In the past, the main thermal management activities were in air routing and system level management and the design of metal heat sinks, heat pipes, and vapor chambers. While these activities remain important, a new set of challenges and opportunities at the micro and nanoscale are growing crucial. These are occurring primarily, or close to, the semiconductor chip, as summarized in these four examples:

Nanoscale Transistor Hotspots: As silicon transistor channel lengths decrease below 100 nm, the spatial volume and number of lattice vibrational states gaining energy from electron scattering are also decreasing. This results in extreme nonequilibirum phonon populations within the device, which impedes conduction cooling and reduces both the source injection and drain series resistances. The impact on device design will be dramatic for transistors below the 50 nm node.

Interconnect Heating: Another on-chip thermal problem is the temperature rise in the metal interconnect structures on chips. The trends to higher current interconnect densities, extreme interconnect aspect ratios, and more metal layers are raising the metal temperature rise to tens of degrees Celsius. This problem is aggravated by trends to novel organic and porous dielectrics, which impeded thermal conduction.

Novel Thermal Microdevices for Information Storage and Diagnostics: Advancements in micro and nanomachining have enabled new realms of imaging and data storage technologies, which are finding impact for the IC industry. This section of the paper presents two novel thermal microstructures including cantilever beams for data storage and microlenses for precise scanning.

Two-Phase Microchannel Heat Sinks and Chip-Level Hotspots: Highly nonuniform rate of heat generation on a semiconductor chip increases the peak chip temperature for a

given total power. This yields milliscale hotspots on the chip, and an excellent approach to cooling them is two-phase convection in microchannel heat sinks. The study of boiling flow in microchannels offers important challenges for pressure stability and convective resistance reduction.

NANOSCALE TRANSISTOR HOTSPOTS

Modeling heat generation at nanoscales in semiconductors is of great interest and particularly relevant to the heating and reliability of nanoscale transistors [1]. With the widespread use of sub-100 nm transistors around the corner, the problem of localized heating of the silicon lattice, induced by electron relaxation, is of increasing importance. Nanoscale heat sources or phonon hotspots, with size of the order of 10 nm and power density reaching 10^{18} W/m^3, are expected to form in the drain of such devices [2]. Such hotspots, with increased populations of slow optical phonons, are expected to exhibit ballistic phonon transport with reduced thermal conductance. Furthermore, the disparity in the electron and phonon relaxation rates by one order of magnitude will cause significant non-equilibrium in the phonon system.

Our past thermometry measurements on a suspended silicon thin film sample have confirmed that the diffusion theory of heat conduction, which is widely used in industrial device simulators, severely underestimates temperatures near such a sub-continuum heat source [3]. We have developed a compact model predicting a fourfold increase in the drain resistance for a channel length smaller than 30 nm. The predicted peak temperature inside such a source is consistent with the experimental data (Fig. 1). The model is, however, too simplistic to provide a full temperature field near a hotspot in a modern transistor.

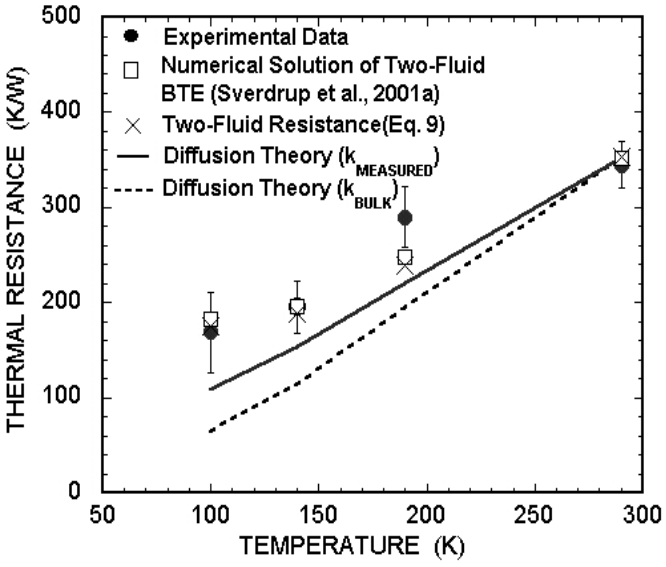


Figure 1. Predictions and data from a measurement of the temperature rise in a doped silicon thermistor suspended in a silicon bridge [3]. As the absolute temperature is reduced, the ratio of the phonon mean free path to the size of the heat source increases, which augments the size effect on conduction and shows the failure of simple diffusion theory.

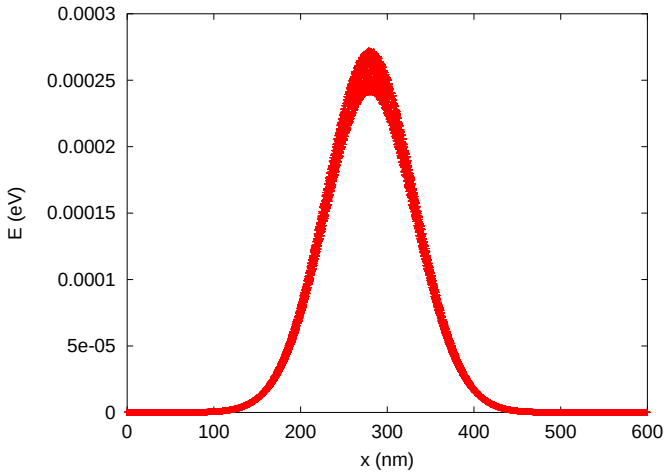


Figure 2. The energy distribution in an atomistic simulation of a phonon hotspot. These simulations were performed in collaboration with S. Phillpot and coworkers at Argonne National Laboratory [4].

The physics of phonon transport at the hotspot needs to be resolved in some detail, and parameters such as mode and amplitude dependent scattering times of optical phonons need to be estimated before a detailed model based on the Boltzmann equation can be developed. It is known from first order perturbation theory of phonons that anharmonic decay rates are strongly affected by large phonon occupation numbers, which are likely at the hotspot. We are investigating the physics of the decay process through atomistic simulations of phonon wavepackets. The wavepackets are constructed from the normal modes obtained using the Stillinger-Weber potential. We model the spatial confinement of the hotspot in an actual device by a Gaussian spread of the wavepacket energy in space (Fig. 2) such that the energy density corresponds to that in the transistor drain. The initial phonon is chosen such that it has a high scattering probability with conduction electrons in silicon. Molecular dynamics is used to evolve the wavepackets in time. Due to computational constraints, we simulate the dynamics of the wavepacket in a one-dimensional system with 64000 atoms. Preliminary results indicate that longitudinal optical wavepackets with hotspot like energies are quite stable in the absence of other phonons. They are found to emit long wavelength longitudinal acoustic phonons that travel at about 8000 m/s as well as other long wavelength acoustic modes that travel with velocities similar to the original optical modes, about 1500 m/s [4]. The energy in the optical wavepacket does not decay significantly for times upwards of a nanosecond. We are currently investigating the interaction of such a wavepacket with other phonons in the lattice.

While the phonon Boltzmann Transport Equation (BTE) has been used to study conduction in nanostructures, its electronic Joule heating term is not accurately modeled as the dot product of the *macroscopic* electric field and current density [5]. This approach does not account for the *microscopic* non-locality of heat generation near a strongly peaked electric field region. It also does not account for branch- and polarization-specific phonon heating. In silicon, as in most semiconductors, Joule heat generation is usually

dominated by optical phonon emission (Fig. 3). Optical phonons are slow and they make virtually no contribution to heat transport. Rather, they decay into the faster acoustic modes which transport the energy away from the hottest regions. If the generation rate of optical modes due to Joule heating via current flow is higher than their rate of decay into acoustic modes, the optical mode density can build up over time, affecting the electron transport. Hence, it is important to understand in detail which phonon modes acquire and which ones transport the electronically-generated heat (Fig. 4), particularly at nanometer scales on the order of the electron and phonon mean free path.

We have implemented an electron Monte Carlo (MC) simulation method to compute the phonon generation rates throughout the Brillouin Zone [6]. The electron energy bands and the phonon dispersion relationship are modeled with realistic analytical curves. Care is taken to incorporate inelastic scattering with both intra- and inter-valley phonons. The emphasis is on detailed physical modeling within a computationally efficient implementation. The use of analytical electron bands and phonon dispersion allows for simulations which are orders of magnitude faster than full-band techniques. This approximation is reasonable because future generations of electron devices are expected to operate at voltages below the silicon band gap (1.1 eV). Hence impact ionization and high band structure electron transport can be neglected.

Previous analytic-band MC approaches have grouped longitudinal and transverse acoustic phonons together, making no distinction between them. This work is the first electron MC calculation to distinguish between the two polarizations, and this becomes particularly relevant near the edge of the Brillouin Zone where transverse acoustic phonons are nearly stationary. The relative magnitude of phonon generation rates throughout the Brillouin Zone and for all phonon branches can be simulated for various uniform electric fields. The simulation can also be run on the non-uniform electric field distribution inside a real electron device. The detailed heating rates can be extracted to aid in the thermal design of future generations of nanotransistors.

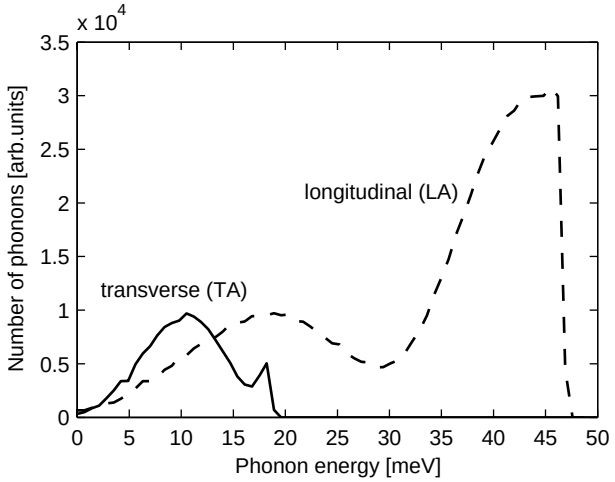


Figure 3: Summary of Joule heating and energy transfer processes in silicon [6].

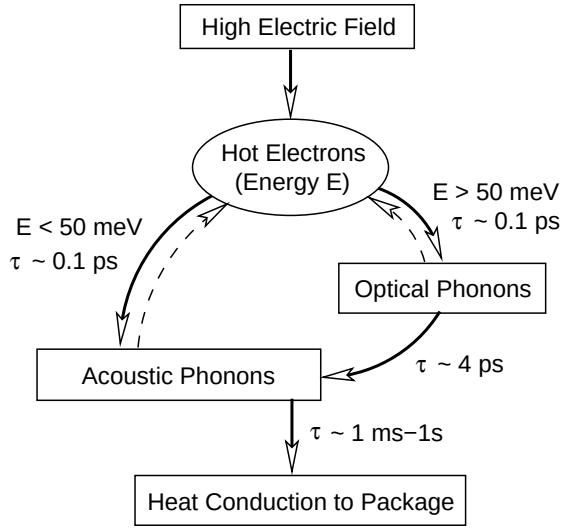


Figure 4: Computed acoustic phonon net (emission minus absorption) generation rates due to electron phonon scattering [6].

Ongoing work is exploring the extension of these simulations to confined (in 2-D thin films) and coupled electro-thermal. The information and source code will be shared online [7]. This work represents a simulation approach which aims to fill the gap of nano-engineering tools between simple analytic-band MC codes and more complex full-band simulators.

INTERCONNECT HEATING

In advanced microprocessors, interconnect Joule heating becomes more important due to aggressive technology scaling. The global interconnect temperatures will significantly increase despite smaller projected increases in the chip power density [8]. We have simulated temperature within the ICs using fully coupled three-dimensional finite element thermal simulation accounting for heat generation in the devices and Joule heating in the interconnects and considering the trend to poorly conducting dielectric materials surrounding the interconnects. The simulations at various technology nodes are based on parameters determined from the International Technology Roadmap for Semiconductors (ITRS) data [9]. Figure 5 shows spatial temperature distributions in the vertical direction from the silicon substrate to the top global metal level in an integrated circuit. With technology scaling, the maximum temperature in the chip (T_{max}) increases and the temperature gradient between the top metal lines and the silicon substrate becomes larger. Simulation results indicate that the device power dissipation is dominant for determining T_{max} for current technology nodes, whereas interconnect Joule heating is significant for sub-100 nm regime. For 35 nm node, T_{max} and temperature gradient are smaller than that for the 50 nm node due to the larger fraction of Cu in the inter-layer dielectric (ILD) layers. It should be noted that the total height of the (Cu + ILD) layers decreases as scaling continues, due to the smaller vertical dimensions of wires and insulators despite increasing number of metal levels. We also observed that T_{max} occurs around the long global wires, which are most prone to electromigration failures and give rise to highest RC delays.

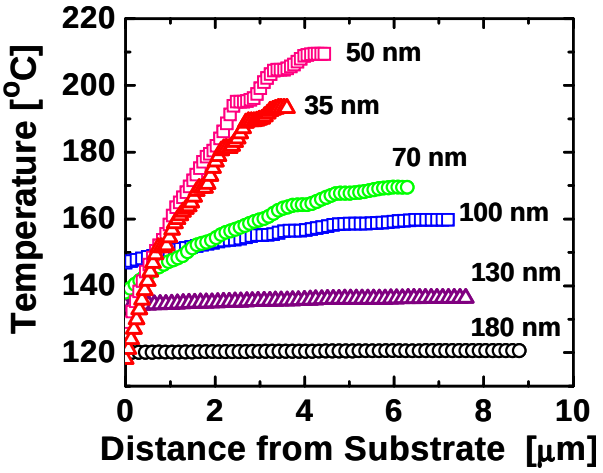


Figure 5: Simulated interconnect temperature distribution in vertical direction, from the upper surface of the silicon substrate to the top metal level for various technology nodes [8].

Prediction of hotspot temperatures and positions in interconnect and via systems is necessary for improving thermal design to minimize electromigration, stress migration, and high-current failures. While some thermal models are available for multilevel interconnect systems, the effects of vias are either neglected or treated very approximately. We have developed an analytical model [10] to evaluate the temperature rise within a via structure coupled with the interconnect line as a boundary condition using extended surface analysis. The simulation result indicates that hotspot locations and the overall temperature field in the interconnect structure are strongly affected by line and via dimensions, and thermal conductivity of metals and low-κ dielectrics. Via self-heating is negligible for vias with larger diameters, which contribute to lowering the average temperature of the interconnect due to their high thermal conductivities. In this case, the maximum temperature occurs at the center of the line. However, for vias with diameters below a certain critical value, the temperature at the end of the line is higher than that at the center, implying that a hotspot is formed within the via to satisfy the heat flow continuity requirement. Figure 6 is a simulated temperature field where a hotspot is shown formed within a 0.06 μm-diameter via.

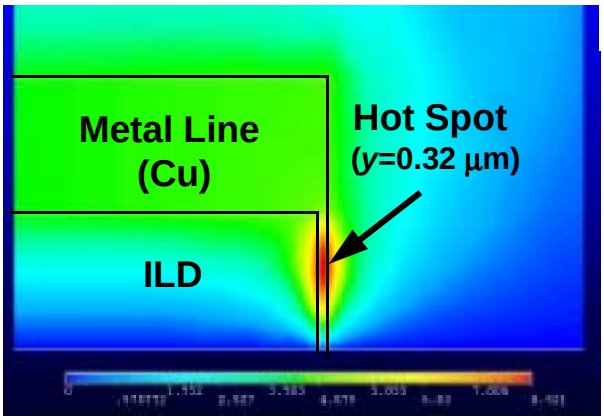


Figure 6: Temperature contour plot showing a hotspot formed within a via between two interconnect levels (line width=0.3 μm, via diameter=0.06 μm) [10].

Another important reliability concern is electromigration failure arising from void nucleation in Cu vias. Additionally, vias can also suffer from thermally-induced damage (due to melting) under high-current stress conditions such as electrostatic discharge. It is shown that design of vias based on ITRS specified maximum allowable currents for various technology nodes can severely compromise their reliability by underestimating chip-level thermal effects and current flow continuity in pitch matched vias, especially at the local interconnect tier [11]. Hence, it is important to carefully consider various effects including via resistance, via self-heating that determines effective via temperatures, and electromigration reliability, while formulating via design rules for nanometer scale interconnect technologies.

NOVEL THERMAL MICRODEVICES FOR INFORMATION STORAGE AND DIAGNOSTICS

Micro cantilever structures have been used for high-density thermomechancial data storage or surface modification [12]. Figure 7 schematically shows that a heated atomic force microscope cantilever (AFM) tip is in contact with and scans over a thin polymer film. Heat conduction along the cantilever tip induces thermomechanical formation of nanometer-size indentations in polymer. Joule heating induced by an electrical bias current from the cantilever legs and force from the cantilever tip causes the polymer to soften and flow, forming an indentation data bit of diameter below 50 nm. Erasing or modifying previously written indentations is possible by melting the region near a previously formed structure, shown in Fig. 8.

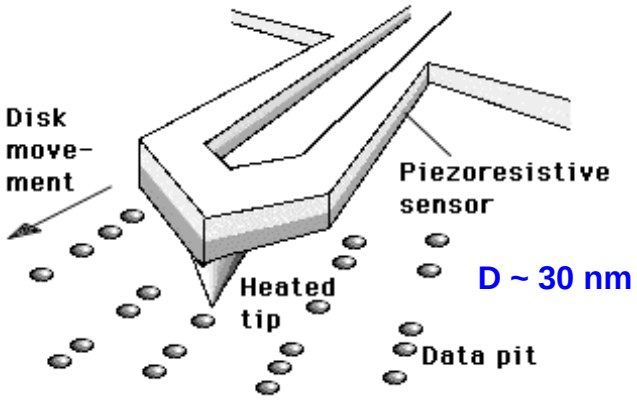


Figure 7: A schematic of atomic force microscope cantilever (AFM) tip for data storage or surface modification. This work was performed in collaboration with Gerd Binnig, Peter Vettiger, and coworkers of IBM [12].

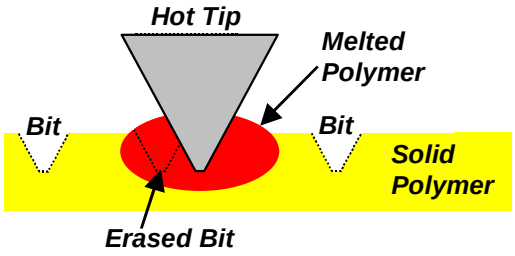


Figure 8: Thermal writing and erasing using the cantilever shown in Fig. 7 [12].

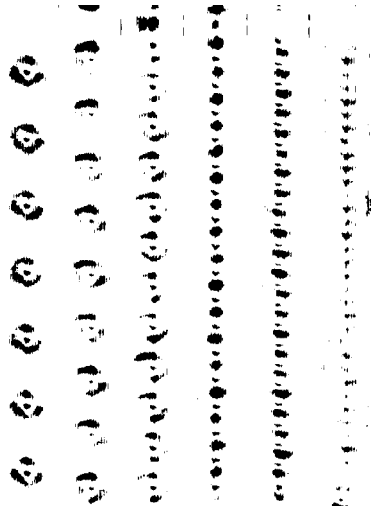


Figure 9: Tracks of thermally written indentations in a thin polymer layer, made using the cantilever shown schematically in Fig. 7. These are imaged using thermal feedback from the same cantilever running at a lower current. This work was performed in collaboration with Gerd Binnig, Peter Vettiger, and coworkers of IBM [12].

We have developed a thermal nanoimaging technique which measures vertical feature sizes by monitoring changes in the thermal impedance across the cantilever-polymer gap as the cantilever tip flows the contours of the writing structures. Indentations written with varying periodicity is shown in Fig. 9, made with thermal nanoimaging technique at 3 kHz and a lateral pixel spacing of 3 nm. The reading sensitivity of $\Delta R/R$ is 0.02 per vertical nanometer. The image indicates that heat transfer and polymer flow near the tip limit the packaging density of indentations, corresponding to data storage density limit of 0.9 Tbit in $^{-2}$. As the indentation periodicity increases, heat diffuses and melted polymer flows such that neighbor indentations are affected.

Solid immersion lenses (SIL) have been used to improve spatial resolution in variety of applications. This technique uses a lens held close to a sample to improve spatial resolution by a factor proportional to the refractive index of the lens. We have developed a 15 μm-diameter SIL from single-crystal silicon and integrated it onto a cantilever scanning [13]. A tip is fabricated opposite the lens to localize lens-sample contact. Figure 10 is a SEM imagine of the microfabricated Si solid immersion lens and cantilever with a tip. The integrated silicon cantilever is 30 μm wide, 3 μm thick and extends beyond the Pyrex handle wafer approximately 150 μm. The tip below the lens is typically 1 mm tall with a flat top 2 to 4 μm in diameter. The focus of the lens at the tip is approximately 3 μm below the geometrical center of the lens. The Root-mean-squared (RMS) deviation of the lens radius from the average value is less than 5%, and RMS surface roughness is estimated from the AFM scans to be less than 15 nm.

We investigated spot size, transmittance, and imaging capabilities of the Si SIL with CO_2 laser operating at λ=9.3 μm [14]. The Si SIL illuminated with a focused λ=9.3 μm can create a $\lambda/5$ spot with primarily reflection losses with an effective NA of 2.5. Power transmittance through the SIL is 10^3 times greater than that through a metal aperture giving equivalent spatial resolution. Figure 11 demonstrates that Si SIL can resolve two 1.0 μm holes separated by 3.0 mm with λ=9.3 mm light.

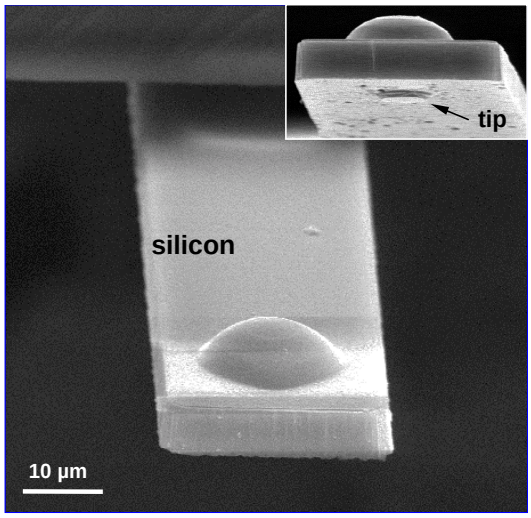


Figure 10: A SEM imagine of microfabricated Si solid immersion lens and cantilever with the tip. This work was performed in collaboration with Prof. Gordon Kino of Stanford University [13].

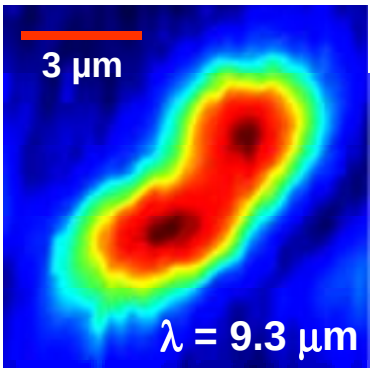


Figure 11: A scanning infrared imagine of two 1.0-μm holes separated by 3.0 μm with the Si solid immersion lens. This work was performed in collaboration with Prof. Gordon Kino of Stanford University [14].

TWO-PHASE MICROCHANNEL HEAT SINKS AND CHIP-LEVEL HOTSPOTS

Two-phase microchannel heat sinks are promising for VLSI chip cooling, in part because they can alleviate the impact of millimeter-scale chip hotspots. We developed measurements and modeling to determine the impact of a microchannel heat sink on cooling for a VLSI chip [15, 16].

Figure 12 shows a schematic of the microchannel heat sink to be analyzed. Heat is dissipated from the top surface while a glass layer insulates the bottom. The heat flux q'' is assumed to vary only along the channels in z direction, and $\dot{m}$ is mass flow rate of water in the channels. A time- and space-averaged one-dimensional conjugate conduction-convection heat transfer analysis is applied to only one channel, and the equations are:

Solid: $$\frac{d}{dx}\left(k_s A_s \frac{dT_s}{dx}\right) - \eta_0 h_0 p\left(T_s - T_f\right) + q'' w = 0, \quad (1)$$

Fluid: $$\dot{m}\frac{di_f}{dx} = \eta_0 h_0 p\left(T_s - T_f\right). \quad (2)$$

where T_s and T_f are the average local temperatures of the solid wall and the fluid, respectively, and i_f is the specific fluid enthalpy. The thermal conductivity of solid is k_s, A_s is the solid cross-sectional area, p is the perimeter of the microchannel cross section, and w is the pitch of the microchannels. The forced convection coefficient for heat transfer between the solid wall and the working fluid is h_{conv}, and η_0 is fin effectiveness η_0. Eq. (1) accounts for conduction along the heat sink and heat transfer rate from solid to liquid, while Eq. (2) indicates change of flow enthalpy due to heat convection from the wall to the fluid. Liquid and vapor phases are assumed to be in equilibrium at the saturation temperature and pressure. h_{conv}, and the pressure drop are evaluated from a correlation for a rectangular channel of a given aspect ratio for liquid flow. For the two-phase flow, Kandlikar's correlation is employed to calculate h_{conv}, and the pressure drop is calculated using a homogeneous flow model with the friction factor proposed by Stanley et al. [15]. Finite volume element is used for the numerical simulation with boundary conditions dictated by the heat losses to the packaging and temperature- and pressure-dependent properties of fluid.

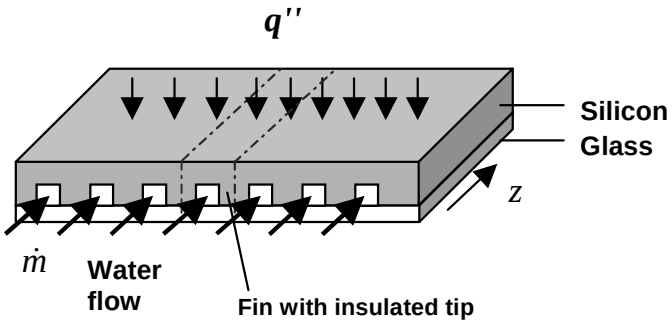


Figure 12: Schematic of a microchannel heat sink [15].

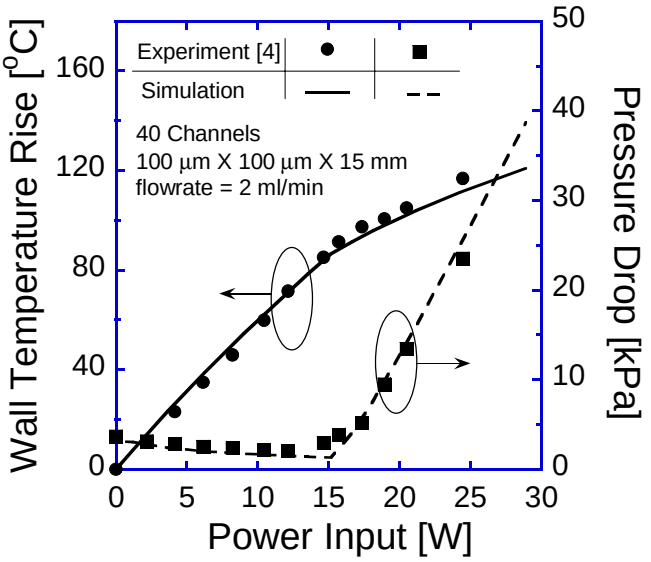
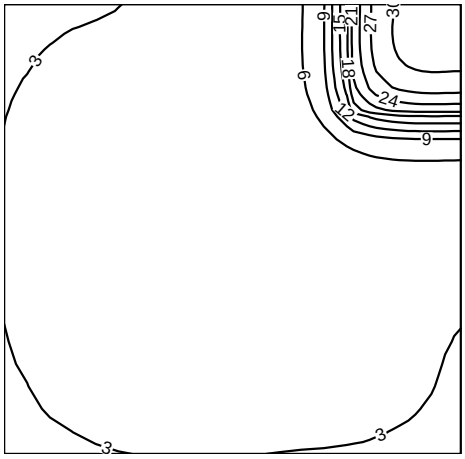


Figure 13: Comparison of numerical simulation with the experimental data for uniform heat generation. The overall heat sink dimension is 15 mm × 15 mm and the chip size is 11 mm × 11 mm [17].

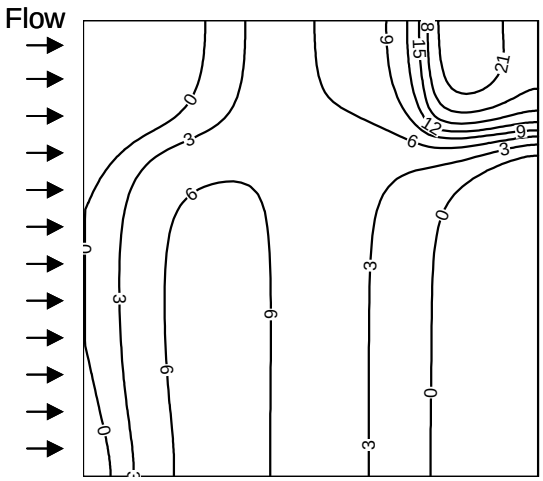
Figure 13 compares the calculated average wall temperature rise and the pressure of the multi-channel heat sink with the measurements of Jiang et al. [17] under uniform heating conditions. The reasonably good agreement provides support for the convection correlation and the homogeneous flow model used for two-phase flow.

The present model and ANSYS are used to evaluate the thermal performance of a microchannel heat sink and a conventional heat sink under a localized junction hotspot [18]. The hotspot is localized at the upper corner are a of 5 mm × 5 mm of a 20 mm × 20 mm chip with a power of 50 W, while the power in the rest of the chip is 100 W. A copper heat spreader with dimensions of 40 mm × 40 mm × 1.5 mm is used to simulate the conventional heat sink. The simulated microchannel heat exchanger, with dimensions of 30 mm × 22 mm × 1.0 mm, consists of 25 microchannels with depth of 300 μm and length of 20 mm. The channels at the hotspot region are 700 μm wide while they are 450 μm wide at the rest of the chip. Water flows through the channels with a flowrate of 20 ml/min and an inlet temperature of 69 °C. The exit fluid pressure is set to 0.31 bar such that phase change occurs at about 70 °C with an exit fluid quality of 0.20.

Figure 14 illustrates the contour plots of the temperature difference between the heat sink junction and its average surface, $(T_j - T_{s,avg})$. The temperature gradient near the hotspot is greatly reduced with the microchannel heat sink. The maximum temperature difference between the junction and the averaged chip temperature is 9 °C lower with microchannel heat sink than that with a copper spreader. The results indicate that a microchannel heat sink can yield far better temperature uniformity than a copper spreader.



(a) Conventional fin heat sink ($T_{j,max}$ - $T_{s,avg}$ = 32 °C)



(b) Microchannel heat sink ($T_{j,max}$ - $T_{s,avg}$ = 23 °C)

Figure 14: Contours of temperature difference ($T_j - T_{s,avg}$). The temperature difference between adjacent contour lines is 3 °C [18].

Microjet impingement cooling is another advanced cooling technology for high heat flux removal. Past research on microjet impingement studies use air as the working fluid, which offers relatively low heat removal rates. Two-phase microjets impingement has been most recently studied because low thermal resistances and high heat transfer coefficients can be achieved due to the thin boundary layer at the chip surface.

We have investigated heat removal capability of microjets impingement using microfabricated single- and multi-jet arrays [19]. The jets, formed using Deep Reactive Ion Etching in silicon substrate, have diameters ranging from 30 to 100 μm with a length of 300 μm. Heater and thermometers are integrated in a heater chip to emulate a high power IC and to measure one-dimensional temperature profiles along the chip surface. The jet chip is bonded to the heater chip to enclose the fluid and to allow for integration of these devices into a closed looped cooling system [17]. Figure 15 shows a schematic of the confined jet test device. Experiments are conducted with water flow rate and pressure necessary for jet formation. Figure 16 plots the temperature profile on the chip surface using a four-jet array at a flow rate of 8 mL/min. The result demonstrates that jet-array impingement significantly reduces chip temperature, and achieves a uniform temperature profile on the chip.

Figure 17 compares measured average chip temperature using a single 76 μm-diameter jet and a four 76 μm-jet-array. Three distinct regions are evident in both single and multi-jet arrays as the power is increased: a linear temperature rise with increasing power in conventional single liquid-phase regime; a temperature plateau during two-phase regime when the latent heat is being utilized; and a sharp temperature rise due approaching the dry-out condition. Minimal superheating of 5 to 10 ° C is present from the data. The four-jet array configuration at 8 mL/min flow rate shows promising heat removal rates of over 90 W/cm^2.

Microjet impingement cooling is promising for the future of IC chip cooling. We are currently pursuing more studies in obtaining a detailed understanding of the jet flow at the exit of the orifice as well as in the stagnation plane. Detailed analysis of this heat transfer problem is also being modeled. This future work will allow for a better understanding of the system, as well as allow for optimization of heat removal of ICs using microjet impingement cooling.

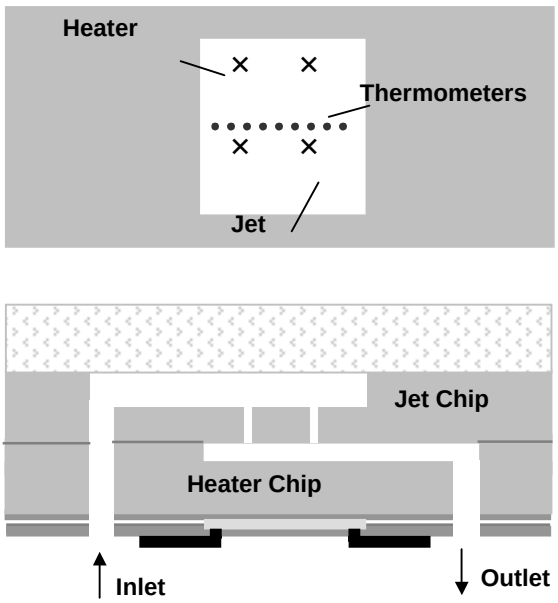


Figure 15: Schematic of a top and cross-sectional view of a confined microjet and heater test device. The crosses show the configuration using a four-jet array on top of a heated region of area 1 cm^2. This work was performed in collaboration with Prof. Thomas Kenny of Stanford University [19].

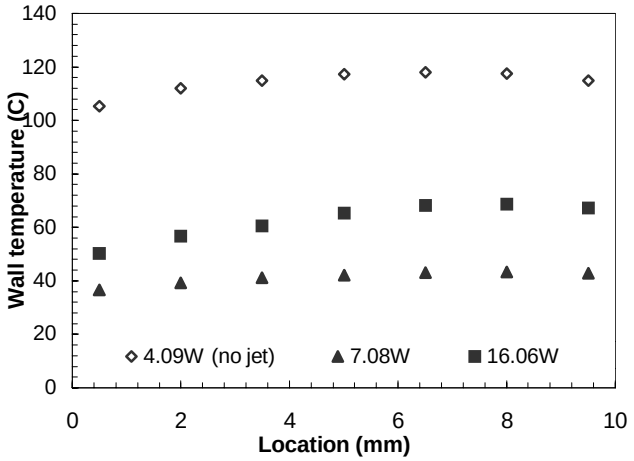


Figure 16: Temperature profile using a four-76 μm-jet array with a 6.9 psi pressure drop in the confined geometry. This work was performed in collaboration with Prof. Thomas Kenny of Stanford University [19].

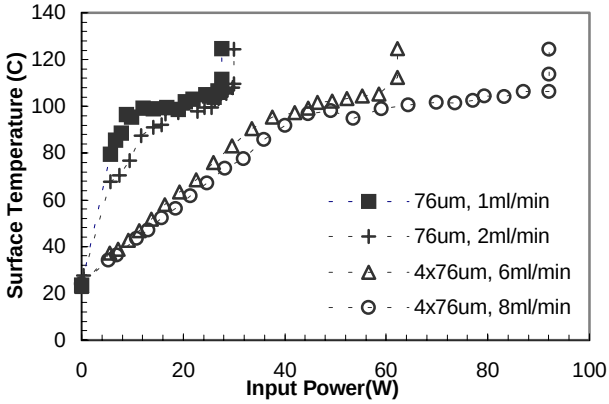


Figure 17: Average temperature as a function of applied power using a single-76μm-jet and a four-76μm-jet array. This work was performed in collaboration with Prof. Thomas Kenny of Stanford University [19].

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