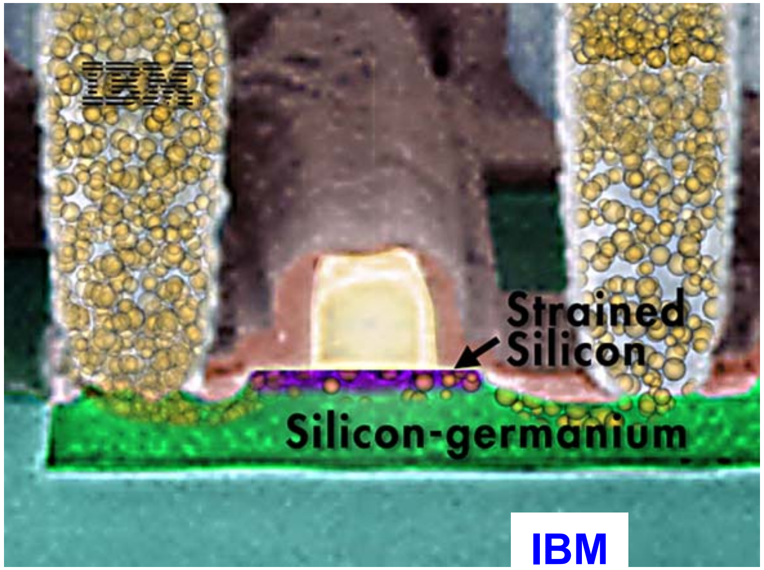
Microscale Thermal Engineering of Electronic Systems

Ken Goodson

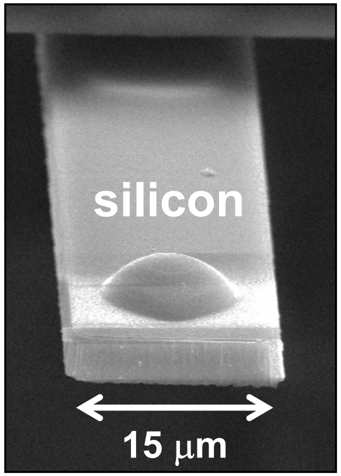
Thermosciences Division
Mechanical Engineering Department

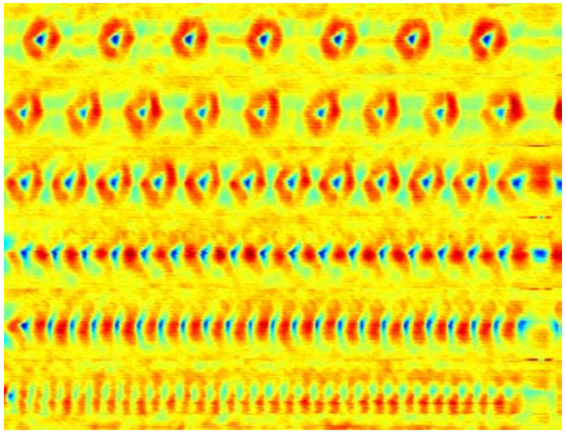
Stanford University

Key Points



1. Self Heating of Transistors and Interconnects

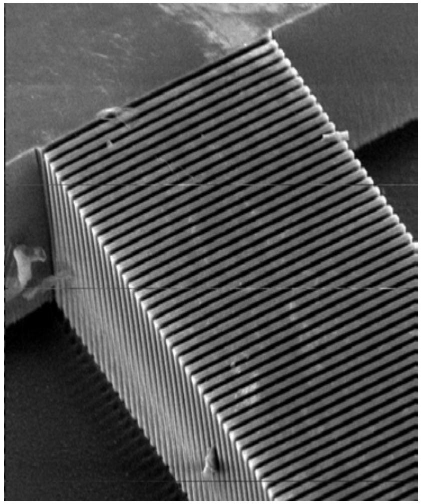




IBM Zurich / Stanford

2. Nanothermal Devices for Information Technology

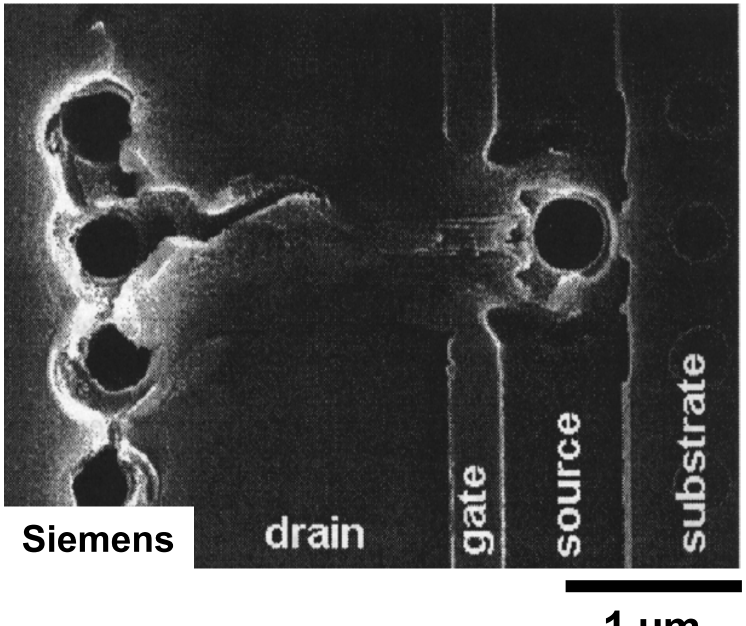
Solid-state EO pump



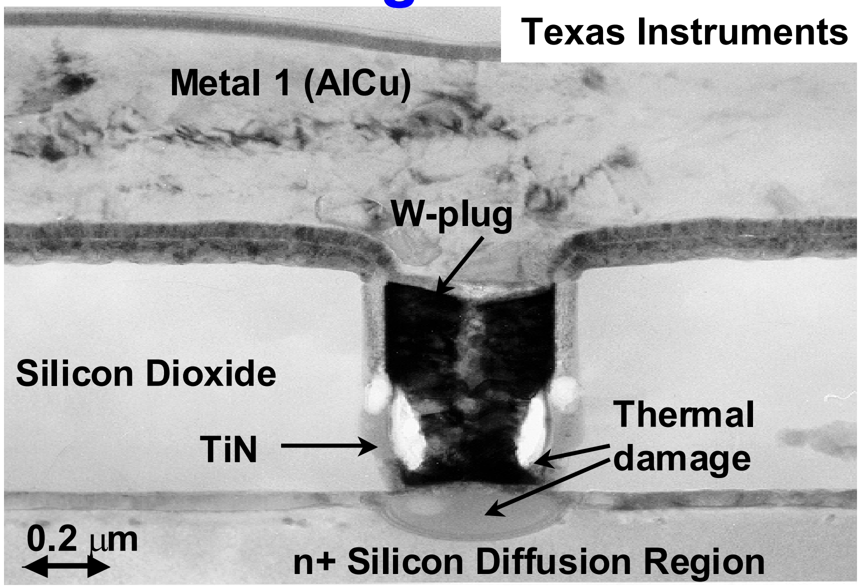
3. Microscale Technologies for Heat and Power Management

Microprocessor Thermal Challenges

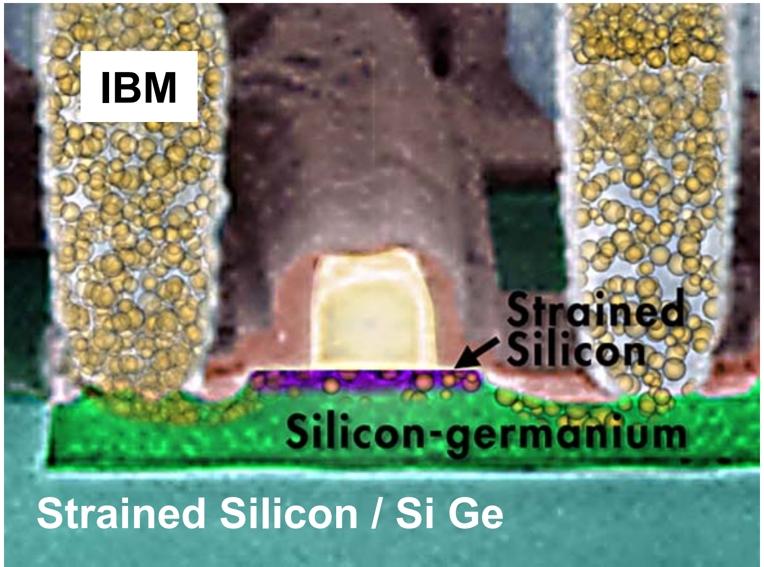
ESD



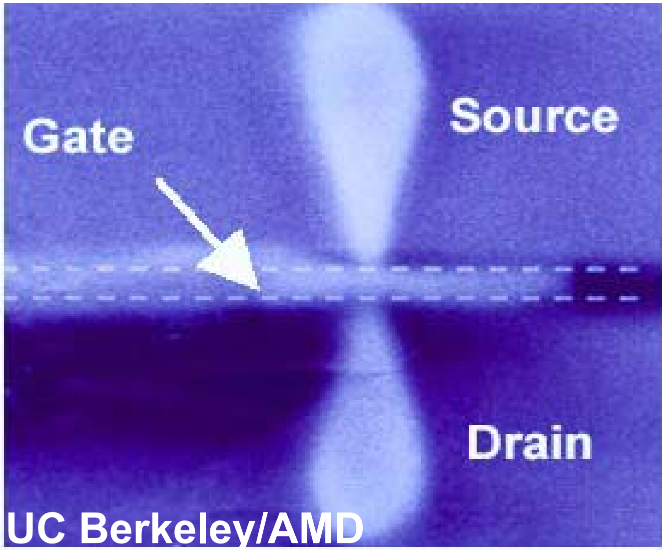
Metal Heating



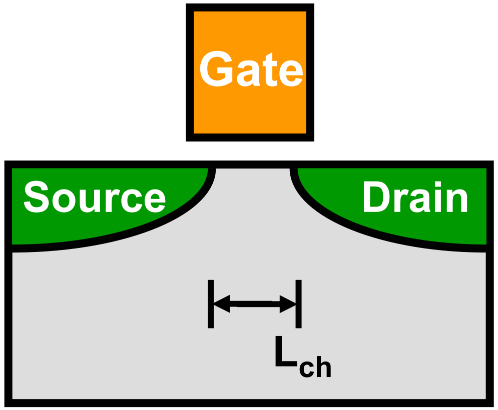
Novel Materials



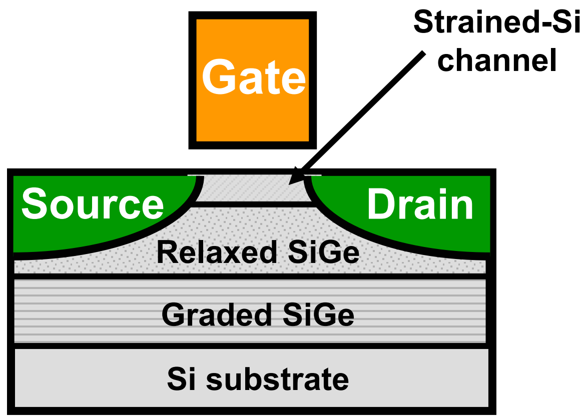
Novel Geometries



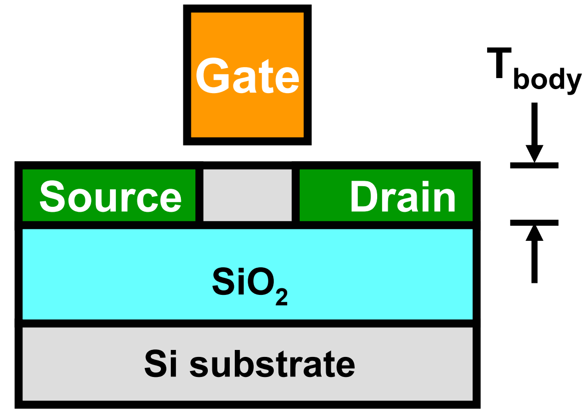
Nanotransistors



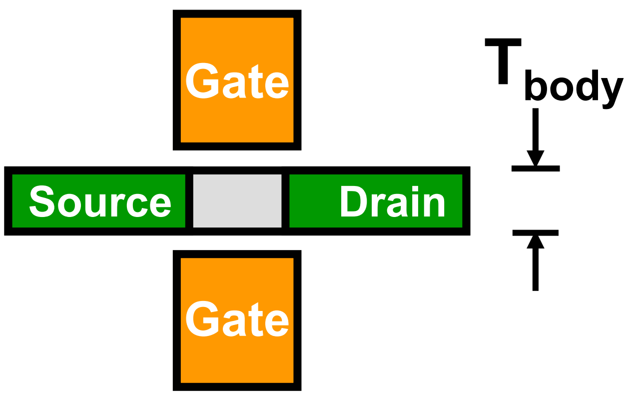
Classic Bulk FET



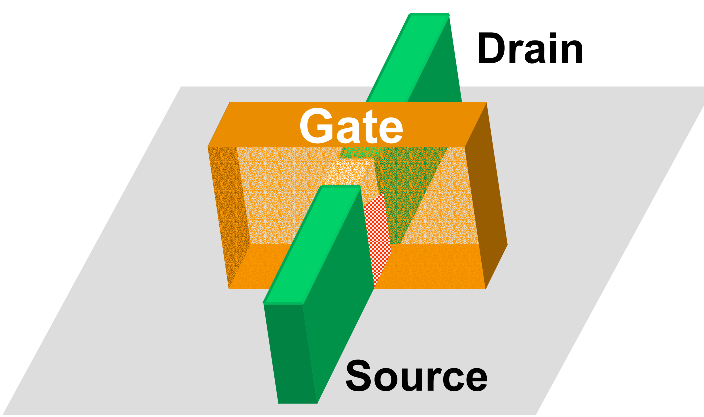
Strained-Si FET



Thin Body SOI

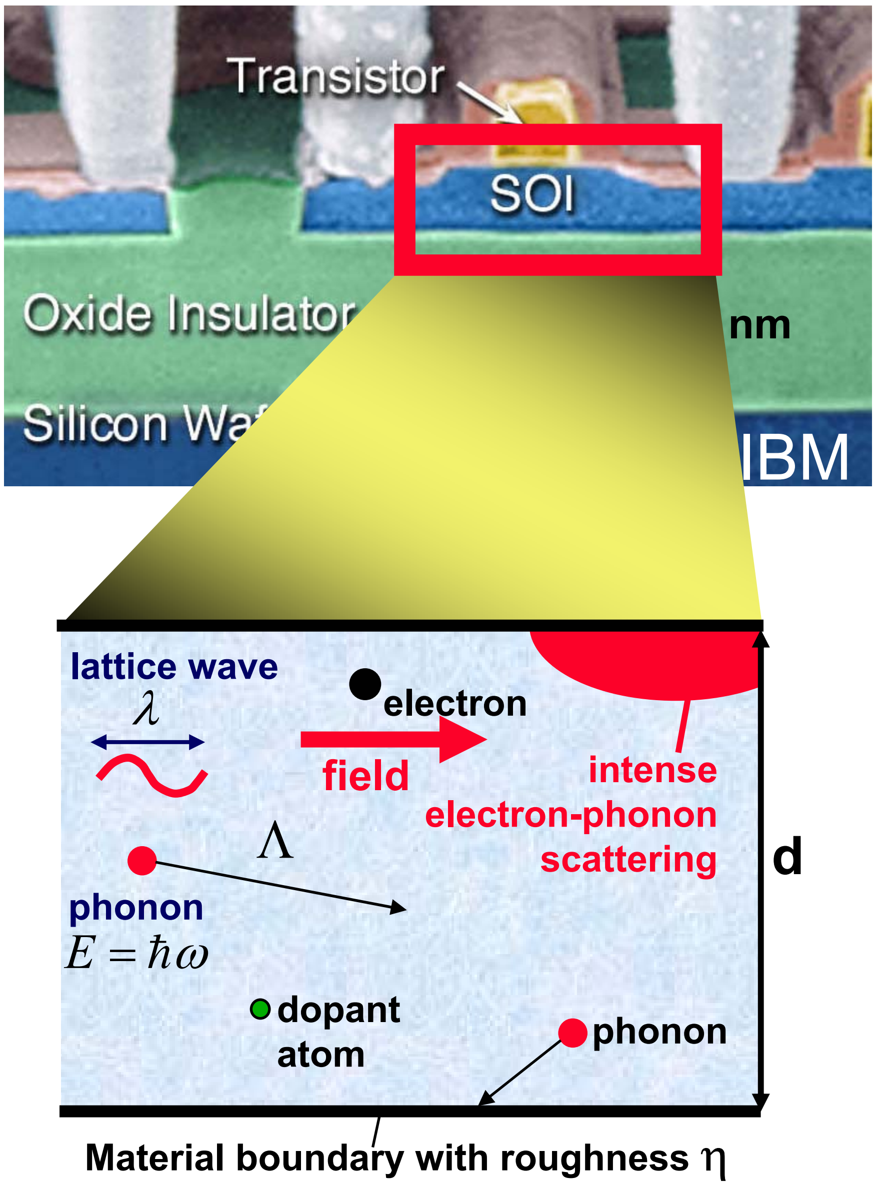


Double-Gate SOI
(Purdue, IBM)

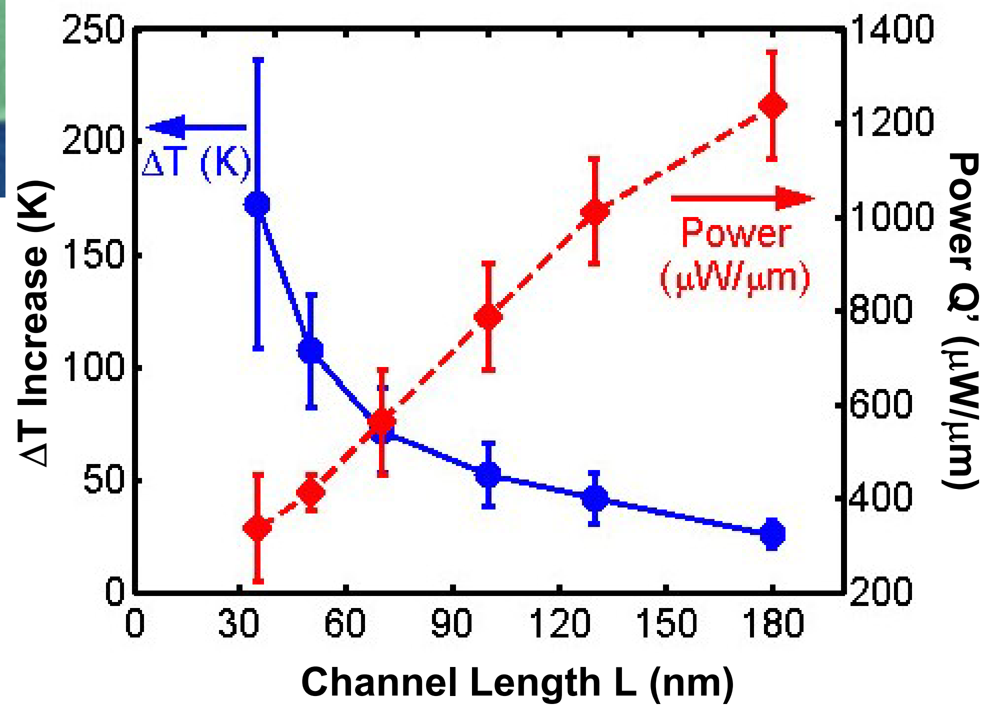


FinFET
(UC Berkeley, AMD, IBM)

Transistor Electrothermal Physics

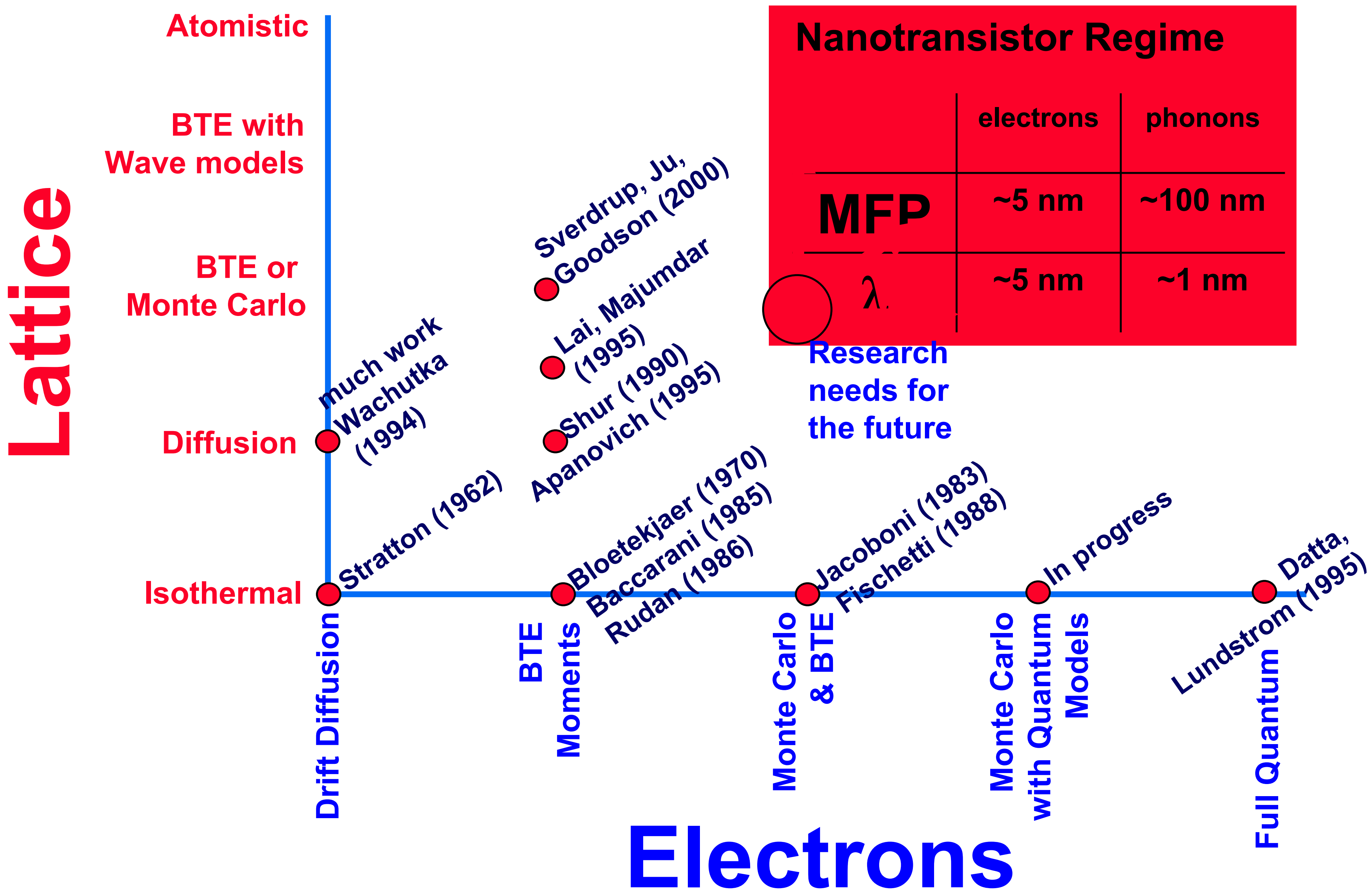


Approximate Impact of Device Scaling on Peak Phonon Temperatures



Pop, Banerjee, Dutton, Goodson,
Proc. IEDM 2001

Transistor Simulation Regime Map

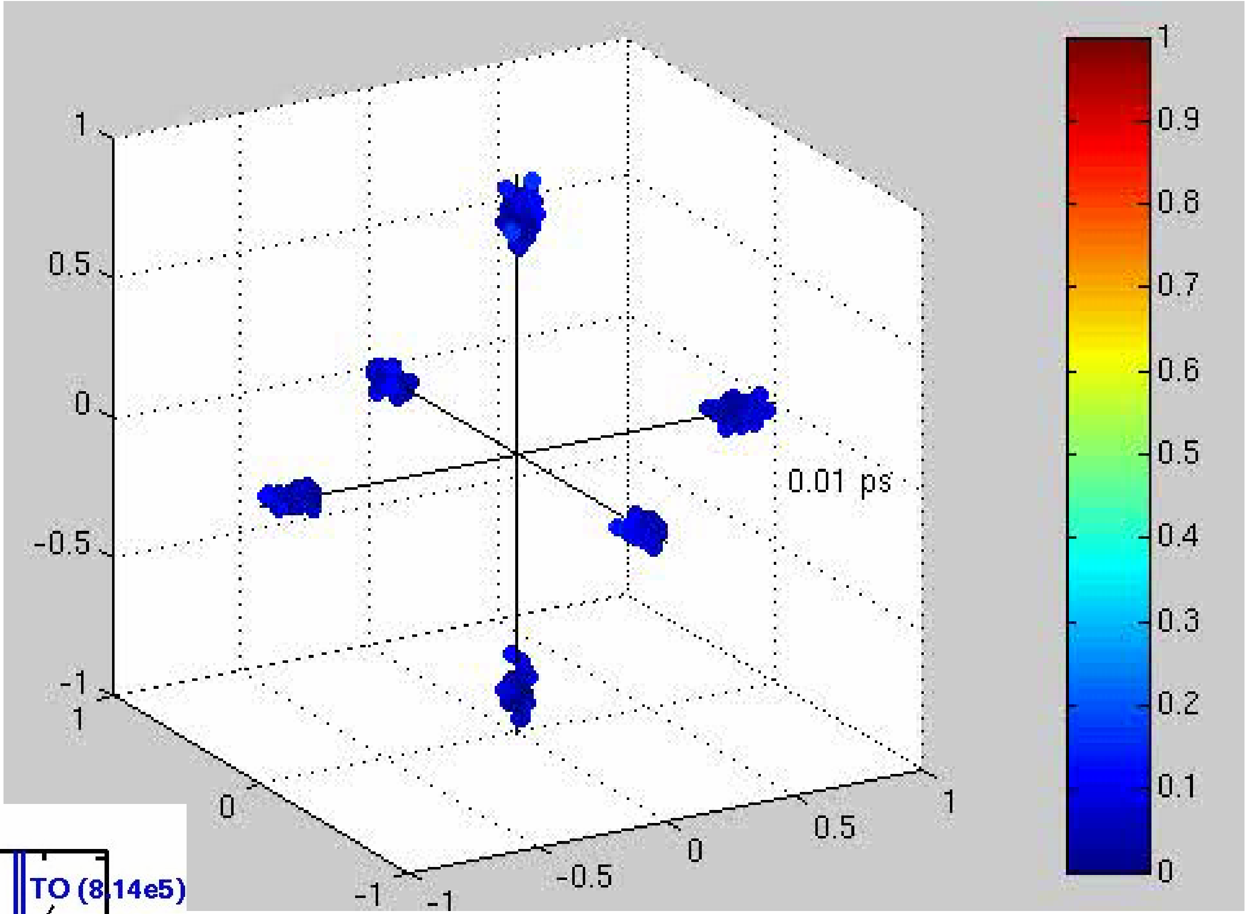


Nanotransistor Regime

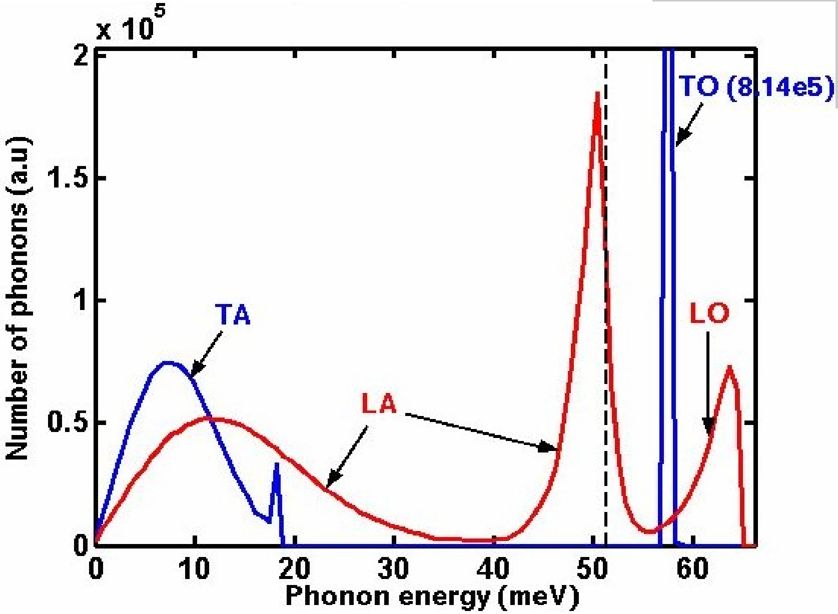
	electrons	phonons
MFP	~5 nm	~100 nm
λ	~5 nm	~1 nm

Electron Drift & Phonon Generation at 40kV/cm

Thesis work of Eric Pop, 2003



Phonon Emission

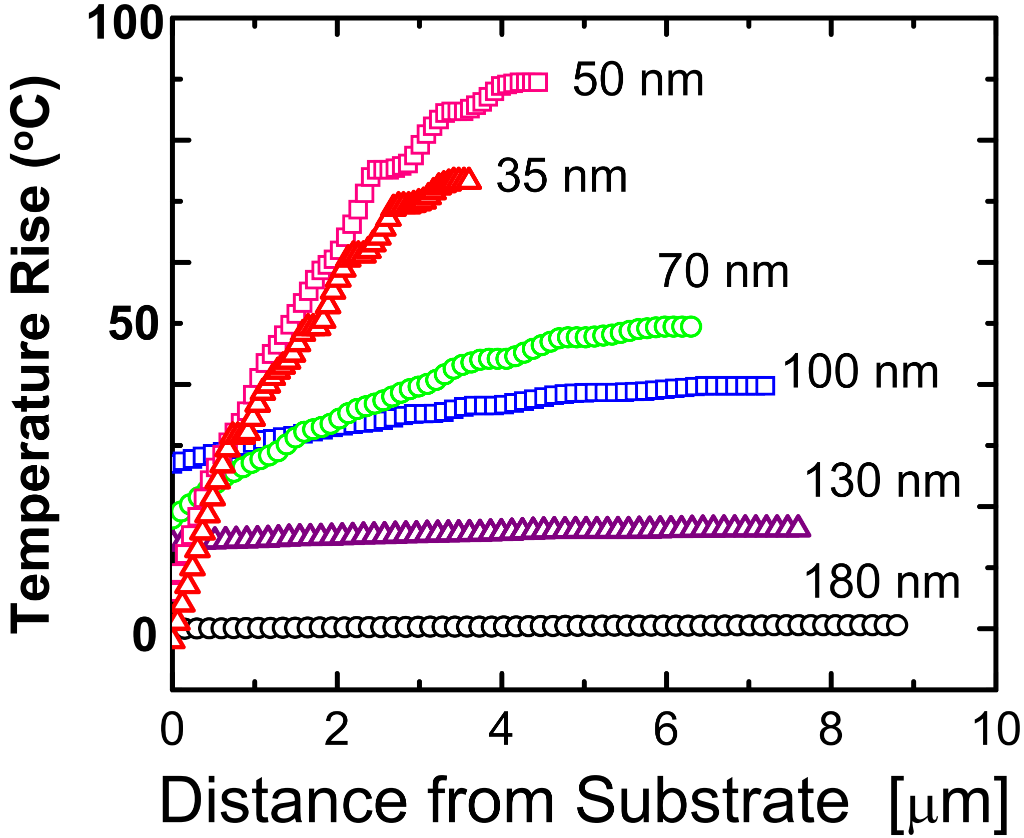


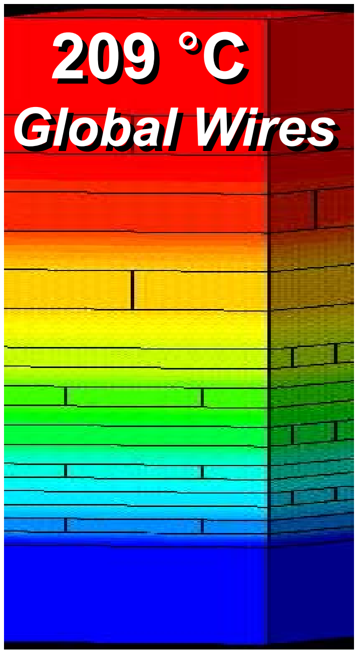
- Monte Carlo, 300 electrons at 300 K
- Electric Field starts at 0.5 ps
- E_{avg} jumps from 39 meV to 290 meV

Interconnect Thermal Management

Student: Sungjun Im. Sponsor – MARCO

Peak ΔT $\sim \overline{j^2}\, d_{MET} \rho_{MET} \frac{d_{ILD}}{k_{ILD}} \overline{\eta}\; N^{1.7}$





Temperature Contour Plot (50 nm technology node)

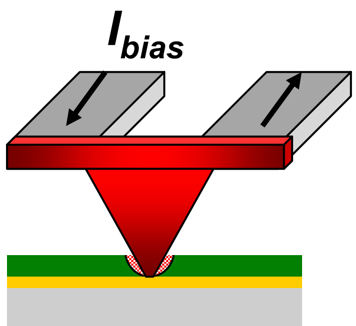
The temperature rise in interconnects is small now, but compounding trends in the ITRS roadmap lead to a tremendous increase at the 70 nm node beyond

- low-k dielectric materials
- increasing current densities and aspect ratios
- increasing number of interconnect layers

Nanoscale Thermal Data Storage

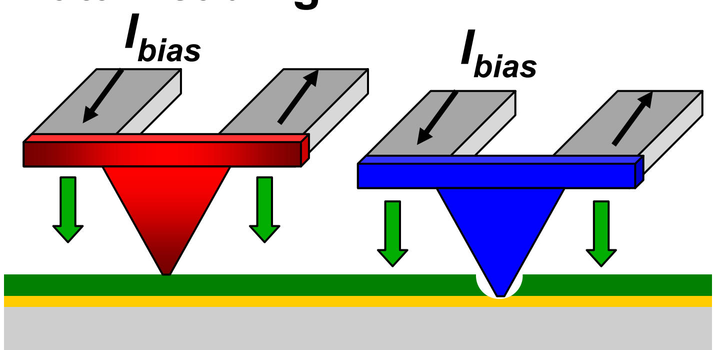
IBM Zurich: Vettiger, Binnig Stanford: King, Kenny, Goodson.
See King et al., Applied Physics Letters 78, 1300 (2001)

Data Writing



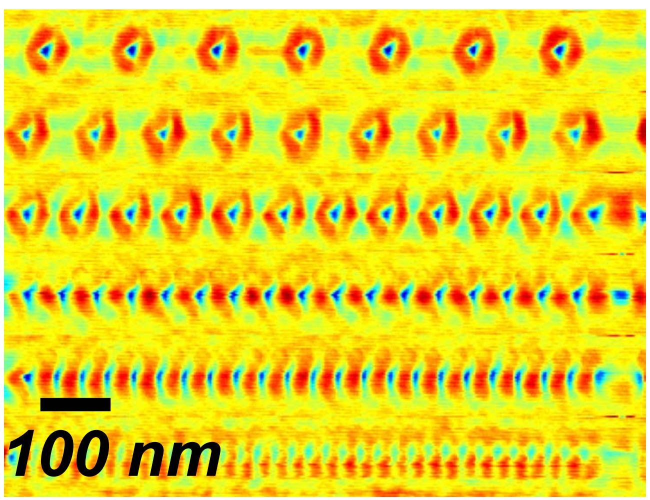
ΔT ~ 300 K

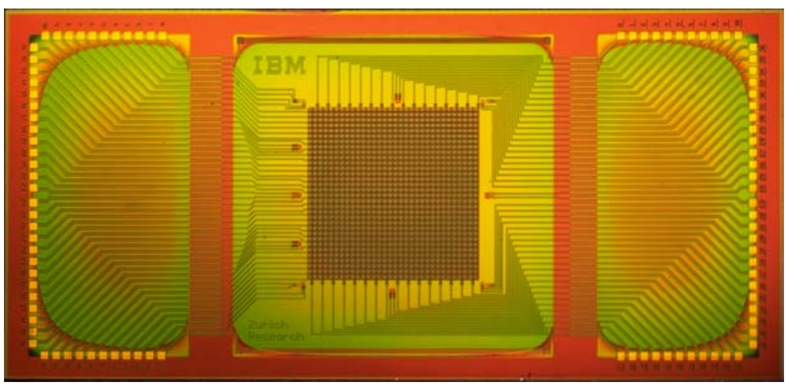
Data Reading



"0"
ΔT ~ 5 K

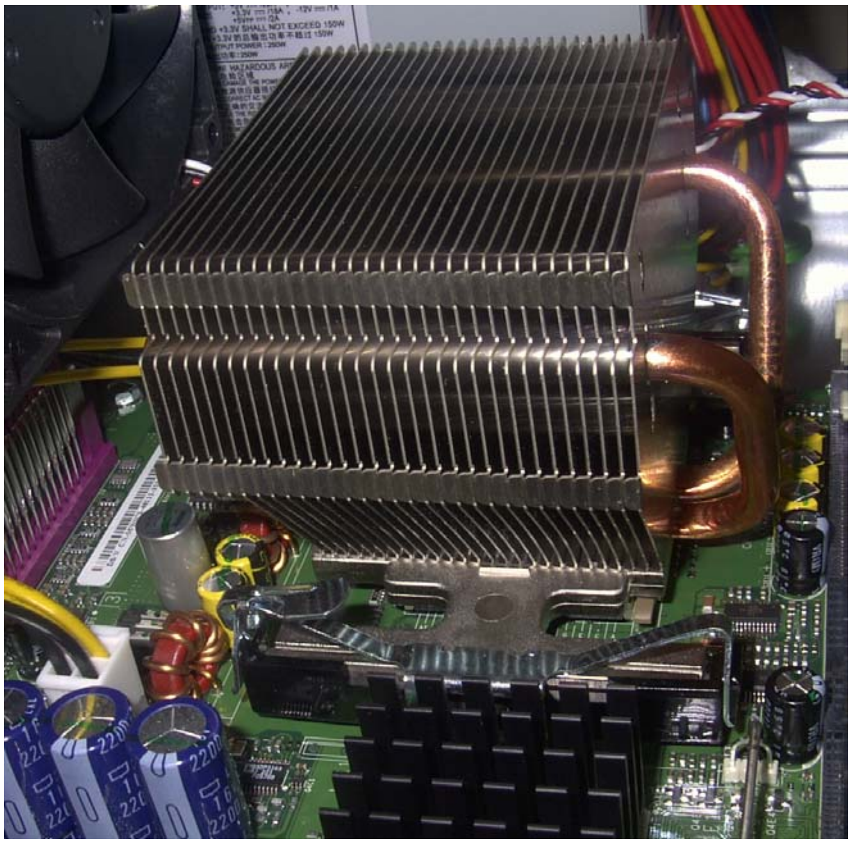
"1"
ΔT reduced

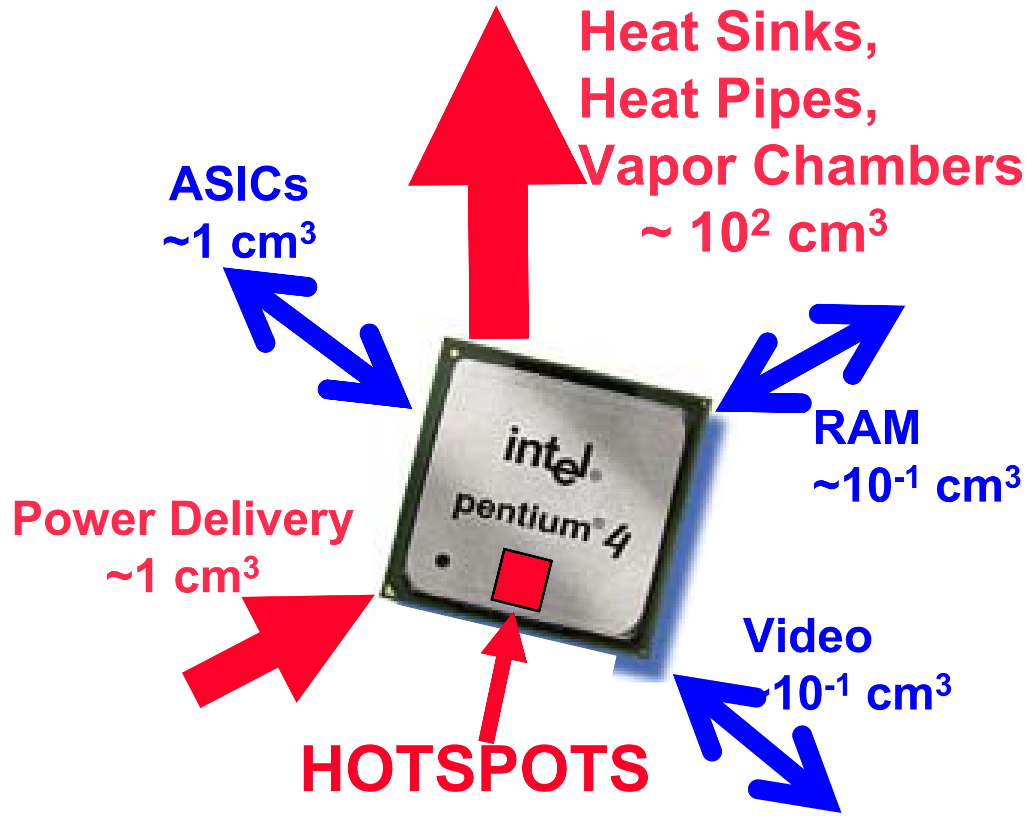




Cantilever Array

Microrocessor Thermal Management





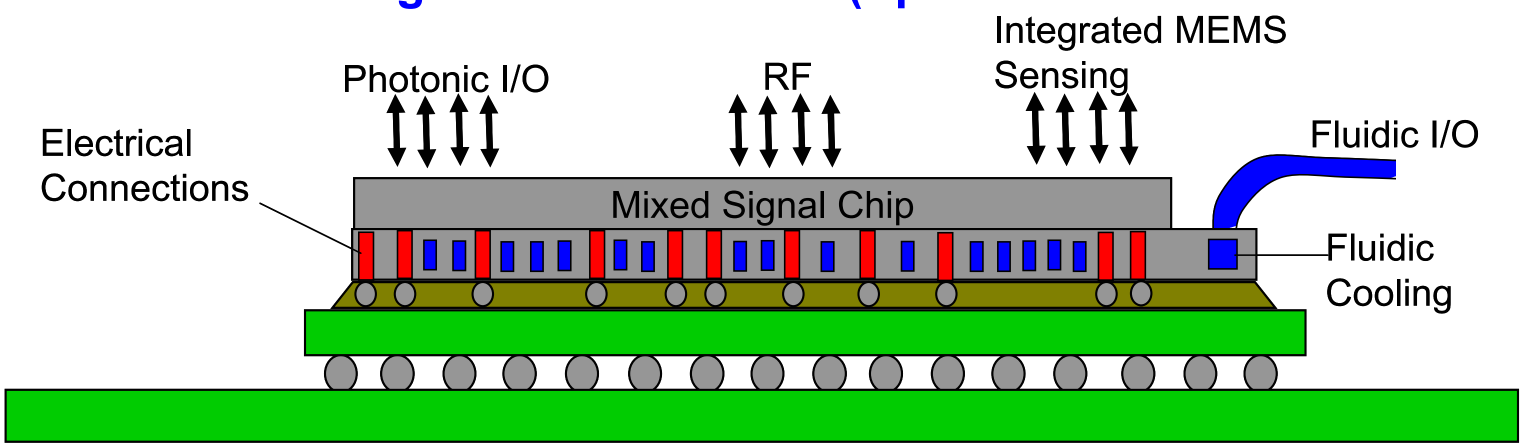
Microprocessor heat sinks are 3000 times larger and heavier than the chip

They crowd away power delivery components, ASICs, RAM, and Video

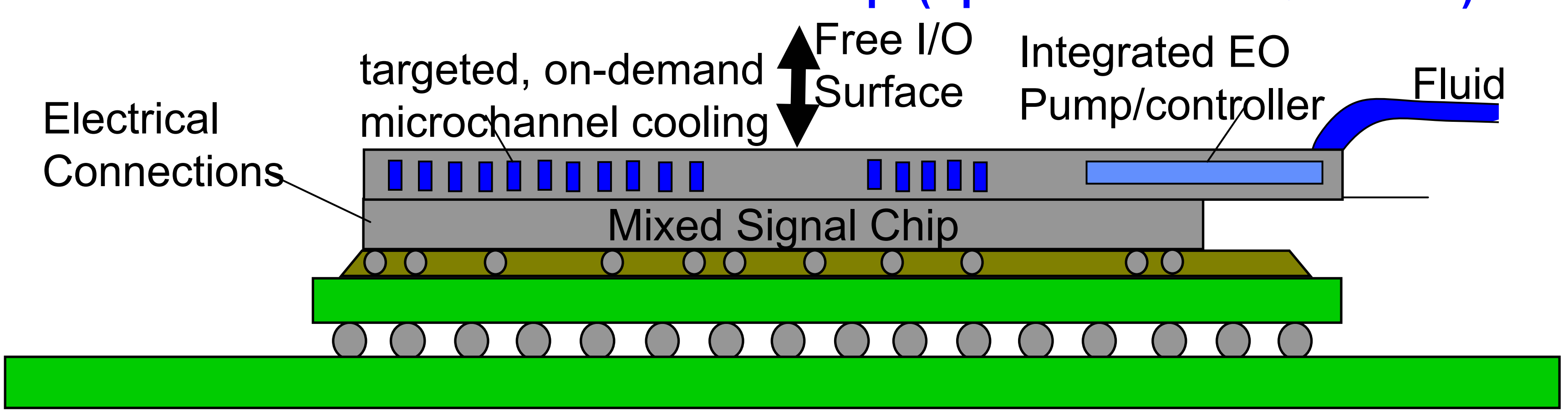
Interdisciplinary Grand Challenge: Integrated Power Delivery & Heat Removal

Groups of Goodson, Kenny, Santiago, Saraswat, Stanford Mechanical Engineering
Groups of Thompson & Troxel, MIT Materials and Electrical Engineering

Thermofluidic Mixed-Signal Power Module (Sponsors: SRC/MARCO & DARPA)



Thermofluidic Module with Solid-State Pump (Sponsors: Intel & DARPA)

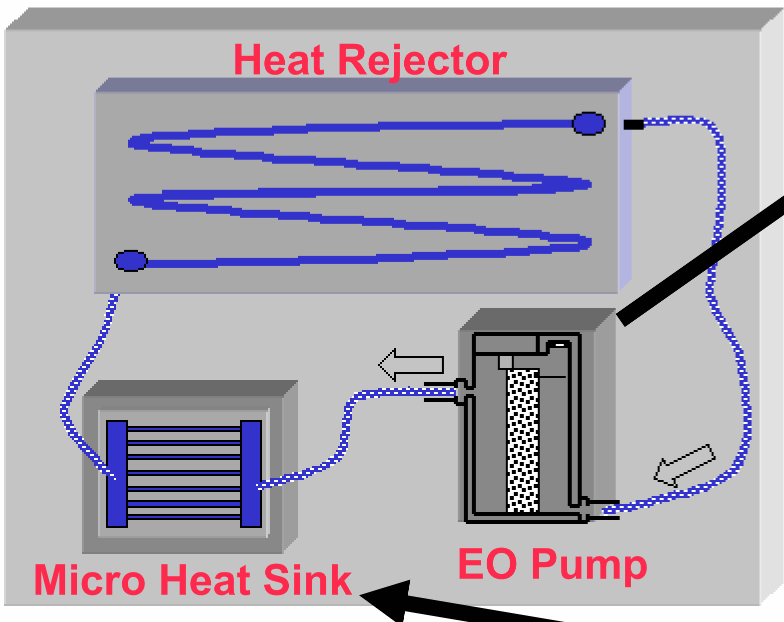


ElectroOsmotic Microchannel Cooler

Sponsors: DARPA, Intel, AMD, Apple. *Trans CPMT* (2002). Best Paper *SemiTherm* 2001
PIs: Goodson, Santiago, Kenny, Stanford ME

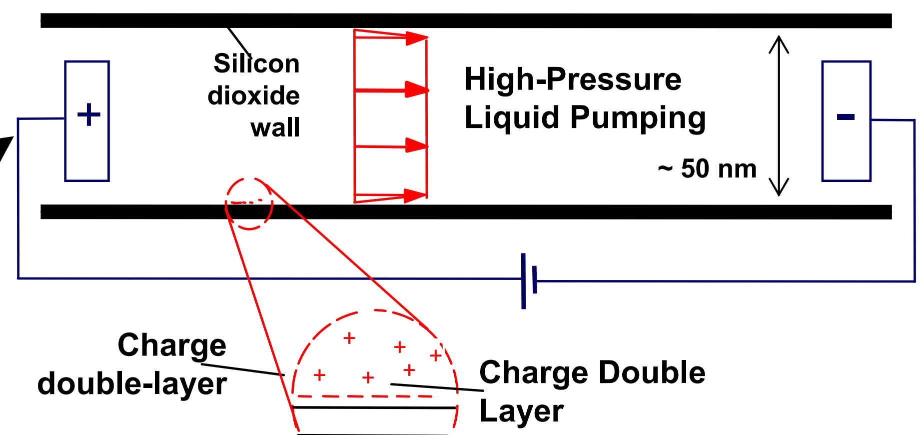
2001: 30 W Demo, 1 cm^2 (Intel)
2002: 100 W Demo, 1 cm^2 (Intel)
2002: 150 W Demo, 4 cm^2 (Intel)

2002: Laptop Demo
2002: Apple Dual Processor Demo
2003: AMD Demo

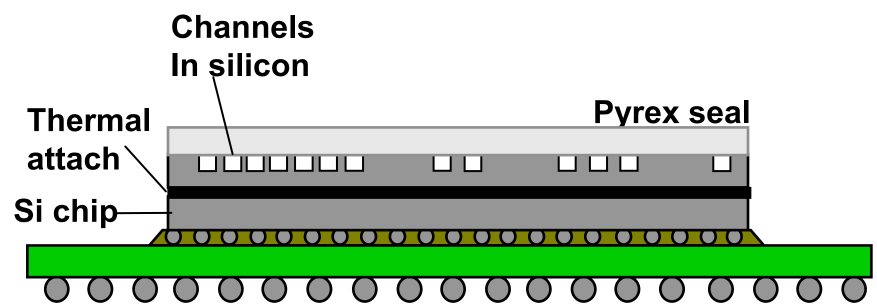


Stanford/Intel 100 W Demo
EO Pump Flowrate ~ 20 ml/min

ElectroOsmotic Pump



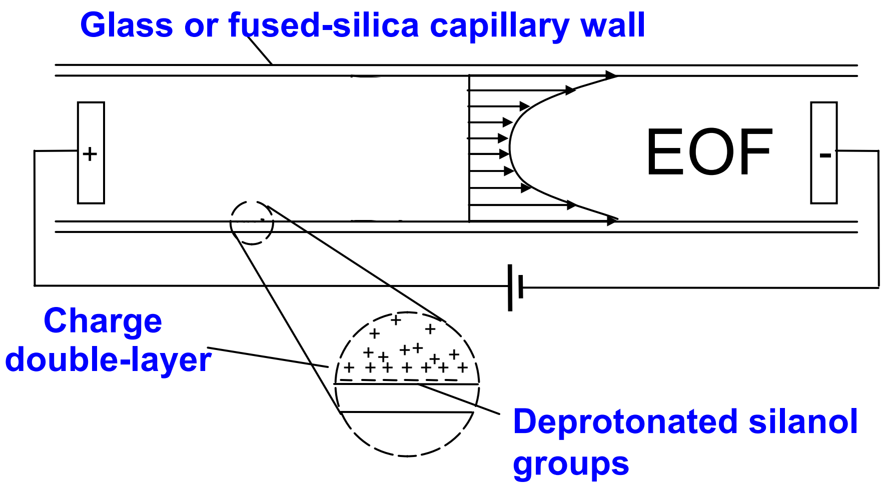
Microchannel Heat Sink

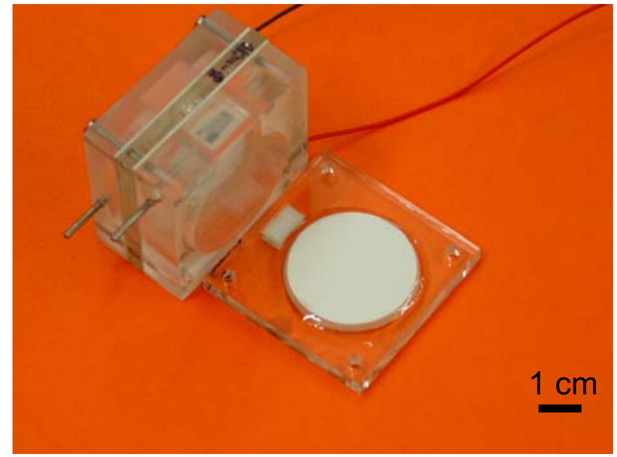


ElectroOsmotic Pumps

With groups of Santiago and Kenny, Stanford Mechanical Engineering
Sponsor: SRC/MARCO, DARPA

Idealized pore channel:





Free-standing pump

$$u(r) = \frac{\varepsilon\zeta E}{\mu} - \frac{dp}{dx}\frac{(a^2 - r^2)}{\mu}$$

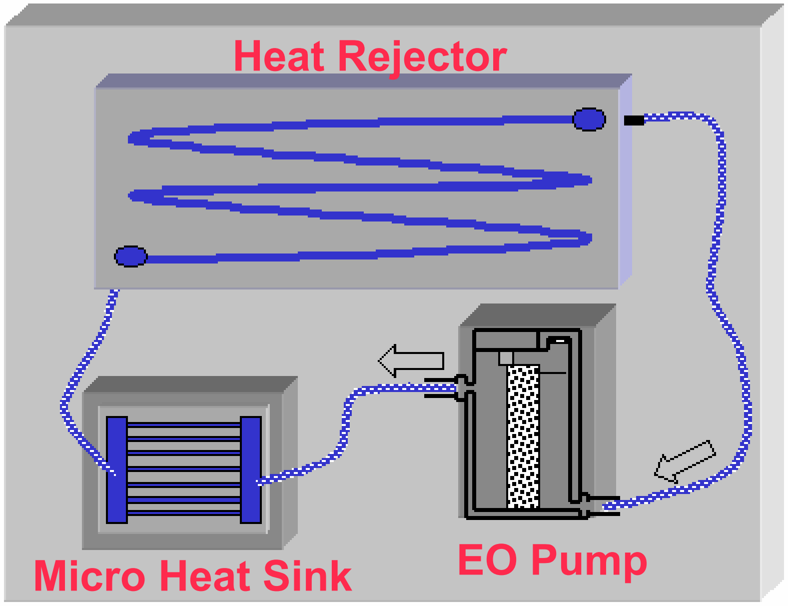
$$Q_{max} = \frac{\varepsilon\zeta}{\mu}\frac{VA}{l} \qquad \Delta p_{max} = \frac{32\varepsilon\zeta}{d^2}V$$

- **Very high volume to flowrate ratio**
- **Stanford pump performance (Feb 2002)**

P_{max} ~ 2 atm, Q_{max} ~ 40 ml/min, Vol. ~ 2 cm^3

2370 Charleston
Mountain View, CA 94043
www.cooligy.com

Cooligy develops thermal management components based on electro-osmotic pumps and novel microscale heat exchangers



- *Founded in 2001 by Stanford Profs. Ken Goodson, Tom Kenny, Juan Santiago, Mechanical Engineering*
- *24 employees (Feb 2003) with engineering expertise including chemical, mechanical, packaging, thermal, & fluidic specialties*
- *Experienced management and directors drawn from Intel, Dell, Corning, Silicon Light Machines.*
- *Focussing on reliability demonstration, product implementation, collaboration with computer manufacturers*

Concluding Remarks

- The next decade of IC research & development will bring solutions to “secondary” challenges associated with Moore’s Law, such as power delivery, heat removal, and package integration.
- IC thermal management problems will have lengthscales spanning six orders of magnitude, from 10 nm in nanotransistors to more than 10 cm at the package level.
- Novel materials and geometries are increasing micro/nanoscale on-chip thermal resistances, leading to hotspots in metallization and interconnects.
- Circuit design focuses computation on the chip, yielding mm-scale hotspots that dramatically increase the thermal resistance from the chip to the package.

Goodson Microscale Heat Transfer Group

Thermosciences Division, Mechanical Engineering Department, Stanford

Current Students and Post-Docs (AY 2002/2003)

Dachen Chu (Physics)
Xuejiao Hu (ME)
Sungjun Im (Materials Science)
Kevin Ness (ME)
Jae-Mo Koo (ME)
Yue Liang (ME)
Angie McConnell (ME)
Eric Pop (Electrical Engineering)

Monikka Mann (ME)
Sanjiv Sinha (ME)
Evelyn Wang (ME)
Ankur Jain (ME)

Dr. Linan Jiang
Dr. Abdullahel Bari
Dr. Samuel Graham (Visitor from SNL)

Alumni (1999-2002)

Prof. Mehdi Asheghi	*Carnegie Mellon University (ME)*
Prof. Dan Fletcher	*UC Berkeley (Bioengineering)*
Prof. Bill King	*Georgia Tech (ME)*
Prof. Katsuo Kurabayashi	*University of Michigan (ME)*
Prof. Sungtaek Ju	*UCLA (ME) – with IBM until Fall 2003*
Prof. Kaustav Banerjee	*UC Santa Barbara (EE)*
Dr. Uma Srinivasan	*Xerox*
Dr. Per Sverdrup	*Intel*
Dr. Peng Zhou	*Cooligy*
Dr. Maxat Touzelbaev	*AMD*