

# MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

## 6.331 Advanced Circuit Techniques

Laboratory 3  
Phase Lock Loops

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In this lab you will investigate phase lock loop (PLL) operation using the CMOS 4046 integrated circuit. It contains two different phase detectors and a VCO. It also includes a zener diode reference for power supply regulation and a buffer for the demodulator output. The user must supply the loop filter. The high input impedances and low output impedances of the 4046 make it easy to select external components.

### Notes

1. This lab is complicated. Be sure that you understand how the circuits are supposed to work before coming into the lab. Do not try to build something that you have not fully analyzed. Read this entire assignment before beginning to work on it.
2. Data taken in Part 1 will be needed in order to complete your designs in the rest of the lab, therefore, do this part carefully.
3. Handle the 4046 with care. CMOS integrated circuits are easily destroyed. Avoid static discharges. Use a  $10\text{k}\Omega$  resistor to couple the signal generator to the PLL. Turn off the signal generator before turning off power to the 4046, or else you will power up the entire circuit from the signal input. Avoid shorting the outputs to ground or the supply. A TTL gate can withstand this kind of abuse, but CMOS cannot (be careful of loose wires). CMOS does not have the output strength to drive capacitive loads.  $V_{SS}$  should be connected to ground,  $V_{DD}$  should be connected to 5V, and pin 5 should be connected to ground (otherwise the VCO is inhibited).

## 1 VCO Operation

Read the circuit description in the datasheet. The VCO constant ( $K_O$  in radians/sec-volt) is the ratio of the change in operating frequency to the change in input voltage (on pin 9). Measure  $K_O$ , that is, graph the output frequency versus the input voltage. Be sure that your data covers the range from 5 kHz to 50 kHz. Make the measurements with various values<sup>1</sup> of  $R_1$ ,  $R_2$ , and  $C$ . Approximately, how is  $K_O$  related to  $R_1$ ,  $R_2$ , and  $C$ ? Measure the rise and fall times of the VCO output. Investigate the effects of capacitive loading.

## 2 Passive Loop Filters

The loop filter is placed between the phase detector output and the VCO input. This filter attenuates the high frequency harmonics present in the phase detector output. It also controls loop

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<sup>1</sup>UNDER NO CIRCUMSTANCES use  $R_1$  or  $R_2$  less than  $50\text{k}\Omega$ .

dynamics. Often a simple RC filter will function adequately. These designs avoid embarrassing level shifting and output limiting problems inherent in active filter designs. On the other hand, active filters may offer superior performance.

## 2.1 Phase Comparator II

Before continuing, consider the output of phase comparator II of the 4046. The output is a tristate device. This causes a reduction of the ripple when the loop is locked. Instead of a 50% duty cycle beat note at twice the fundamental, there is no beat note at all. Unfortunately, when one wishes to construct a block diagram for the loop,  $K_D$  is not well-specified. When either the upper or lower driver is on, the output looks like a voltage source, but when the output is floating, it is essentially a current source (a source of 0 amps). Therefore the value of  $K_D$  will depend on the specific filter. Consider Figure 1.

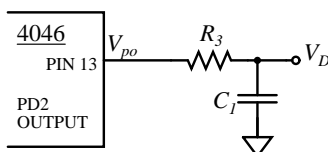


Figure 1: Phase comparator II output

So the phase comparator output is  $v_{PO} = +5V$  when the upper driver is on,  $v_{PO} = 0V$  when the lower driver is on, and  $v_{PO} = v_D$  when the phase comparator is in the open state. We can find the average value of the output:

$$\begin{aligned} v_{PO} &= (5V)\frac{\theta_e}{2\pi} + v_D(1 - \frac{\theta_e}{2\pi}) = v_D + (5 - v_D)\frac{\theta_e}{2\pi} & \text{for } \theta_e > 0 \\ v_{PO} &= (0V)\frac{\theta_e}{2\pi} + v_D(1 + \frac{\theta_e}{2\pi}) = v_D + v_D\frac{\theta_e}{2\pi} & \text{for } \theta_e < 0 \end{aligned}$$

Note that the value of  $K_D$  depends on the value of  $v_D$ . This makes the mathematics of the loop much more confusing. In fact  $K_D$  is different for positive and negative phase errors when  $v_D$  is not 2.5 volts. In order to get a usable output, we can modify the output to yield a fixed value of  $K_D$ . To do this we can put an active element in to define the value of  $v_D$  when the output is open. In both Figures 2 and 4 the open value is defined as 2.5 volts which leads to an equal value of  $K_D$  for positive and negative  $\theta_e$ . If you use phase comparator II with just an RC network, be sure to realize that the loop dynamics may be considerably compromised at extremes of lock range.

A simple second order PLL with “passive” loop filter is illustrated in Figure 2. Phase comparator II is used. When the loop is locked, the average phase detector output voltage is  $v_D = 2.5 + 2.5(\theta_e/2\pi)$  volts. The incremental phase detector gain constant is then  $K_D = 2.5/2\pi$  volts/radian. Consider the following specifications:

loop crossover frequency	$\omega_c = 1000$ rad/s
phase margin	$\phi_m = 45^\circ$
center frequency	$f_O = 19$ kHz
phase detector	II

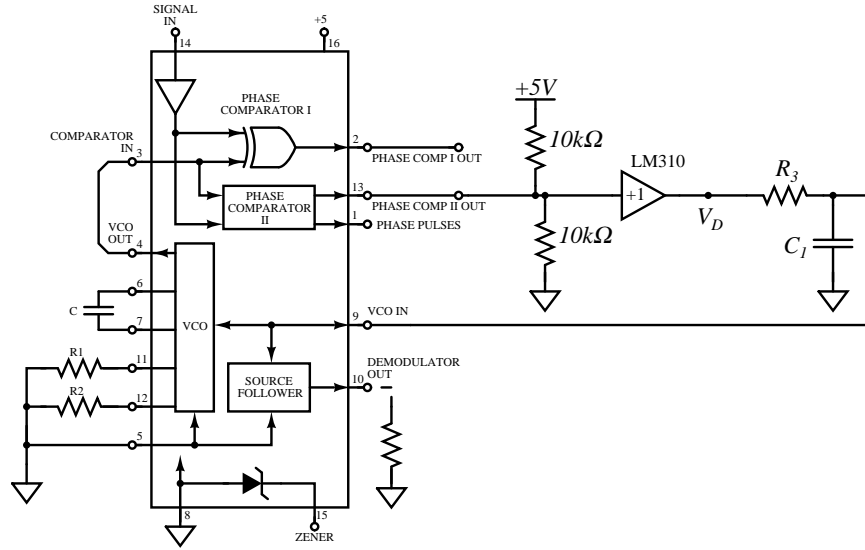


Figure 2: “Passive” loop filter

Where we define the center frequency,  $f_O$ , as the VCO output frequency when pin 9 is 2.5 volts. Using the topology illustrated in Figure 2, design and build a circuit that meets these specifications<sup>2</sup>.

Document your design with block diagrams and Bode plots of the magnitude and angle of the loop transmission. What is the steady state phase error and lock range? How do your predictions and measurements compare?

The phase margin of the loop may be deduced from measurements of the step response of the loop. One technique is to apply a FM signal to the input and look at the demodulated output. Specifically, use a square wave to modulate the frequency of the function generator which you are using for your input<sup>3</sup>. Observe the VCO input voltage. Measure the risetime and peak overshoot. Are these results compatible with a second order system with the specified crossover frequency and phase margin? NOTE: the frequency deviation should be very small so that the PLL does not break lock.

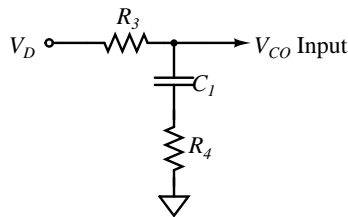


Figure 3: Lag loop filter

The loop filter is replaced by the lag network illustrated in Figure 3. It will allow you to set  $K_O$  and  $\omega_c$  independently. Hence, the loop may have a wide lock range (as determined by  $K_O$ ) and

<sup>2</sup>Hint: let  $R_3C_1 = 1$  ms. Then  $C$  and  $R_1$  are chosen to set  $K_O$ , while  $R_2$  determines  $f_O$ .

<sup>3</sup>If frequency generators are in short supply, consider using the VCO from another 4046.

a narrow bandwidth. Design and build a circuit to meet the following specifications:

loop crossover frequency	$\omega_c = 1000$ rad/s
phase margin	$\phi_m = 45^\circ$
center frequency	$f_O = 19$ kHz
lock range	9 kHz to 29 kHz
phase detector	II

Include the appropriate Bode plots.

The lag filter does not provide much attenuation of the high frequency ripple from the phase detector. This is evident when you observe the voltage at the VCO input (pin 9). Place a capacitor across  $R_4$  in order to increase the high frequency attenuation. If this pole is placed beyond the loop crossover frequency, there will be negligible change in the FM step response, except that the high frequency teeth will be removed.

Now try increasing the FM frequency deviation so that the loop breaks lock. Note the response at the phase comparator output and VCO input.

## 2.2 XOR Phase Detector

What happens if you substitute phase comparator I (an exclusive-or gate) for phase comparator II in the lag compensated PLL described in Part 2.1? You should be able to answer this question theoretically and experimentally. Specifically, what is the phase detector gain  $K_D$ , the loop bandwidth, the phase margin, the steady state phase error, the lock range, and the ease of acquiring lock (experimentally)?

Note: if you have difficulty in acquiring lock, try slowly scanning the input frequency until the circuit locks. Will this circuit lock on harmonics? Is the circuit duty cycle sensitive?

## 3 Active Filters

Return to the lag compensated PLL using phase comparator II as in Part 2.1. Apply a FM modulated input to observe the step response as before. Look at the output of the phase comparator (pin 13). The steady state phase error and dynamic tracking error should be apparent if you mentally average out the high frequency components<sup>4</sup>. Try varying the input frequency range.

Active filters are used to reduce this tracking error. A possible active filter PLL realization is illustrated in Figure 4.

Certain precautions must be taken when such filters are used. The opamp can easily supply voltages to the 4046 that will burn it out. For this reason, it is a good idea to diode clamp the inputs to the PLL as shown. The low pass filter ( $R_3$  and  $C_2$ ) provides extra attenuation of the high frequency phase detector ripple. It also should keep the opamp from slew rate limiting.

Again the active circuit specifies the open state output of phase detector II to be 2.5 volts. The inverter is necessary because the PLL wants a non-inverting topology.  $R_4C_1$  sets the crossover frequency, and  $R_2$  sets the zero location, hence the stability.  $1/(R_3C_2)$  should be set at least a

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<sup>4</sup>Note: If you find mental averaging unsatisfying, filtering  $v_D$  with a simple passive RC filter with  $RC = 0.1$  ms will give you a picture of the average value of the phase error. To avoid loading the phase comparator with a low impedance, make the resistor R a large value (1M $\Omega$  is fine). IMPORTANT: this filter is not in the loop, it is between the phase comparator output and the scope.

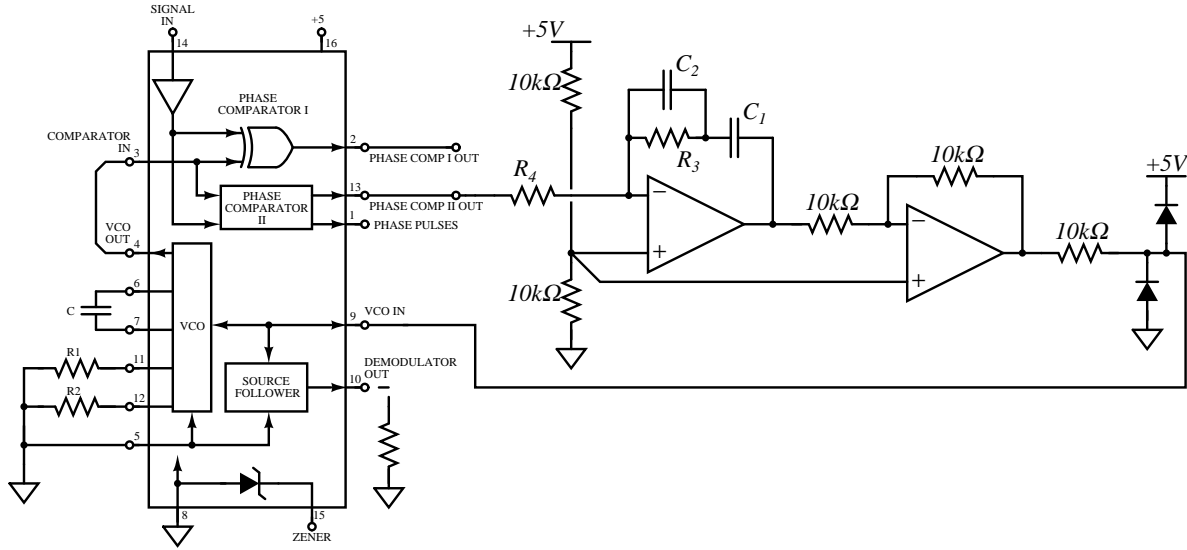


Figure 4: Active loop filter

factor of 5 above  $\omega_c$ .  $K_D$  is the same as before (as it would be for any loop filter which specified the open state volatage of the phase detector as 2.5 volts).

Feel free to design your own second order loop filter topology if you wish, just be careful not to destroy the 4046. Design and build a PLL using an active loop filter to meet the folowing specifications:

loop crossover frequency	$\omega_c = 1000 \text{ rad/s}$
phase margin	$\phi_m = 45^\circ$
center frequency	$f_O = 19 \text{ kHz}$
lock range	18 kHz to 20 kHz
steady state error	$e_{ss} = 0$
phase detector	II

Draw the appropriate Bode plots. Make measurements of the step response. Again look at the phase detector output (pin 13). What can you say about the dynamic tracking error? What about the steady state error?

## 4 Linear Phase Detectors and Frequency Synthesis

Consider the problem of trying to lock onto a signal in a composite mix of signals. The zero crossings of the composite signal may not coincide with the zero crossings of the signal you wish to lock to, thus the use of zero crossing sensitive phase detectors, such phase comparator II, or even XORs, is impossible.

We wish to use a linear phase detector that implements an analog multiplication of the composite signal and the VCO output. Since the VCO output is a square wave (a series of ones and minus-ones) we can relax our requirement to needing a multiplier that can multiply the incoming composite signal by either 1 or  $-1$  with minimal distortion.

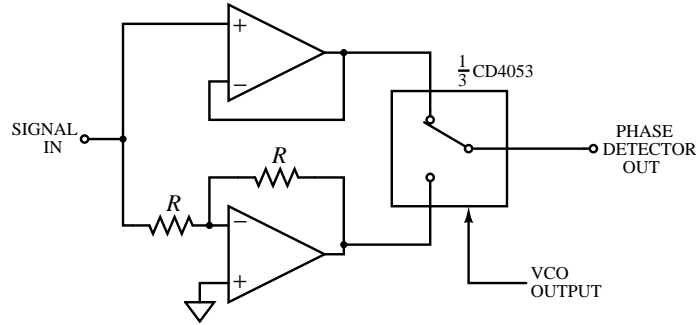


Figure 5: Linear Phase Detector

Consider the circuit in Figure 5. What is  $K_D$  for this phase detector? What will be the steady-state phase error for a zero output?

Note that  $K_D$  will depend on the amplitude of the incoming signal. For the rest of this lab, assume that the signal that we wish to lock to has an amplitude of 300 mV peak-to-peak.

Now, also consider the problem of wanting a VCO output frequency that is twice the input frequency. By putting a divide-by-two block in the feedback path as in Figure 6, the closed loop system should implement a multiply-by-two function.

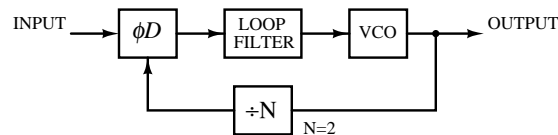


Figure 6: Multiply-by-two PLL

Design and build a circuit to meet the following specifications:

loop crossover frequency	$\omega_c = 100 \text{ rad/s}$
phase margin	$\phi_m = 45^\circ$
center frequency	$f_O = 38.0 \text{ kHz}$
lock range	18.5 kHz to 19.5 kHz
steady state error	$e_{ss} = 0$
phase detector	linear

Note that “zero steady state phase error” is not well defined for a frequency multiplier system. For our purposes, we define “zero steady state phase error” to be when the positive going transistions of both the input and output coincide. Using a D-flipflop (74LS74) implement a divide-by-two block in the feedback path of your PLL. Be sure to include its effects in your loop analysis. Note that if the phase detector has a steady state phase offset, you can compensate for this in your divide-by-two block. Phase shifts of  $\pm 90^\circ$  or  $180^\circ$  can be accomplished by mixing the input and output of the D-flipflop with the appropriate network of inverters and XOR gates.

Draw the appropriate Bode plots. Make measurements of the step response. Again look at the phase detector output (pin 13). What can you say about the dynamic tracking error? What about the steady state error?