

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.331 DESIGN LAB3: ANALOG-TO-DIGITAL CONVERTER

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## I. DISCUSSION AND DESIGN POINTS

I designed a dual-slope ADC for the slow but accurate specs with an auto-calibration cycle. The specs were as follows:

Resolution	12 bits
Conversion time	1 second
Power Supplies	+/-15V 1/2V accuracy
Temperature	25° +/- 10°C
Input Range	0 to 10 Volts
Source Impedance	1kΩ

For completeness, the basic operation of the dual-slope integrating ADC is shown in Figure 2. If the fixed integration time is  $\tau_1$  and the de-integration time is  $\tau_2$  then charge balance requires:

$$\frac{V_{in}\tau_1}{RC} = \frac{V_{ref}\tau_2}{RC} \quad (1)$$

which gives the dual-slop relation

$$\frac{V_{in}}{V_{ref}} = \frac{\tau_2}{\tau_1} \quad (2)$$

and it is independent of capacitor nonlinearity and even the values of the resistor and capacitor.

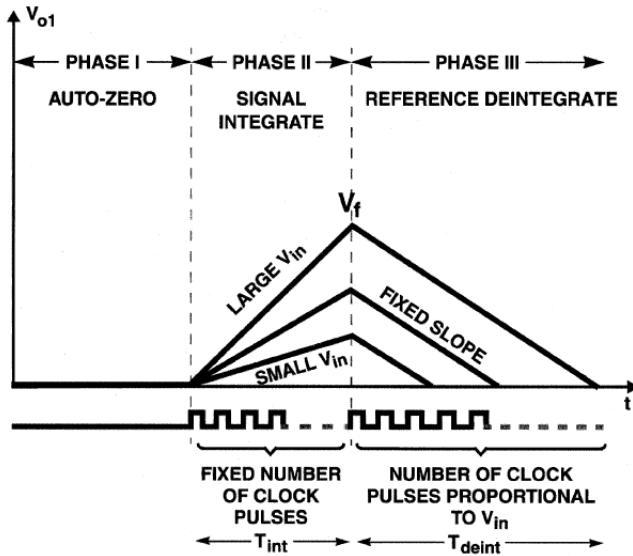


Fig. 2. The basic operation of a dual-slope ADC. First the input voltage is integrated for a fixed time. Then a negative valued reference voltage deintegrates. The total time is proportional only to the ratio of the input voltage and the reference voltage.[2]

The switching and timing logic to implement the auto-calibration cycle as well as the ramp timing for the integration would have been relatively complicated. Instead of spending a lot of my time on the digital logic, I just added a PIC which can be used later to interface the ADC with a PC. The full schematic of the dual-slope ADC is shown in Figure 1.

Starting from the left: The input voltage should be sampled with a long hold time sample and hold (S/H). I show the lab1 sample and hold because I designed one that (if it could be made to work) would be sufficient. The S/H is necessary to ensure that the input voltage does not vary during the 1 second-long conversion cycle.

There are voltage buffers for the reference voltage and for the input voltage. The op-amps in the input buffers are OP27's. I keep going back to OP27's because of their very low drift and high accuracy specs. Particularly for this case, we can neglect 1/f noise effects that could be overwhelming with other op-amps. The OP27 datasheet claims a total input voltage noise of  $80nV_{p-p}$  in the frequency range 0.1Hz–10Hz. This frequency range corresponds roughly to the frequencies that we are interested in and is well below the acceptable error levels. 1/2LSB for the full-scale input voltage range is 1.2mV. The sample and hold buffers the large source resistance, but the input buffers here include an additive input for offset correction of both the reference and the input voltage. This will be discussed in the auto-calibration section. The input buffer resistors are chosen to be 0.1% 5ppm/°C resistors. The tolerances do not account for the 12-bit accuracy because the auto-calibration will take care of these errors. This is one example of how cheaper parts can be used when an auto-calibration cycle is used.

There are 4 input switches. Two are for auto-calibration alone. The other two switch between the input voltage and the negative-valued reference voltage. The switches are implemented as NFETS. In order to reduce charge injection from the switches turning on or off, the FETs' source terminals are capacitively coupled to the sources of dummy switches that turn on when the input switches turn off. The capacitive coupling is necessary because without it, the input node to the integrator would be driven to the voltage connected to the drain of the dummy switches when they are on. In order to reduce the effect of input voltage dependent charge injection, the source voltage of the input switches is buffered with another OP27 and that voltage, the so-called bootstrap (bs) node, drives the sources of the dummy switches. The channel charge stored in the switches is

$$q_{ch} = WLC_{ox}(V_{GS} - V_T) \quad (3)$$

so if the threshold voltages for the switches are matched, controlling  $V_{GS}$  should match the channel charge well.

The integrator input resistor is chosen to be much larger than the  $R_{DS,on}$  of the FET switches, 5Ω, in order to minimize that error. It does not have to be very accurate because of the dual-slope integration. However, I chose it to be a low temperature coefficient resistor anyway so its another 0.1% 5ppm/°C resistor. The integrator capacitor is a 1.1μF polypropylene cap for minimum dielectric absorption. The R and C integrator values also needed to be chosen so that the integrator did not saturate during integration for a full-scale input voltage. That is,

$$\frac{V_{in,fs}\tau_1}{RC} < 12V \quad (4)$$

The switch across the integrator capacitor resets the capacitor between conversion cycles. The output of the integrator drives an LM311 comparator. The comparator offsets will also be accounted for each auto-calibration cycle. The comparator output collector pin is pulled up to 5V in order to drive the logic input level on the PIC microcontroller.

The PIC has a 10MHz clock. That means that each machine cycle takes

$$T_{machine} = 4 \times \frac{1}{10^7} \text{seconds} = 0.4\mu\text{s}. \quad (5)$$

The fixed integration time,  $\tau_1$  is chosen to allow 10 machine cycles per bit. This gives 40920 machine cycles for the fixed integration time. This corresponds to 16.4ms whereas the period of a 60Hz sinusoid is 16.7ms. Therefore, the fixed integration will do a good job of rejecting 60Hz components present in the input signal. The total number of conversion cycles available for the auto-calibration is limited by the long integration time, but we will see in the next section that this is not a problem. The PIC drives the switches with inverters that overdrive the gates to 15V.

Also at the output of the integrator is a correction feedback circuit for reducing the effects of dielectric absorption in the feedback capacitor. Referring to Bob Pease's article [1], the voltage on the capacitor will be held for no less than 16.6ms and no more than 33.2ms. The average voltage on the capacitor during that time is about half of the input voltage. According to Figure 7 in [1] this will cause about 0.0013% error even if the capacitor is reset for a tenth of the integration time. This error is about one twentieth of the total error budget. The model for the dielectric absorption is series RC legs in parallel with the capacitor. To fix this we can add appropriate current back into the integrator with the feedback network. The attenuation in the feedback measurement is to make the values for the R's and C's reasonable. In order to get values for the model for the capacitor in my integrator I would have to measure its time-domain response after being held and then reset and then let go for the times in my ADC. I don't have this data but I left connections in the design for the RC legs if I did.

Two bi-directional charge pumps are included in order to adjust the offset voltages input voltage and the reference voltage. Operation of the charge pump is as follows referring to the "REFUP" input. When REFUP is pulled high (to  $V_{DD} = 15V$ ), that voltage appears divided down onto the  $10\mu\text{F}$  capacitor as

$$V_{pump} = V_{DD} \frac{200\text{pF}}{10\mu\text{F}}, \quad (6)$$

where I have used the fact that the input capacitor is much smaller than the output capacitor. The RC time constant of the inverter pull-up resistor and the input capacitor is 200ns. When the input voltage goes low, the input capacitor, 200pF, discharges through the diode connected between  $V_{DD}$  and the transistor-side of the input capacitor. The charge that accounted for the voltage bump on the output capacitor stays there because it cannot flow back to the input capacitor. The output capacitor is buffered with a JFET op-amp so that it's voltage droops very slowly. The input bias current for the AD822 is about 2pA giving a droop of 200nV/sec out of an error budget of 1.2mV (6000x) so it is negligible. The capacitor values in the charge pumps are chosen to give voltage

steps of about  $1/8^{\text{th}}$ LSB. That is

$$V_{step} \approx \frac{(15V)(200\text{pF})}{10\mu\text{F}} \quad (7)$$

$$= 0.3\text{mV} \quad (8)$$

The PIC interfaces with the switches and the charge pumps with the inverters shown. There are two types of inverters. One is a normal inverter whose output goes from 0V to +15V. The inverter with the line through it is an inverter whose output goes from 0 to -15V. The 0-5V output voltages from the PIC output pin are level shifted with the resistor divider so that the gate of the PFET goes from -0.5V to -4.1V (enough to turn the PFET off and on). This inverter is used to drive the negative going pulses on the "down" inputs of the charge pumps.

Finally, The reference voltage and the full-scale input voltage for auto-calibration are AD588's with temperature coefficients of 1.5ppm/ $^{\circ}\text{C}$ . The power supplies are bypassed with large electrolytic capacitors and small ceramic capacitors. Not shown are  $0.1\mu\text{F}$  ceramic bypass capacitors at each of the op-amp power supply connections.

## II. AUTO-CALIBRATION

The PIC microcontroller supervises the auto-calibration as well as the conversion cycle switching. Flow charts that depict how this should work are shown in Figure 4. The first step in the auto-calibration (auto-cal) is to correct the scale-factor error. It does this by first connecting the full-scale input voltage (+10V reference) to the input and converting. The integration timing is set so that each bit gets 10 machine cycles. The PIC knows that the full-scale input voltage should result in a count of exactly  $81840 = 2(40920)$  machine cycles (because the de-integration reference is -10V). The auto-calibration takes the form of a successive approximation of the error voltages. It measures the difference between the measured counts and the correct counts. It then makes its best guess at the number of pulses to give to the charge pump to correct the offset and then tries again. The full-scale error is corrected by adjusting the reference voltage. Once the offset is less than  $1/2\text{LSB}$  (5 machine cycles) from what it should be, it moves onto the next step. Also, because the auto-calibration relies on one good reference voltage, namely the full-scale input voltage of +10V, that reference should be trimmed to within  $1/2\text{LSB}$  of +10V. The auto-calibration takes care of errors in the -10V reference voltage for de-integration so it does not need to be trimmed so well.

After the first full-scale error correction it then corrects for the zero-input or offset error in the same way except with the input grounded. Finally, it re-corrects the full-scale error to get both the offset and the scale-factor right. This correction process is depicted in Figure 3.

Because of the "best guess" or successive approximation technique for correcting the offset, each error correction step shouldn't take more than a few conversion cycles. Conversion cycles take about  $1/60^{\text{th}}$  of a second for zero inputs and twice that for full scale inputs. That means about 45 conversion cycles can fit into 1 second. Since there are three error correction steps each taking only a few conversion cycles in

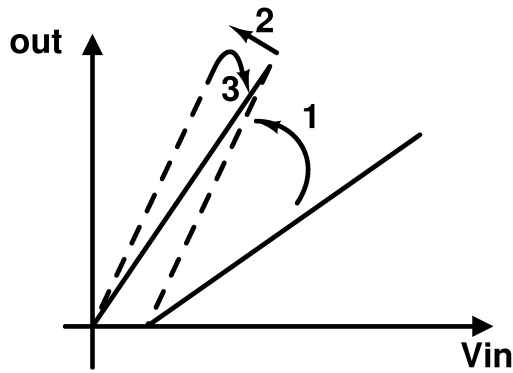


Fig. 3. The auto-calibration process corrects the full-scale error, then the offset error, then the full-scale error again to get both endpoints right.

addition to the final real conversion cycle, this should not be a problem.

### III. ERROR SOURCES

Relative accuracy is how well the conversion data represents the ratio of the input voltage to the reference voltage. Absolute accuracy is how well the conversion data represents the absolute voltage value at the input to converter. This depends on the relative accuracy and on the accuracy of the reference voltage. Non-monotonicity can occur whenever there is an error of more than  $1/2\text{LSB}$ . A lot of error sources are accounted for by the auto-calibration cycle (offset and scale-factor). These errors sources include the following. Charge dump from the input and reset switches cause a pure offset error. An input offset at the integrator causes both an offset and a scale factor error. Op-amp dynamics and delays in the comparator and PIC result in a non-zero turn-around time after the comparator triggers and this results in a pure offset error. Any delay in the startup time of the integrator causes an error that depends on the slope of the integration so it is a scale factor error. Delays in the comparator and PIC at the end of the integration cause a pure offset error because they are independent of the input voltage. All of these scale factor and offset errors are taken care of in the auto-calibration cycle.

The dual-slope integration produces an output code that is independent of the resistor and capacitor values. Also, because it integrates the capacitor voltage up and down the total time depends only on the charge balance which does not depend on capacitance nonlinearity as its value changes with voltage.

Drift that occurs right after the auto-cal is not accounted for. Power supply variations that occur during the final conversion cycle are not accounted for nor are noise sources on the input. 60Hz pickup should be a non-issue because the input voltage integration time is almost exactly one 60Hz period.

#### A. Power Supply Variations

Power supply variations could show up on the outputs of the op-amps. The OP27 has a PSRR of 120db so that to cause a  $1/2\text{LSB}$  error, the  $\pm 15\text{V}$  supplies would have to vary by

1.2kV. The AD822 op-amps also have a PSRR of 100db for unity gain so that a 120V variation would be necessary to cause a  $1/2\text{LSB}$  error there. The reference voltages have a PSRR of 100db at low-frequency so there errors will also be negligible.

The only other place that the power supplies are connected are at the inverter pull-up resistors and at the bias voltages for the transistors in the charge pump. The accuracy of the charge pump bias voltage won't matter much. As long as the transistors in the charge pump don't saturate due to the output voltage level, the operation is roughly constant. Also, any small variations in the charge pump operation are dealt with automatically by the calibration cycle. That is, the auto-calibration does not rely on the charge pump steps being very precise.

The power supply variation on the inverter pull-up resistors affects how strongly the switches are turned on. This results in  $R_{DS,on}$  variations but I already showed that I chose the only resistor that matters for that, the integrator resistor, to be large so that the value of  $R_{DS,on}$  has no significant impact on the integrator timing.

#### B. Temperature Drift

Temperature drift after the auto-cal could also cause errors. The input buffer and integrator resistors have temperature coefficients (tempco's) of 5ppm/ $^{\circ}\text{C}$ . The OP27 op-amps have tempco's of  $0.2\mu\text{V}/^{\circ}\text{C}$  and the AD822  $0.3\mu\text{V}/^{\circ}\text{C}$ . The reference voltage has a tempco of  $1.5\text{ppm}/^{\circ}\text{C}$ . The input buffer resistors are connected ratiometrically so if they see the same temperature, then they will cause negligible errors proportional to differences in their tempco's. Over the full temperature range of  $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ , the input offset drift of the op-amps is only  $2\mu\text{V}$  which is about one  $1000^{\text{th}}$  of  $1/2\text{LSB}$ . That leaves the integration resistor and the reference voltage. Errors in the integration resistor can only effect the output if they change during the integration cycle. This is one of the advantages of the dual-slope integration. The time to integrate and de-integrate only depends on the ratio of the input voltage to the reference voltage. If we model this effect as an integration with one R-value,  $R$ , and a de-integration with another R-value,  $R'$ , we can get a feel for the error it would cause. The resulting dual-slope relation would become:

$$\frac{V_{in}}{V_{ref}} = \frac{R}{R'} \frac{\tau_2}{\tau_1}. \quad (9)$$

If the temperature changed by  $10^{\circ}\text{C}$  right at the turn-around point (or effectively did so), the error in the output data would be

$$\epsilon = (5\text{ppm}/^{\circ}\text{C})(10^{\circ}\text{C})(100) = .005\% \quad (10)$$

or about half of  $1/2\text{LSB}$ .

#### C. Noise

Noise on the input will be sampled on the S/H capacitor. If it is thermal noise it will cause  $\sqrt{kT/C_{SH}}$  total sampled noise. We can tolerate about  $.5\text{mV}$  total noise meaning the SH capacitor needs to be larger than  $17\text{fF}$  so this won't be a problem.

We might simplify the effect of integrating the noise over the dual-slope integration cycle to say that the noise bandwidth is about  $1/(\tau_1 + \tau_2)$  which is never more than 60Hz. The thermal noise density from the input switch is small compared to the integration resistor's noise because it is  $\sqrt{4kTR_{DS,on}}$ . The voltage noise density from the integration resistor is  $\sqrt{4kTR} = 18\text{nV}/\sqrt{\text{Hz}}$ . The input noise of the OP27 is  $3\text{nV}/\sqrt{\text{Hz}}$  but at these low frequencies its  $1/f$  noise takes over and we get a total noise of about  $80\text{nV}_{\text{p-p}}$  over 0.1Hz to 10Hz. Extrapolating that as an rms voltage noise density gives  $18\text{nV}/\sqrt{\text{Hz}}$ . There are 5 OP27's contributing noise to the measurement. Before considering their individual effects, the total noise from each is only 140nV which is one 14,000<sup>th</sup> of 1/2LSB so it will always be negligible. The  $1\text{M}\Omega$  resistor at the output of the integrator for the dielectric absorption compensation does not contribute significant noise because of the low-impedance output of the op-amp it faces.

#### IV. ABBREVIATED PARTS LIST

- 1) .1% 5ppm/ $^{\circ}\text{C}$  metal film chip resistors: Vishay RCME series
- 2)  $1.1\mu\text{F}$  Polypropylene Cap: Vishay MKP series
- 3) 2N7000 FET switch: Digikey 2N7000FS-ND
- 4) PFET ZVP3306A: Digikey ZVP3306A-ND
- 5) dual OP27 op-amp package: Digikey OP270GN8-ND
- 6) AD822 JFet op-amp: Digikey AD8225AR-ND
- 7) AD588 voltage reference: Digikey AD588JQ-ND
- 8)  $200\text{pF}$  25V ceramic capacitor: Digikey 04023A201JAT2A-ND
- 9)  $10\mu\text{F}$  25V ceramic capacitor: Digikey 445-2892-ND

#### REFERENCES

- [1] Robert A Pease "Understanding capacitor soakage to optimize analog systems" National Semiconductor Corp, No Date.
- [2] Ji-Jon Sit, Rahul Sarpeshkar "A Micropower Logarithmic A/D With Offset and Temperature Compensation" IEEE Journal of Solid State Circuits, Vol. 39, No. 2, February 2004.



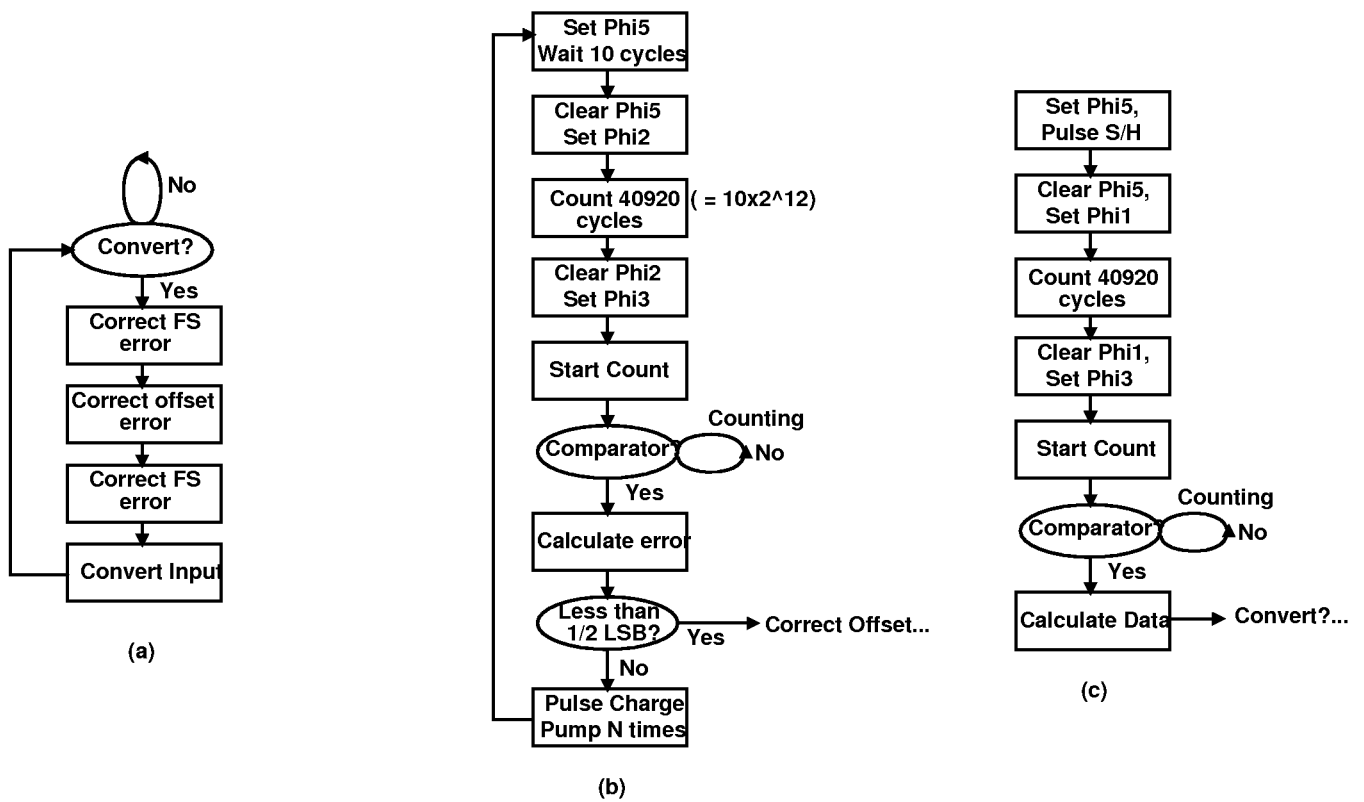


Fig. 4. Flow charts for the ADC algorithms for PIC software including auto-calibration and conversion. (a) is the overall conversion cycle. (b) is an example zoom-in of one of the error correction blocks, namely the first Full-scale error block. (c) is the input voltage conversion cycle.