A 2 μW, 100nV/rtHz, Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials

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Abstract* –This paper describes a prototype micropower instrumentation amplifier intended for chronic sensing of neural field potentials. Neural field potentials represent the ensemble activity of thousands of neurons, and code useful information for both normal activity and disease states. Neural field potentials are small--on the order of tens of μV--and reside at low bandwidths that make them susceptible to excess noise. Therefore to ensure the highest fidelity of signal measurement for diagnostic analysis, the amplifier is chopper-stabilized to eliminate 1/f and popcorn noise. The circuit was prototyped in a 0.8μm CMOS process, and consumes under 2.0 μW from a 1.8V supply. A noise floor of 0.98 μV_{rms} was achieved over a bandwidth from 0.05 to 100 Hz; the noise-efficiency factor of 4.6 is one of the lowest published to date. A flexible on-chip high pass filter is used to suppress front-end electrode offsets while maintaining relevant physiological data. The monolithic architect and micropower low-noise, low-supply operation could help enable applications ranging from neuroprosthetics to seizure monitors that require a small form factor and battery operation. Although the focus of this paper is on neurophysiological sensing, the circuit architecture can be applied generally to micropower sensor interfaces that benefit from chopper stabilization.

I. Measurement Background

Recording of neurophysiological activity is an accepted medical diagnostic approach for applications ranging from seizure monitoring to neuroprosthesis. As illustrated in Fig. 1, neuronal activity can be measured with a number of techniques, ranging in resolution from single cell recording[1-3] to the measurement of gross cortical activity with the electroencephalogram (EEG). Each technique has its trade-offs. Single-cell recording provides high spatial resolution, but at the cost of amplifier power, the need for pre-processing of information prior to telemetry, and challenging requirements for chronic electrode-tissue interface stability[1,2,4]. EEG provides minimally-invasive recording, but at the expense of small signals subject to artifacts, and limited spatio-temporal resolution[4]. In practice, the choice of a particular measurement approach is a balance of several system constraints, including the measurement electrode's spatial resolution, the desired neurophysiological information content, and the power requirements for sensing, algorithm/control and telemetry. Finding the proper balance between signal coding and technical trade-offs is key to building practical neuroprothetics.

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The measurement of neural field potentials (NFPs) provides acceptable trade-offs for a variety of biomedical applications.

TABLE I
KEY NEURAL AMPLIFIER REQUIREMENTS

Specification	Value	Units/Comments
Supply Voltage	1.7 to 3.3	Volts
Supply Current	1.0	uA
Gain	40 (min)	dB
Noise	1.5	μV rms , 0.05 to 100Hz
CMRR	> 80	dB (DC to 60Hz)
Nonlinearity	< 0.1%	Harmonic Distortion
Aliasing	< -40	dB (compared to baseband)
Functional Range	20 to 45	Celsius
High-Pass Corners	0.05, 0.4, 2.5	Hz, no external components
Electrode Polarization	15, 50	mV (DC headroom)

A particular advantage of NFP measurements, both on the surface of the cortex (electrocortigraphy/ECoG) and from a region around an implanted electrode, is that it is less susceptible to chronic measurement issues and can provide more robust measurement of biomarkers[2,4]. Because NFPs represent the ensemble activity of thousands to millions of cells in an *in vivo* neural population, their recording can avoid issues like tissue encapsulation and micromotion encountered in single-unit recording[2, 4, 5], and motion/muscle artifacts in externalized surface EEG[4]. Though less spatially refined as single cell microelectrode recordings, recent work has demonstrated that spectral decomposition of NFP signals can encode the necessary information for building an effective neuroprosthetic interface [4,5,7]. NFPs also encode biomarkers for disease states where ensemble neural firing is the hallmark of the disease; examples of these pathologies include epileptic seizures[7] and basal ganglia rhythms in Parkinson's disease[8].

NFP measurement provides some technical advantages for chronic recording. Given that NFPs represent the average ensemble activity, the spectral content is limited to relatively low frequencies (< ~150 Hz). The focus on low frequency measurements limits the required gain-bandwidth product for the amplifier, aiding in lowering system power. An additional motivation for NFP-based systems is the constraint that the electrode places on the measurement. Limiting the design to state-of-the-art technology, the implementation of a system with interleaved sense and stimulation can require electrodes with a large surface area that affectively averages neuronal activity and effectively limiting measurement to NFPs.

NFP measurement does present some unique challenges. In particular, NFP signals of physiological interest generally fall below a hundred Hertz[4,6,9], which shifts the circuit design problem away from the thermal noise issues in single spike recordings to one of addressing the significant excess 1/f and popcorn noise in transistors. This excess noise can artificially depress the signal-to-noise ratio and lead to incorrect diagnostic conclusions.

This paper introduces a prototype chopper-stabilized instrumentation amplifier architecture that achieves excellent noise performance while being practical for portable, microwatt neural sensing applications targeting NFPs and even extending to EEG. Though this paper's focus is on neurophysiological applications, the chopper-stabilization architecture is broadly applicable to general low-noise, micropower sensing applications that can benefit from dynamic offset compensation.

II. Neural Amplifier Design Requirements

As shown in Fig. 2, the neural recording signal chain places unique physiology-driven constraints on the design of the front-end amplifier. Neural field potentials created by an ensemble of neurons represent fundamental inputs to this signal chain. These ionic potentials are transduced into electrical signals at the tissue-electrode interface. Placement of a metallic electrode in the tissue results in charge redistribution creating a capacitive double layer that can lead to significant polarization voltages[10]. These offsets can easily saturate the high-gain amplifier designed to record microvolt range NFPs and hence must be adequately rejected. Another key requirement is to avoid corrosion of the electrodes that may cause cytotoxicity. This necessitates a limiting of leakage current from the amplifier inputs.

In addition to these requirements, as mentioned previously, recording of low amplitude and relatively low frequency neural field potentials requires minimization of the effects of intrinsic 1/f and popcorn noise sources from the amplifier. Hence the focus of this work is to design an amplifier that adequately addresses these key requirements, summarized in Table 1 for convenience. Such a design can provide high-fidelity neural field potential measurements that can be digitized for application specific signal processing to extract biomarkers of interest.

A. Electrode- Tissue Interface Constraints

Platinum-iridium (PtIr) brain stimulation electrodes [11] were characterized to model the tissue-electrode interface and define amplifier requirements. PtIr is a polarizable material that forms a double layer junction with an excess capacitance from the plating of ions[10]. To characterize the junction, impedance sweeps of four 6 mm^2 PtIr stimulation electrodes were performed to model transduction characteristics in the signal band. Extrapolating from the data in Fig. 3, the electrode can be modeled as an equivalent 3.2 μF capacitor in series with a 1 kΩ resistor. In addition to these ac characteristics, the dc polarization voltage was measured across 100 electrode pairs soaking in sodium chloride solution (2700μS-cm) at 37 C, with a 20 MΩ bias resistor biased the dc potential of each electrode to ground. The electrode's mean differential offset was 0.1 mV, with a standard deviation, σ, of 2 mV. Using this data, we specify a 15 mV of headroom for greater than +/-6 σ range for a diagnostic recording system. In the presence of stimulation, polarization transients of one hundred millivolts can exist that decay with a 1 s time constant. By specifying +/-50mV of headroom, and assuming a suitable high-pass filter is employed, we can reacquire signal acquisition within 5 seconds of stimulation cessation.

The tissue-electrode interface characteristics drive key design inputs for the amplifier design. First, the series capacitance can create a parasitic high-pass pole for the signal chain. To avoid this issue, the input resistance of the amplifier is specified to have an impedance greater than 5 MΩ. This value insures that the highpass pole is set by on-chip circuitry. The second electrode-driven design constraint is the polarization headroom that must be rejected by the on-chip highpass filter. The scaling of the on-chip high-pass was designed to support both 50 mV for sense-stimulation applications, and 15 mV for diagnostic (no stim) applications. The final constraint is the minimization of leakage currents through the electrodes; the input leakage must be well under 1μA to minimize electrode corrosion[10,11]. Bounding the differential polarization to 50 mV, and assuming a 5 MΩ differential input resistance, we limit the maximum bias current of the amplifier to 10 nA.

B. Micropower Chopper Stabilization Design Paradigm

The properties of the electrode-tissue interface and the frequency distribution of NFPs motivate the amplifier design. First, the amplifier must reject the electrode polarizations characterized in the previous section, which would otherwise saturate the amplifier. In addition, the design must minimize susceptibility to excess low frequency noise in the transistors to maximize sensitivity to NFP-based biomarkers. To suppress both of these error sources we designed a chopper stabilized amplifier employing multi-path feedback.

Chopper stabilization is an established technique for suppressing offsets and drift, and has been explored extensively for biomedical applications [12,14,15]. Fig. 4 illustrates the core elements of a typical open-loop chopper amplifier. At the input, a CMOS switch modulator translates the input signal, $V_{in,}$ to the chopper frequency prior to entering the amplifier at node V_A. The lower limit of the modulation (chopping) frequency is generally set by the amplifier's excess noise corner, illustrated as "aggressors" superimposed at node V_A [12]. After amplification, a second demodulator at V_A' translates the signal back to baseband while shifting the aggressors up to the modulation frequency. The final lowpass filter of the signal at V_B then ideally restores the desired amplifier signal at the output, while suppressing the up-modulated offsets and 1/f noise from the amplifier at the output V_{out} [13]. A benefit of chopper stabilization for NFP measurement is that it suppresses the low-frequency noise with minimal signal or noise aliasing [12, 16].

In micropower applications, however, the chopper architecture has issues to be resolved. The primary issue is the finite bandwidth of the signal chain creating signal errors. To help illustrate this effect, Fig. 4 plots the time-domain response of the signal chain responding to a dc input. While responding to the modulated input at V_A, the amplifier's limited bandwidth creates a first-order transient response at V_A'. When this bandwidth-limited signal is demodulated at V_B and lowpass filtered, the transient results in even harmonics at the chop frequency which create distortion and sensitivity errors. As described in [12], the sensitivity of a chopper amplifier with ideal gain, A_o, is reduced to an effective gain of $(1-4\tau/T)$, where τ is the time constant of the amplifier and T is the chopper period. This issue can be particularly bad in micropower amplifiers, where the amplifier has a limited bandwidth product compared to the lower-limit dictated by the 1/f noise corner. In practice, robust open loop chopper architectures can require a gain-bandwidth product approximately ten times greater than the NFP application demands [17]. The excessive power burden to implement chopper stabilization then makes it impractical. A secondary consideration with the open loop architecture for low-supply designs is the headroom requirement for offsets being amplified prior to chopping and lowpass filtering. The amplified offset signal at V_A' requires limiting the front-end gain to avoid saturation, which can undermine performance by introducing second-stage noise.

The proposed chopper architecture circumvents the major issues of low power designs by using closed-loop feedback with specific timing constraints. To illustrate this concept, the proposed signal flow graph for an amplifier responding to a step is illustrated in Fig. 5. Feedback is a well-known technique to suppress distortion and increase precision in circuits[12, 18]. The implementation of feedback in this micropower application, however, required two design paradigms. First, input and feedback paths around the amplifier are conveyed as ac signals that were up-modulated to the chopper modulation frequency. The ac feedback ensures that all signals passing through the front-end of the amplifier are well above the 1/f corner for the transistors. Using ac modulation also allows for input and feedback signal chain scaling to be achieved with low-noise, on-chip poly-poly capacitors as opposed to resistors that potentially draw excess power and add noise to the signal chain [12,15,18]; Fig. 5 applies this ratio by the scaling factor $1/A_o$ in the feedback path Second, chopper modulation throughout the signal chain is designed such that switching dynamics are much faster than the chopper period. The impact of this criterion depends on the location of the chopping operation. At the input and feedback nodes, V_{in} and V_{out}, the effective time constant of chopper settling is constrained to be orders of magnitude smaller than the chopper period. Within the forward amplifier path, fast modulation is performed by steering currents within the transconductance stage prior to integration and loop compensation. By partitioning the forward path such that modulation occurs prior to integration, the steady-state signal is minimized which helps further suppress distortion. Following these design ideas enables chopping the amplifier at higher frequencies (e.g. 4 kHz), which are substantially above the gain-bandwidth for the overall feedback loop.

The proposed use of feedback in this chopper stabilized amplifier has some advantages over those explored in previous designs [15, 18]. Perhaps the greatest advantage of this design is the use of ac modulation in the input and feedback paths, which allows for the front-end gain to be set with on-chip capacitor ratios with excellent noise and linearity properties, instead of requiring high-value on-chip resistors [15, 18]. The net sensitivity error ε is then set to first-order by differences in the settling time-constants in the input and feedback paths: $\varepsilon = [T-\tau_{in}]/[T-\tau_{fb}]$, where T is the chopper clock period, and $\tau_{in,}$ τ_{out} are the settling times of the input and feedback switching paths. With a modulation frequency of 4 kHz and τ of the order of 100 ns, the gain error was kept to below 0.2% without further compensation. In practice, gain errors will be dominated by relative component matching. An additional advantage of this design is that by taking advantage of global feedback to a summing node, we can architect the forward path's transconductor and integrator to run with low supply overhead to aid in minimizing power without sacrificing noise performance[1,15]. A final potential advantage of using this feedback topology is that it allows for larger front-end gain by filtering the up-modulated offset with a first-order lowpass filter. At the output, the residual ac offset signal is $\pi f_{3db} A_o V_{off}/(2f_{chop})$, where f_{3db} is the lowpass corner of the feedback loop, A_o is the net gain, and f_{chop} is the chop frequency. In theory, the offset filtering allows more gain to be placed in the front-end amplifier, suppressing sensitivity to secondary stage imperfections and allowing lower supply voltages. In practice, however, the need to suppress electrode polarization sets a practical upper limit on the front-end gain. The next sections cover the detailed implementation of the prototype amplifier.

III. Neural Amplifier Design Overview

A. *Amplifier Top-Level Architecture*

The implementation of the chopper instrumentation amplifier requires ac modulated feedback paths as well as a chopper stabilized amplifier. This section is a top-level discussion of the feedback and peripheral circuitry. Fig. 6 illustrates this scaling with a signal flow graph and its implementation with the top-level architecture. A difference between this signal flow and that presented in [19] is that in this design overview the gain was repartitioned to be x20 on the chopper front-end, with a buffer amplifier with a gain of x5 to achieve a total gain of x100, as opposed to achieving all of the gain in the first-stage chopper amplifier. The motivation for this repartitioning will be evident in the discussion of the on-chip high-pass filter implementation.

The gain and high-pass filtering characteristics of the chopper-stabilized instrumentation amplifier are set by the input and feedback switched capacitor networks. The amplifier summing node, V_A, receives a differential signal input scaled by the capacitor C_{in}, which is balanced by two single-ended feedback networks. The path through C_{fb} sets the midband gain for the amplifier, while the path through the feedback integrator and C_{hp} sets the high-pass corner for the amplifier. Chopper modulation is performed with cross-coupled, minimally sized (0.8μm), complimentary CMOS switches throughout the design; the appropriate signal polarities for negative feedback is achieved by relative clock phasing. Note that these feedback paths are always negative; when the polarity around the amplifier shifts, the internal chopper modulation within the transconductor also changes sign to maintain loop stability.

The on-chip poly-poly capacitor values for scaling the signal paths were chosen to meet the key design requirements for sensitivity and filtering. The input capacitors are 15 pF, so that with a 4 kHz chopper frequency the differential input impedance is greater than 8 MΩ to avoid loading the electrodes. The midband gain of the chopper amplifier is then determined by the ratio of the feedback capacitors C_{fb}, to C_{in}. For the 40dB gain amplifier this set C_{fb} to 750 fF for a front-end gain of 20, while for the higher gain system C_{fb} was reduced to 250 fF for a front-end gain of 60. To provide both ac modulation and a set-point for the single-ended output, the voltage to C_{fb} is switched between the amplifier output and a system-supplied reference potential, V_{ref}, which supplied externally along with the 4 kHz system clock.

A second shunt feedback loop sets the highpass characteristic for the amplifier using on-chip feedback in a manner conceptually similar to [20] and [15]. This high-pass, however, was implemented monolithically with switched capacitor techniques to try to achieve higher accuracy and to minimize external components. Although this sampled-data filter is subject to aliasing and kT/C noise, by sampling after the front-end's lowpass filtering the aliasing is suppressed.

Several design constraints must be considered in the high-pass design. The first constraint is the scaling of the capacitor C_{hp}, which is dictated by the dc polarization headroom that must be blocked by the amplifier. In our application, this is the differential polarization of the platinum-iridium electrodes. Referring to the signal flow diagram in Fig. 6, in steady-state the charge induced on V_A from the input modulation through C_{in} must be countered by the feedback capacitor C_{hp}. This constrains the available headroom with a single-ended feedback to

$$V\max \approx \pm \frac{C_{hp}}{C_{in}} \bullet \frac{V_{dd}}{2}. \qquad (1.1)$$

To ensure 50 mV of headroom with a 2V nominal supply, the value of C_{hp} must be greater than or equal to 750 fF for a single-ended feedback scheme. Note that adding additional C_{hp} for greater headroom loads the summing node of the amplifier, which acts as an input charge divider. The impact of this charge divider is to increase the input-referred noise:

$$e_{net,RTI} = \left(\frac{C_{in} + C_{hp} + C_{fb} + C_{amp}}{C_{in}} \right) \cdot e_{n,amp} \qquad (1.2)$$

where $e_{n,amp}$ and C_{amp} represent the input referred noise and input capacitance of the transconductance amplifier, respectively. Because noise is of primary concern in this amplifier, we designed for the minimum allowable polarization headroom in the amplifier.

The gain of the high-pass feedback path sets the overall filtering characteristic. The voltage modulated through C_{hp} is provided by a switched capacitor integrator circuit that samples the output of the mixer-amplifier relative to V_{ref}, and then drives the output towards V_{ref} in steady-state. The implementation of the integrator is shown in Fig. 7. The unity gain frequency of the net loop transfer function

$$L(s) \approx \frac{C_{hp}}{C_{fb}} \cdot \left(\frac{F_{Chop}}{2\pi C_{\text{int}}} \cdot C_{samp} \right), \qquad (1.3),$$

determines the effective high-pass corner. The bracketed expression represents the switched capacitor integrator gain set by the sampling capacitor, C_{samp}, and the integration capacitor C_{int}. The sampling of the high-pass loop is performed at twice the chopper frequency to cancel out the up-modulated offset ripple from the chopper amplifier by averaging the two phases of the ac ripple. In [19], we explored implementation of this loop after a gain of 40dB in the chopper circuit. With such a large gain, the ratio of C_{hp} to C_{fb} is 5 and with the chopper clock at 4 kHz, we required a ratio of C_{int} to C_{samp} of 64,000:1 to implement the 0.05 Hz pole. This ratio can be accomplished with an on-chip 1nF capacitor that uses ~ 1mm^2 of area for C_{int}, with a sampling capacitor of 15 fF, but this design has poor yields and unacceptable sensitivity to process variation. To improve the robustness of the design, the gain of the chopper was dropped to twenty which relieves the ratio of C_{int} to Cs_{amp} by 5, to 12,800:1.

Even with this relaxed constraint, the fabrication of the 4.2 GΩ resistor is a challenge. To achieve acceptable matching between sampling capacitors and C_{int}, a parallel bucket-brigade of capacitors was used with 6x the target capacitor value. This was done in an attempt to achieve better matching for the C_{samp} capacitor with respect to the C_{int} integration capacitor. The switches for the bucket brigade were minimally sized and care was taken in layout to minimize stray coupling to the clocks. To adjust the high-pass corner, the loop gain was adjusted by either tapping into different points along the C_{samp} chain, or using the full cascade of six capacitors and adjusting the size of the integration capacitor. For the 2.5Hz corner, one cascade cap of 190 fF was tapped off with a C_{int} of 100 pF. The 0.05 and 0.5Hz corners used the full 6x cascade and then adjusted through adjustment of C_{int}. The operational amplifier used for this stage was not drift compensated; with the gain of 20 and rescaling of input transistors, its noise contribution is still minimal in the measurement band. The operational amplifier used was a two-stage Miller-compensated design with a total current consumption of 50nA; the details are not critical to the operation of the design and will not be presented here.

The final addition in this latest design is a 5x buffer amplifier and lowpass filter which drives the ADC. The output buffer takes advantage of high-resistance CrSi in the process to build the on-chip filters; this allows for continuous-time filtering of the chopper output. Since the resistors are placed after the chopper amplifiers gain, their input-referred noise is kept under 25 nV/rtHz in the passband. As shown in Fig. 8, the inverting amplifier uses a cascade of two lowpass filters with individual corners at 200 Hz to suppress the up-modulated offsets, and provide a net -3dB point at 130 Hz. This amplifier is a standard two-stage op-amp design, and was biased with 150nA of current; the details of the amplifier are also not critical to the operation of the design and will not be presented here.

The architecture developed in this section has several key advantages. The use of continuous-time modulation of the input and feedback signals provides low-noise amplification through the use of on-chip capacitors within the sensitive first-stage. Sensitivity throughout the signal chain is set by ratios of similar components, either on-chip capacitors or CrSi resistors. At the front end, the switching of the input between two capacitors provides good CMRR and rail-to-rail common-mode input swing, without adversely interacting with the electrodes. Finally, the use of on-chip switched capacitor techniques to create the high-pass filters provides high accuracy and eliminates the need for external components, while the sampling after the first-stage gain and lowpass filtering minimizes the aliasing and sampling noise associated with this feedback path. The repartitioning of the gain in the signal chain, coupled with the cascaded sample capacitors helps to make the monolithic high-pass filter more robust. The limitation of this architecture is the finite polarization headroom, which will be discussed in more detail later.

B. Micropower Chopper-Stabilized Amplifier

The design of the chopper amplifier targets low noise and low supply operation along with current steering demodulation. Chopping signal currents is achieved by modifying a folded-cascode amplifier. This implementation requires few modifications to the basic design, and high-power examples of chopper cascode architectures were previously studied in [21] for operational amplifiers.

The classical architecture requires only two additional sets of CMOS switches to chopper stabilize the amplifier. The architecture is shown in Fig. 9; the bias networks are not shown to simplify the diagram. The first switch set is placed at the sources of the bias transistors M12/M13, which demodulates the desired ac signal as well as upmodulating the front-end offsets. The second switch set is embedded within the self-biased cascode mirror to up-modulate the errors from M8/M9. The source degeneration of M6/M7 and bias network M12/M13 attenuates their offsets and excess input-referred noise. With this switch architecture, the output of the transconductance stage is at baseband, which allows for the integrator to both compensate the feedback loop and filter upmodulated offsets and noise.

An additional advantage of the folded-cascode amplifier is that currents can be better partitioned to improve noise performance. In this design, we allocated 300 nA to flow through each input pair, 50 nA to flow through each leg of the folded cascade, and 50 nA for the output stage, and 50 nA for bias generation and distribution. To suppress the noise contribution from M3 and M4 at the chopper frequency, they were scaled to be relatively large and 200 kΩ CrSi resistors were used to degenerate their sources and lower their effective transconductance. The 80 pF compensation capacitor stabilized the amplifier to a first-order system. The chopper design is compensated as a typical g_m/C amplifier, with a net bandwidth of roughly 1 kHz in the gain 20 configuration.

TABLE 2
KEY BIOPOTENTIAL AMPLIFIER RESULTS

Specification	Value	Units/Comments
Supply Voltage	1.8 to 3.3	Volts
Supply Current	1.0	uA
Gain	41, 50.5	dB (High polarization), Diagnostic)
Noise	0.95	μV rms , 0.05 to 100Hz
CMRR	> 80 > 100	SE dB (DC to 60Hz) DE dB (DC to 100Hz)
Nonlinearity	< 0.1%	Harmonic Distortion (5 mV input)
Aliasing	< -50	dB (compared to baseband)
NEF	4.6 / 5.4	Diagnostic / Sense-Stim Modes
High-Pass Corners	0.05, 0.4, 2.5	Hz, digitally programmable No external components
Lowpass Corner	180	Hz (-6dB 2-pole filter)

C. Amplifier Front-End Biasing

The biasing design of the summing node V_A at the input of the chopper amplifier is a balance between noise and settling considerations. Although the signal characteristics are purely ac at this node, the amplifier must have the proper dc biasing to ensure the appropriate amplification and demodulation of the signals. In particular, the dc bias network's impedance must be large enough to minimize noise, while still being small enough to keep the input held at the bias in the presence of typical leakages and common-mode perturbations.

To balance these performance constraints, the input stage was biased with "long-FET" (W/L << 1) transistors to a value of roughly 7.5 GΩ [9]. As illustrated in Fig. 10, a bias current was passed through a reference FET M1, biased in sub-threshold. The gate voltage was then mirrored to a long-length FET M2. Assuming symmetric drift currents, the net small-signal impedance of M2 to the reference voltage is modeled as

$$R_{eq} \approx \frac{W1}{L1} \cdot \frac{L2}{W2} \cdot \frac{kT}{\kappa q I_{bias}} \qquad (1.4)$$

where κ is the sub-threshold slope factor of approximately 0.7. This model demonstrates that synthesizing a resistor on the order of 7.5 GΩ is feasible using on-chip FETs biased with 5 nA of current. Unlike diode biasing with non-linear settling time-constants, this approach settles out with a defined time constant of R_{eq}*C_{in}, or roughly 125 ms in our implementation.

The noise for the bias circuit is modeled by shot noise in the equilibrium drift currents through M2. This model predicts the equivalent noise current as

$$I_n^2 = \frac{4kT}{R_{eq}} \cdot \left[A^2 \big/ Hz \right] \qquad (1.5),$$

that when referred back to the input through the input capacitors impedance at the chop frequency yields a net noise

$$e_n = \sqrt{\frac{4kT}{R_{eq}}} \cdot \left(\frac{1}{2\pi C_{in} F_{chop}} \right) \cdot \left[V \big/ \sqrt{Hz} \right] \qquad (1.6)$$

of roughly 25 nV/rtHz.

D. *Low-Noise Strategy Review*

This chopper-stabilized instrumentation architecture has several features that combine low noise with low power. At the system level, chopper stabilization suppresses the net 1/f noise for the amplifier, since the modulation frequency of 4 kHz is 5x the mixer-amplifier's inherent 1/f corner [12]. The use of continuous time modulation techniques in the sensitive first gain stage minimizes aliasing of noise from the amplifier, uses low-noise capacitors for setting gain, and avoids the kT/C noise from sampling input voltages. At the block level, currents were partitioned to minimize noise. The primary chopper-stabilized amplifier was biased with 800nA total current, with the bulk of current (600nA) through the input pair. The remaining current was allocated after the x20 gain stage (150nA output buffer, 50nA high-pass integrator) with minimal noise penalty. To further suppress noise, modest source degeneration of the NFETs M3 and M4 was added to help to suppress the transconductance of the low-side NFETs and minimize their noise impact. Finally, the summing node of the mixer-amplifier is biased with long-FETs to minimize residual shot noise, and the summing node's shunt capacitance was minimized to prevent signal charge attenuation that would boost the amplifier's referred-to-input (RTI) noise. With these techniques, the RTI noise floor for the instrumentation amplifier can be estimated as the sum of the thermal noise in the transconductor's input transistors (g_m), the V_A long-FET biasing circuit, and the input resistor on the buffer's lowpass filter (R_{LPF}):

$$e_n^2 = \left[\left(\frac{C_{tot}}{C_{in}}\right)^2 \cdot \left(\frac{4kT}{g_m} + \frac{4kTR_{LPF}}{\left(\frac{C_{int}}{C_{fb}}\right)^2} \right) + \frac{4kT}{R_{eq}} \cdot \left(\frac{1}{2\pi C_{in} F_{chop}} \right)^2 \right] \left[V^2 / Hz \right] \quad (1.7),$$

Note that C_{tot} represents the total capacitance loading the summing node of the mixer-amplifier. Estimating values from the design, this back-of-the-envelope calculation predicts a noise floor of 85 nV/rtHz, dominated by the transconductor's input FETs. SpectreRF simulations accounted for more secondary sources throughout the chopper-stabilized folded-cascode, and boosted the estimate to 95nV/rtHz.

IV. Prototype Results

The proposed design was prototyped in a 0.8µm CMOS process with on-chip poly-poly capacitors and high resistivity CrSi. The target application is a Li-battery powered NFP amplifier. Two amplifiers were prototyped: one with a gain of 100 (50 mV headroom) for high polarization sense-stim applications, and the other with a gain of 300 (15 mV headroom) for low polarization diagnostics. The results are summarized in Table 2; key results are summarized here.

A. *Transfer Function and CMRR*

The transfer function of the amplifier met the design expectations and requirements. From Fig. 11, the untrimmed gain of the circuit was measured to be 41dB. Similar to [19], the slight increase in gain was caused by parasitic fringe mismatch between C_{in} and C_{fb} which was not corrected in this design. The high-pass corners from the on-chip feedback network came to within 5% of the design target with no trim or external components, while the un-trimmed lowpass corner of 120Hz (-3dB, for two pole roll-off) lower that the design intent; this was due to 7% lower CrSi resistance than the design calculations assumed. The tighter tolerance on the high-pass corners resulted from the improved partitioning of the chain with more reasonable ratios of on-chip capacitors. Note that the x300 amplifier's high-pass corners were shifted up by a factor of three, due to the increase in the loop gain in equation 3 by decreasing C_{fb}.

The CMRR at low-frequencies had a floor of 105dB with no trim. The increased common-mode sensitivity above roughly 5Hz results from the feed-through of the dynamic common-mode through the single-ended feedback capacitors C_{fb}. Shifting to a fully-differential architecture would help to improve the overall CMRR performance.

B. *Noise*

The measured noise floor and the SpectreRF estimates are in excellent agreement. A spectral noise plot is shown in Fig. 11. Measuring noise with an HP 88410A spectrum analyzer, the amplifier noise floor was found to be 0.98µVrms, referred-to-input, over a band from 0.05 and 100Hz for the gain x100 amplifier and 0.83µVrms for the gain x300 amplifier. The 1/f noise corner for the circuit was found to be roughly 1 Hz, a factor of more than 500 lower than for an uncompensated design. The residual 1/f noise results from the output buffer and highpass feedback network, which are uncompensated. The total noise for the system, integrated from 0.05 to 4kHz, was measured to be 1.1µVrms for the 50.5 dB gain diagnostic design, and 1.30µVrms for the 41 dB gain sense-stim design. Note that the modest increase in noise from [19] was caused by the additional noise from the output buffer's filter resistors and slight increase in 1/f noise from lower first-stage gain.

A noise figure of merit helps to establish the quality of the design in comparison to the state-of-the-art. As described in [1], the noise-efficiency-factor (NEF) scales the noise, power and bandwidth of a design against a reference BJT amplifier. The NEF equation must be slightly modified to account for the bandwidth of 120Hz set with the cascaded second order lowpass filter to avoid underestimation,

$$NEF = V_{i,\,rms} * \sqrt{\frac{I_{tot}}{(1.22)Vt\,4kT\,BW}} \quad (1.8)$$

where BW is the net -3dB point, 120Hz, of the cascaded filter. With a total amplifier current draw of 1.05µA (including output buffer and high-pass feedback), the NEF is 4.6 and 5.4 for the 50.5dB and 41dB amplifier, respectively. Comparing this value to recent amplifiers in the literature, the amplifier described here compares favorably to 4.8 for the micropower EEG amplifier in [1], and 9.2 for the chopper stabilized amplifier presented in [15]. A significant advantage of this design is that it maintains low noise scaling even with low supply rails—a major limitation found with the designs in both [15] and [1].

V. Discussion

A. Chopper-Stabilization of Neurophysiological Amplifiers

Brain-machine interfaces and neurophysiological diagnostics could significantly improve the lives of patients. The approaches for accessing neural information are quite diverse, ranging from highly-invasive single cell spike recording to non-invasive measurement of potentials on the skin. A compromise solution could be the measurement of neural field potentials. As described in [2, 4-5], significant useful information can be extracted by monitoring neural field potentials over the cortex with minimally invasive techniques that do no penetrate neural tissue. As circuit designers, the monitoring of NFPs puts the focus on addressing excess noise from the transistors well above theoretical thermal noise expectations. The chopper-stabilized NFP amplifier presented here provides immunity to these excess noise processes, allowing for flexibility to use industry standard small geometry processes with no modification.

Excess noise is not a hypothetical problem: popcorn noise in particular can undermine the fidelity of an NFP amplifier and is a residual problem in some sub-micron processes. Popcorn noise is a defect related noise process, where the spectral characteristics are modeled in the frequency domain by a Lorentzian distribution [22]. Due to gate processing and isolation techniques, popcorn noise in excess of 500μVrms RTI can exist in micropower NFP amplifiers--more than two orders of magnitude above the targeted noise floor. Fig. 13 provides an example of popcorn noise superimposed upon a ramp response for two amplifiers fabricated in a sub-micron CMOS process.

Application of chopper stabilization reduces the susceptibility of the NFP amplifier to these disturbances. The two prototype amplifiers in Fig. 13 were chopper stabilized using the chopper-stabilized amplifier architecture described in this paper. To demonstrate the impact of chopper stabilization, the response of the amplifiers to a slow ramp was measured twice—once with chopper stabilization engaged, once with it disengaged. With the chopper frequency of 16 kHz placed well above the estimated Lorentzian corner of 1 kHz, chopper stabilization eliminates the popcorn noise from the signal band and restores performance to the theoretical thermal noise floor. The mathematical analysis for popcorn noise is similar to the rejection of 1/f noise [16], with the goal of selecting the chopper frequency above the intersection between the popcorn processes' Lorentzian distribution and the amplifier's thermal noise floor. As demonstrated by the low NEF for the prototype in this paper, and additional results illustrated in Fig. 13, the use of the proposed chopper-stabilized amplifier architecture helps to maintain robust signal integrity and inoculate the analog block from potential process issues as biomedical systems push to deeper sub-micron geometries to enable higher on-chip integration.

B. Performance Summary and Comparisons

The chopper instrumentation amplifier developed in this paper has several advantages that make it particularly useful for field potential recording [1,12,14,15,23]. Referencing Table 2, the primary benefit is the low noise performance and immunity to excess noise resulting from the chopper stabilization. Other authors have explored feedback in chopper instrumentation amplifiers, but their implementation requires three orders of magnitude more power for a similar noise floor, and is not suitable for chronic recording [14]. The benefits of this particular topology include the ability to partition the currents efficiently using a folded-cascode architecture. Using the chopper-stabilized folded-cascode also allows for operation off a Li-ion battery down to 1.8V, something that is not feasible with other recent designs for measuring neuronal potentials[1, 15]. One should note that this design does not require high dc accuracy for its intended application. Because the design is inherently ac coupled, the techniques of [25-27] for absolute accuracy were not implemented in this design. Another benefit includes the application of ac feedback to realize front-end gain and the high-pass network. Scaling of sensitivity in the front-end with low-noise on-chip capacitors is an advantage over [15], which requires a ratio of resistors to triode FETs to establish the gain. On-chip capacitors were also used to set the high-pass filter without external components. Since the signal chain is fully integrated, the amplifier can be scaled for large electrode arrays with minimal area penalty.

The die photograph in Fig. 14 shows the aspect ratio of the amplifier. The chopper amplifier, high-pass integrator amplifier and output gain amplifier require $0.7mm^2$ of die area, while the on-chip capacitor requires an additional $1mm^2$. The large area of the capacitor is set by the 0.05Hz highpass pole, which is not required in the majority of NFP measurements [2]. In practice, the pole could be shifted an order-of-magnitude higher in most applications, reducing the area for the amplifier to $0.8mm^2$. This is feasible for NFP measurements, which as shown in Fig. 1 generally sample an area of roughly $1mm^2$; the NFP application does not require the fine pitch of a single-cell recording array [1].

The trade-off of this design compared to other recent work is limited CMRR and polarization headroom. The modest CMRR is generally not an issue in implantable systems [17], where body shielding limits coupling and systems with ~ 40dB CMRR can still yield acceptable recordings; in fact, the finite electrode matching in practical multi-electrode systems makes one question the relative value of CMRR beyond 100dB without a detailed characterization of the electrode system.

The bigger limitation of the design proposed here is the hurdle of suppressing polarization voltages substantially beyond 50mV, while maintaining operation at 1.8V. Designs such as [1] include complete ac coupling of the electrodes to the amplifier, giving them excellent immunity to static polarization potentials. If polarization voltages do extend to the single-volt range, this design would require a substantially higher C_{hp} to balance the input signal. As described in equation 2, this would adversely affect the NEF for the amplifier. However, the NEF penalty is not catastrophic, and even scaling to support a +/-500mV polarization potential would only increase the NEF by two to essentially 10, on par with the chopper design presented in [15]. We should note that the feedback design in [15] is also limited to +/-50mV by the relative scaling gain amplifier's resistor and the feedback transconductor, demonstrating that techniques employing feedback to suppress dc offsets generally suffer from limiting constraints on available headroom. As a note of caution, when discussing building arrays of electrodes for sensing, the design engineer needs to be certain to separate the *differential* polarization offsets that one should expect to see in practice, from the absolute offsets that might exist to the reference electrode for the system. Confusing these values can lead to an over-specified amplifier design.

C. Demonstration of a Brain-Machine Interface

As demonstrated at ISSCC 2007 [19], an intuitive approach to interpreting neuronal activity derived from NFP measurements is to think of the detection system as a "brain radio," where physical location of the electrode maps functionality (motor, sensory, etc) and frequency encodes the activity. Useful diagnostics and algorithms can be constructed by analyzing fluctuations in the power within bands. For example, brain-machine interfaces (BMIs) using the 10 Hz "mu-wave" over sensory-motor cortex signals have been used to control cursors on a screen, while monitoring a patients theta-waves helps to track sleep patterns [6,9]. To demonstrate the suitability of this amplifier for such applications, an electrode was placed over the O2 and A2 regions of the head using the international 10-20 system. This measurement vector provides information on the activity of the visual cortex. Referencing Fig. 15, a distinct band appears from the alpha waves (10Hz) when the subject's eyes are closed and mentally relaxed, which disappear upon opening.

The detection of alpha waves over the cortex allows for the construction of a demonstration brain-controlled actuator shown in Fig. 16: by using a bandpass filter to extract 10Hz brain signals in the alpha band, it has been possible to consistently actuate a light bulb by the controlling alpha activity over the visual cortex by simply opening and closing one's eyes. The alpha band signals are amplified and subsequently rectified and low-pass filtered to produce a dc signal that is proportional to the incoming amplitude. This signal is compared to a long-term average, which consists of a longer time constant low-pass filter; changes in the alpha band content of the EEG spectrum actuates a light bulb. The chopper-stabilized amplifier in this paper enables BMI systems to be used in portable and implanted applications by combining low-noise with power efficiency.

VI. CONCLUSION

This work has introduced a chopper-stabilized amplifier suitable for chronic monitoring of local neural potentials in battery powered applications. The primary goal of these chronic measurement systems is achieving low noise with minimal power drawn from a single-battery. The use of AC feedback around a chopper-stabilized mixer-amplifier eliminates excess 1/f noise without aliasing of signals or noise, thereby providing high fidelity diagnostic measurements. Additional benefits of the architecture include accurate gain and filtering characteristics using on-chip components, with an acceptable CMRR and input impedance for practical applications. Although a neural field potential amplifier was the focus of this prototype, the architecture concept is quite general and can be applied to a large class of sensors that benefit from synchronous demodulation.

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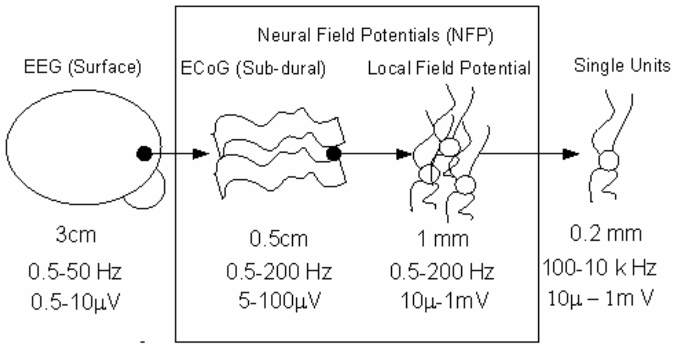

Fig. 1: Relative comparisons of neurological recording technologies, including estimates of spatial resolution, bandwidth and signal levels[1, 2, 4].

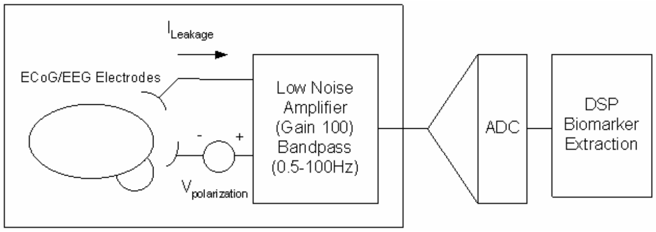

Fig. 2: A typical signal chain for recording neural field potentials. The focus of this paper is on the interface between the neural tissue and the amplification of neural signals prior to digitization.

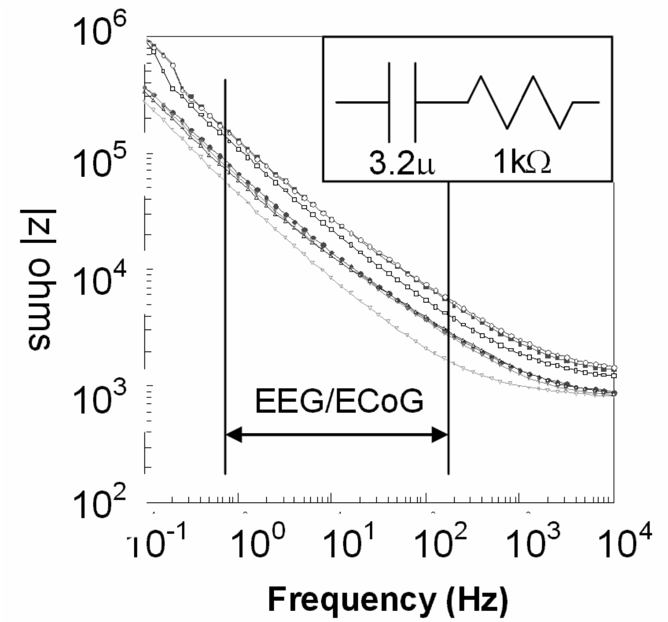

Fig. 3: Impedance sweep of electrodes referenced to a large titanium plate (bottom cluster) and paired-electrode (top cluster) electrochemical interfaces. The electrodes are made of platinum-iridium, with a surface area of $6mm^2$. The equivalent circuit over the NFP region is modeled as a 3.2μF capacitor in series with a 1kΩ resistor.

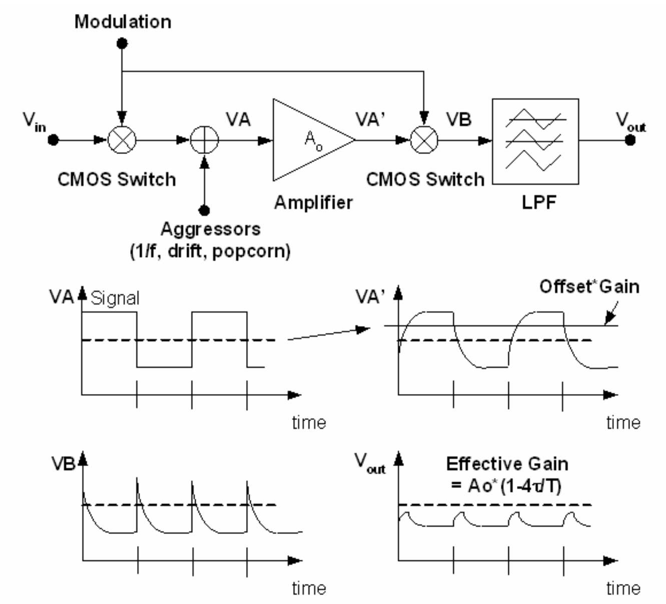

Fig. 4: Distortion and headroom problems encountered with an open-loop, low-power chopper amplifier architecture, assuming a dc input [12]. Note that to simplify the figure, the ac offset signal at VB is not shown.

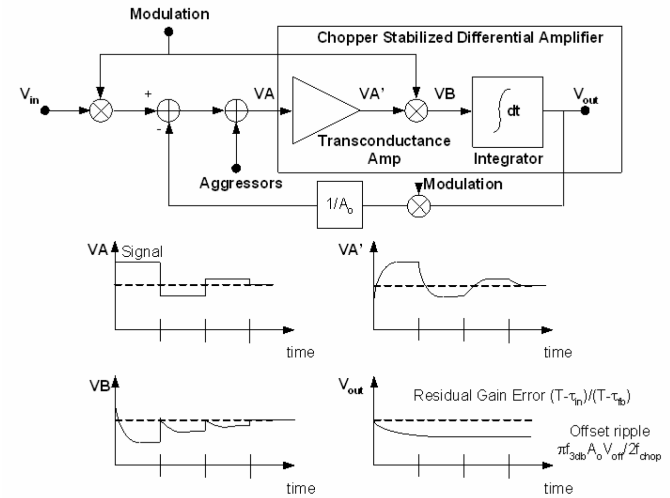

Fig. 5: Feedback of up-modulated signal significantly suppresses distortion and increases headroom.

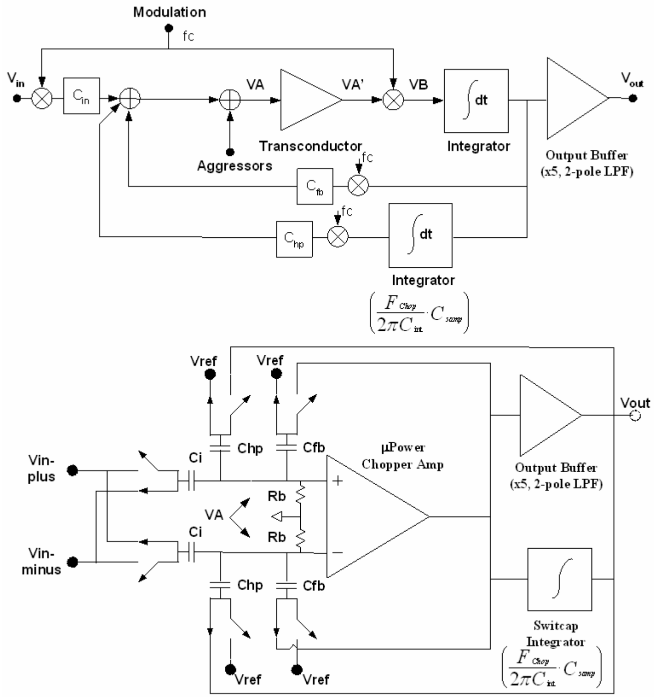

Fig. 6: High-level signal flow graph and circuit architecture of NFP instrumentation amplifier, illustrating the multi-loop feedback paths around the amplifier.

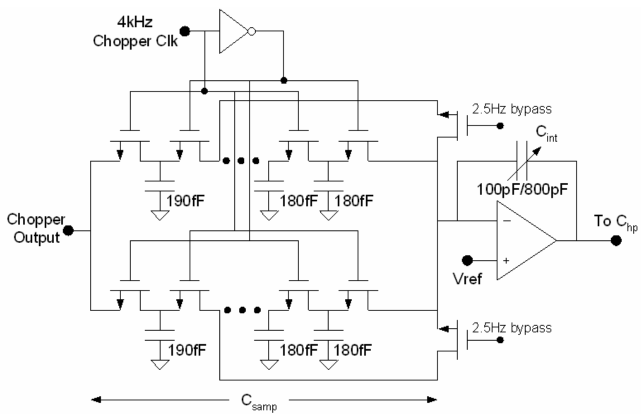

Fig. 7: Switched capacitor integrator for driving the high-pass feedback capacitor, Chp. The summing capacitor "Csamp" is implemented as a parallel branch, each branch composed of a cascade of six capacitors and sampled on alternating phased of the chopper clock. The gain of the integrator is adjusted by switching the value of C_{int} by 6, and tapping off different points along the cascade of sampling capacitors.

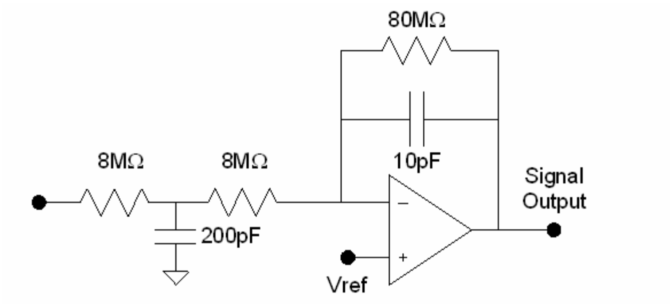

Fig. 8: Output filter and gain amplifier to buffer the chopper and drive the ADC. The continuous time filtering suppresses residual chopper ripple in the signal chain.

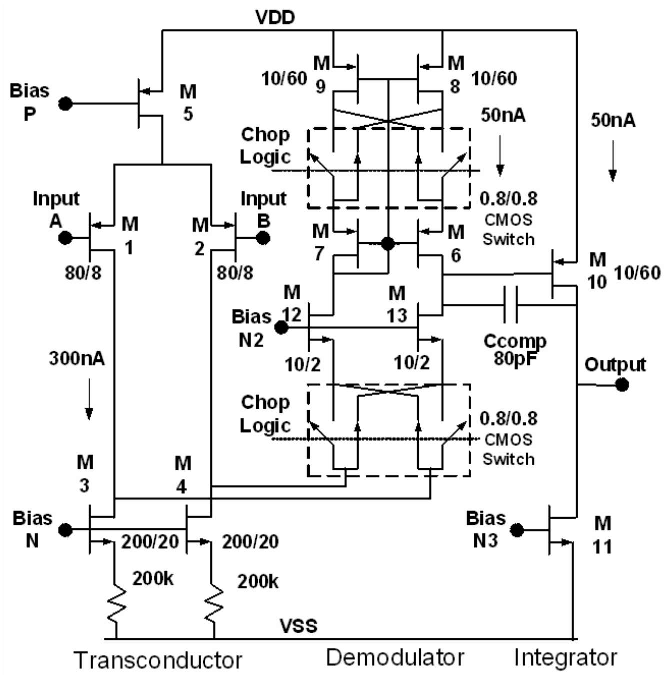

Fig. 9: Adding CMOS modulation switches to a classical folded-cascode amplifier enables the chopper-stabilized amplifier.

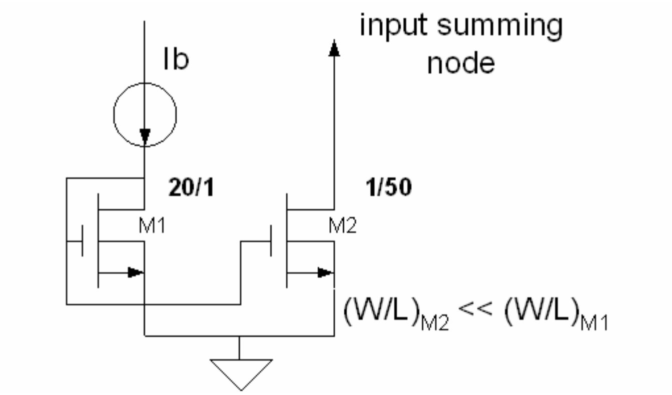

Fig. 10: Long-FET biasing scheme for practical implementation of the monolithic 5 GΩ bias impedance.

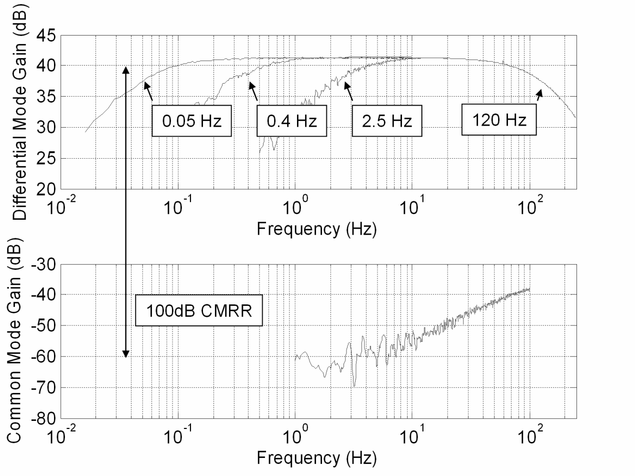

Fig. 11: Differential and common-mode transfer functions of the prototype amplifier in gain 100 mode measured with an HP89410A (buffered through a 10x instrumentation amplifier). The high-pass filter corner is set by digital adjustment of the high-pass integrator time constant.

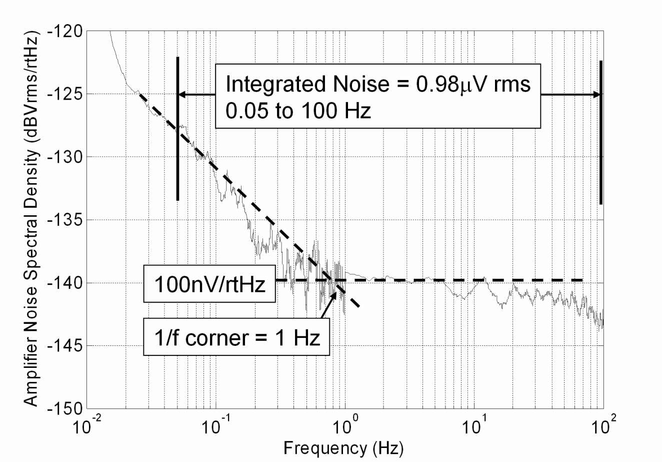

Fig. 12: Noise spectrum acquired with an HP88410A spectrum analyzer; note that two data regions were merged to assemble this figure. Noise estimate is 100nV/rtHz in the passband (-140dBrms/rtHz), with the residual 1/f corner estimated at roughly 1 Hz. The spectral bump at 10mHz and the modest bump at 1Hz is from DC spectral leakage of the HP88410A.

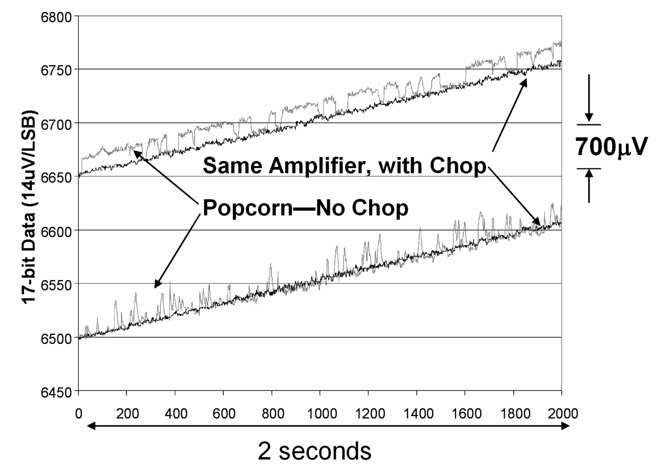

Fig. 13: Suppression of in-band popcorn noise in two prototype amplifiers. Use of the chopper stabilized amplifier architecture proposed results in the stabilized noise floor being set by the theoretical noise limit, not the excess noise.

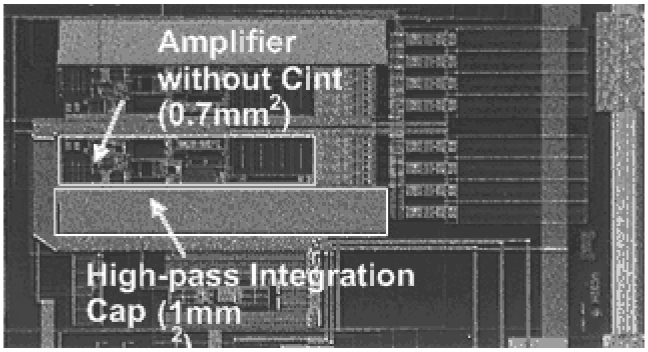

Fig. 14: Die photograph of two prototype amplifiers in the 0.8µm CMOS technology. 60% of the circuit area is taken up by the on-chip capacitor for implementing the 0.05Hz high-pass pole. For most applications, 0.5Hz is sufficient and the total cell area would be $0.7mm^2$ for the chopper amplifier.

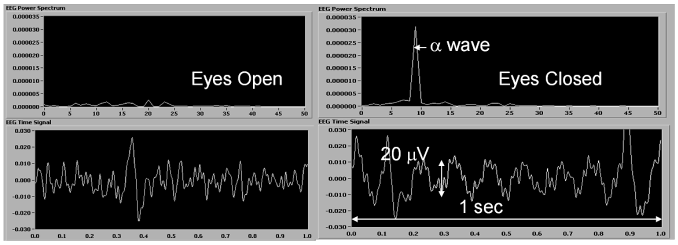

Fig. 15: Spectrogram of surface EEG from visual cortex, demonstrating acceptable signal-to-noise to clearly extract alpha waves corresponding to eye closure; note noise floor of "eyes open" includes cortical noise. Extraction spectral features like these is the basis for several BMIs in the literature [2, 6, 9].

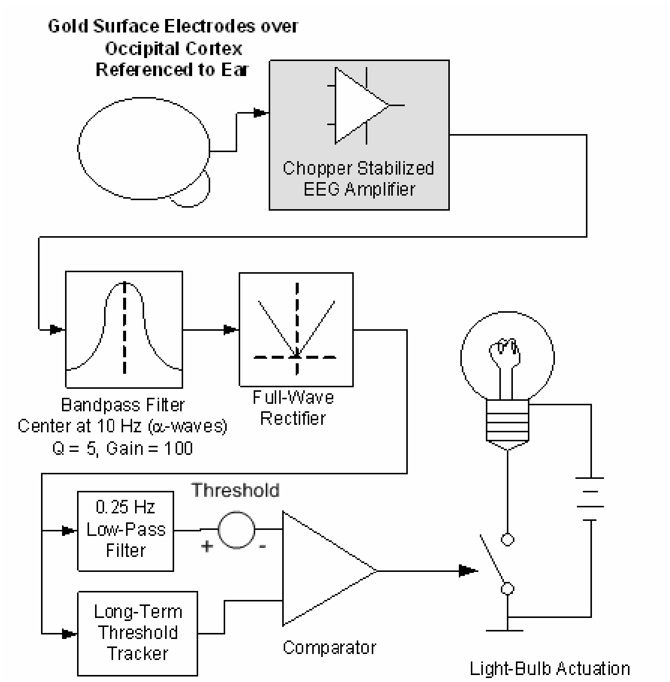

Fig. 16: Prototype of a demonstrative "brain machine interface." The light bulb is actuated by alpha band fluctuations from the visual cortex. The signal to the amplifier increases from 500 nV_{rms} when the eyes are open to 5 μV_{rms} when the eyes are shut and the subject "relaxes", overcoming the threshold to acuate the light.