

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE  
6.775 FINAL PROJECT

John Cooley, Masood Qazi

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## Abstract

This project presents an Analog to Digital Converter (ADC) in a  $0.18\mu\text{m}$  CMOS technology. A pipeline architecture is utilized to present a balanced tradeoff between accuracy, power, and area.

## 1 Overview

The analog to digital converter implements the following relation:

$$\begin{aligned}
 v_{IN} &\in (v_{ADC}, v_{ADC} + V_{LSB}) \\
 v_{ADC} &= -V_{REF} + \\
 &\quad 2V_{REF} \left( \frac{D[N]}{2} + \frac{D[N-1]}{2} + \dots + \frac{D[0]}{2^N} \right) \\
 v_{LSB} &= \frac{2V_{REF}}{2^N}
 \end{aligned} \tag{1}$$

which discretizes the input voltage  $v_{IN}$  into  $2^{10}$  bins indexed by the 10-bit digital code  $D[9 : 0]$ . The binning of input values is depicted in Fig. 1 (for  $N = 10$ ).

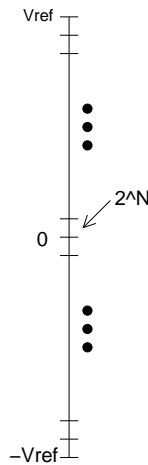


Figure 1: The input voltage is discretized into  $2^N$  bins.

Shown in Fig. 2, is a top-level block diagram of the pipelined ADC system. One can see that each basic stage gives two bits of information and passes on a residue signal—produced by the MDAC from the two FLASH ADC bits and  $v_{IN}$  of the current stage—for an additional two bits from the next stage. This allows for a simple FLASH subrange ADC that requires only three comparators. In the next section, the design of each of the building blocks will be discussed in addition to a digital error correction technique. Finally, simulations results will be presented in the last section.

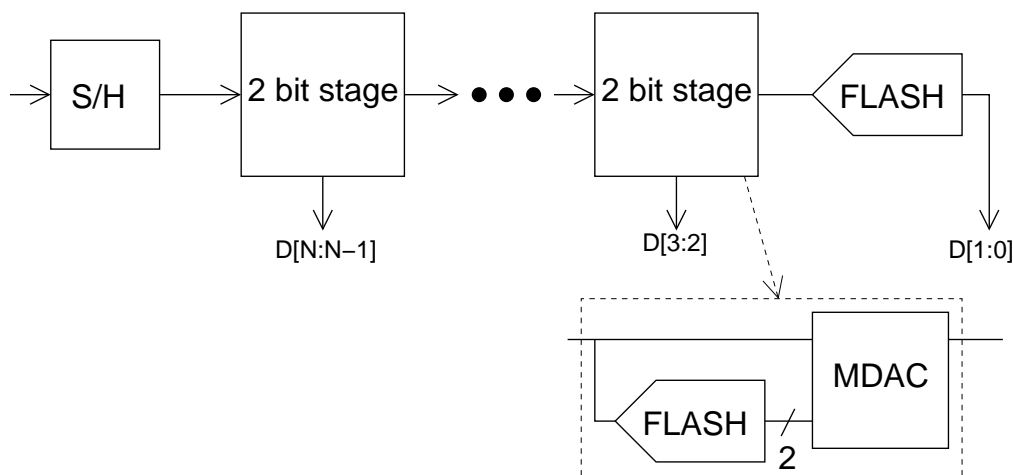


Figure 2: Shown is a top-level block diagram of the ADC system

## 2 Design

### 2.1 2-bit Flash ADC

Each stage of the pipelined ADC has a 2-bit Flash ADC. The Flash ADC is shown in Figure 6. The Flash ADC has three comparators that each compare the input voltage for the stage (input or residue voltage) with a fixed reference or threshold potential. The overall reference voltage for the Flash ADC is 1.4 V or  $\pm 0.7$  V (supply voltages are  $\pm 0.9$  V). The threshold potentials are created with a resistor ladder (-0.35V, 0V, +0.35V). The comparators are implemented as single-stage diff-amps. One design issue with the comparators is that they need to operate for large-signal (as opposed to small-signal) input voltage deviations. The inputs to the diff-amps are buffered with voltage follower circuits in order to allow for the wide input voltage range. For example, with an input voltage close the positive supply, the voltage presented to the diff-amp input device is guaranteed to be one  $V_{gs}$  below the actual input voltage. This level-shift allows the diff-amp to operate with high input voltages. Level-shifting both inputs equally ensures the proper comparator transfer function. The input voltage range with the buffered inputs is wide enough to include the three reference potentials for the Flash ADC. The transfer functions of the three Flash ADC comparators are shown in Figures 3, 4, and 5.

The comparator topology was chosen because it provides a simple solution for the requirements of the Flash ADC. The voltage followers on the inputs are sufficient to allow the input devices in the diff amps to conduct for most of the input voltage range. The gain of the comparators (measured as the slope of the  $v_{out}/v_{in}$  curve at the transition) is 110 (40 dB). The systematic input-referred offset of the comparators (measured as the difference between the input voltage at the output voltage zero-crossing and the threshold voltage) is 4 mV.

In order to implement a pipelined ADC with 10-bits of accuracy and with no Digital Error Correction (DEC), each comparator needs to be accurate to the accuracy of the full ADC.

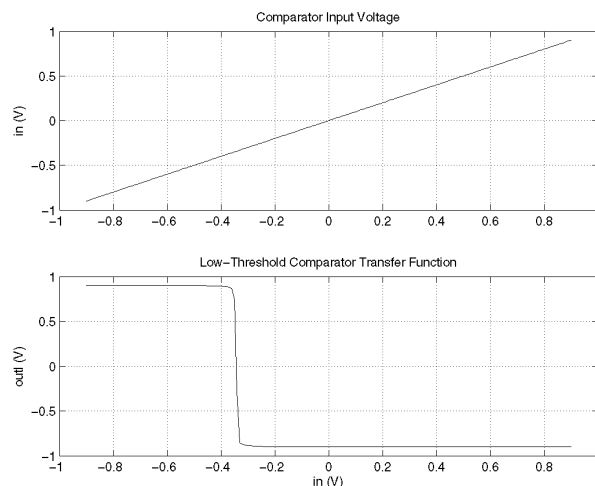


Figure 3: The transfer function of the low-threshold comparator.

In our case this would constrain the input-referred offset voltage of the comparators to be less than  $\frac{1}{2}V_{LSB} = 680\mu\text{V}$ . Increasing the gain of the comparator would decrease the input-referred offset. We define the accuracy of an ADC as the effective number of noise-free bits available at its output and the resolution as the input voltage deviation necessary to change the output code by one LSB. Because we employ DEC, the input-referred offset of the comparators is not constrained by the accuracy of the full ADC. Instead it is only constrained by the resolution of the current stage Flash ADC. That means that the offset of the comparators needs to be less than  $\frac{1}{2}V_{LSB,stage} = 175\text{mV}$ . Therefore, the measured input-referred offset of the comparators is safely within the accuracy requirement for the DEC pipelined topology.

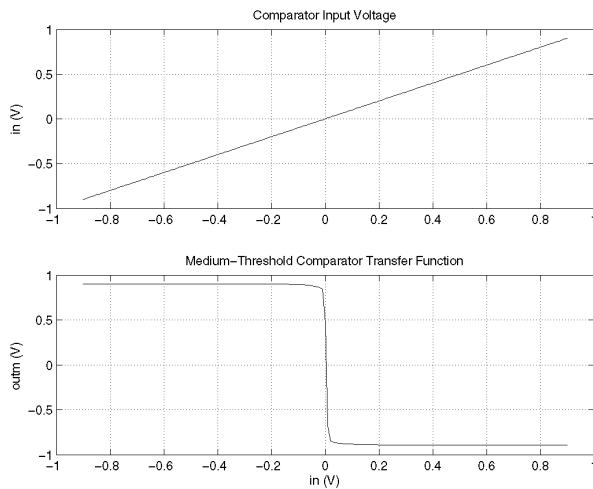


Figure 4: The transfer function of the middle-threshold comparator.

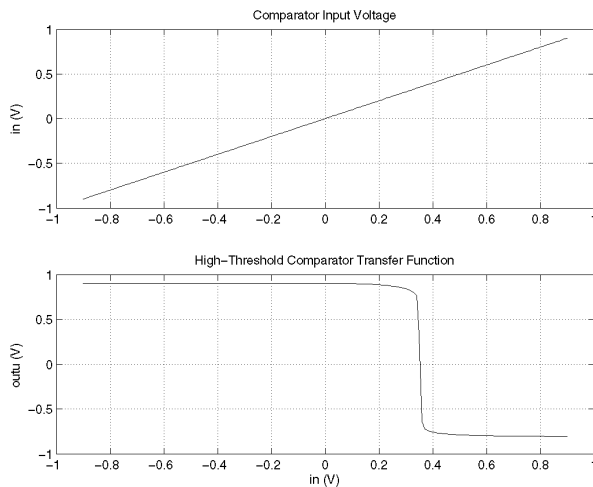


Figure 5: The transfer function of the upper-threshold comparator.

## 2.2 Closed-Loop Sample-and-Hold

The pipelined ADC has one sample-and-hold (S/H) at the input to the first stage. This S/H allows the first stage ADC time to decide on its digital output code without the input voltage changing during that time. The S/H topology that we chose is a switched-cap closed-loop offset canceling S/H. The schematic of the S/H is shown in Figure 7.

The S/H circuit has two phases, “sample” and “hold.” During the sample phase, the op-amp is connected in unity-gain feedback and the voltage ( $v_{in} - v_{os}$ ) is stored on the sampling capacitor, where  $v_{os}$  is the input-referred offset voltage of the op-amp. In the hold phase, the sampling capacitor is connected from the inverting input terminal to the output terminal. The output voltage of the op-amp during this phase is  $v_{in}$  regardless of the input-referred offset voltage of the op-

amp. Also, the output voltage is a low-impedance voltage source due to the op-amp. Plots of a piecewise-linear input voltage to the S/H and the resulting output voltage waveform are shown in Figures 8 and 9 respectively.

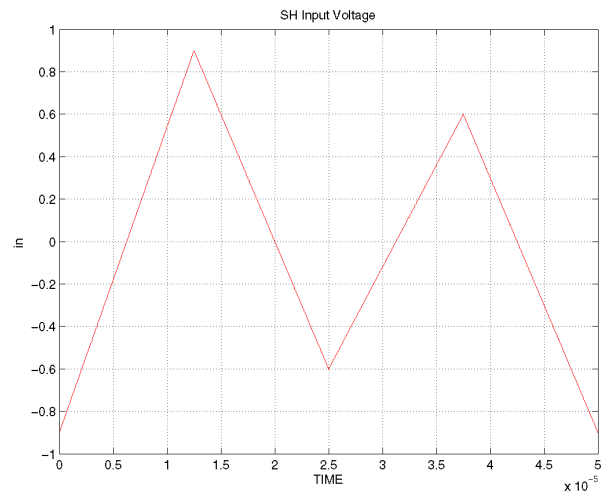


Figure 8: The piecewise-linear input voltage to the S/H for simulation.

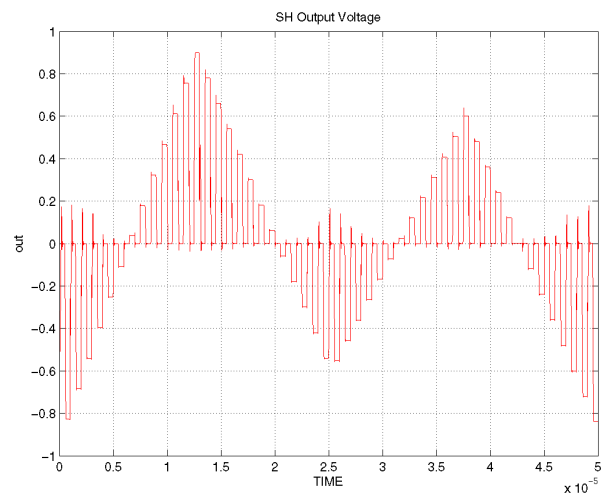


Figure 9: The sampled output voltage of the S/H resulting from the piecewise-linear input voltage.

Once the input-referred offset of the op-amp has been canceled, the dominant source of error in the S/H circuit is charge injection. This is the result of switches turning off and storing some of their channel charge on the sampling capacitor. In order to reduce the error due to charge injection, we increase the sampling capacitor because the larger the capacitance, the smaller voltage change will result from the same amount of extra charge. Also, by increasing the sampling capacitor, the sampled noise that appears at the output of the S/H is reduced. This is because one source of sampled noise is the  $\frac{kT}{C_s}$  total voltage noise sampled on  $C_s$  from the thermal noise

in the input switch. At  $C_s = 1\text{pF}$  this term is  $64\mu V_{rms}$  and it decreases as we increase  $C_s$ . This term is added in quadrature with the sampled noise due to the voltage noise of the op-amp whose bandwidth is dominated by the internal compensation capacitor  $C_c$ .

We measured the offset error at the output of the S/H due to charge injection by comparing the sampled input voltage to the output voltage for that sample. Figures 10 and 11 show how this offset was measured for one particular sample. Figure 12 shows plots of the measured total sampled noise and offset error for varying sampling capacitances. Based on those plots we chose a sampling capacitor value of 5 pF. The resulting offset error for this sampling capacitor was  $410\ \mu\text{V}$  and the sampled output noise was  $162\ \mu\text{V}_{ac,rms}$ .

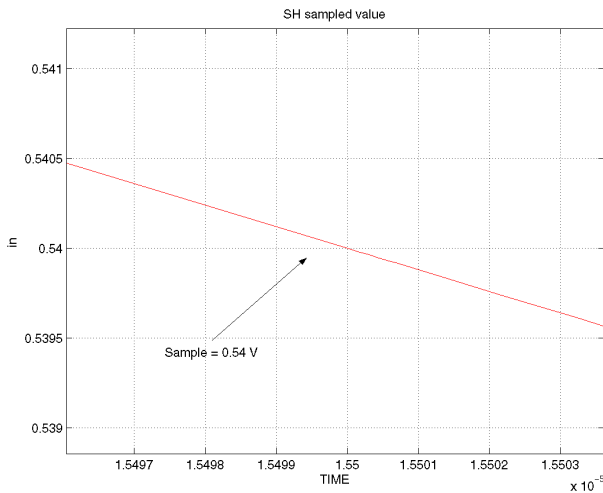


Figure 10: A “zoom-in” of the input voltage sample for the S/H circuit.

It turns out that the offset error due to the S/H is not as limiting as it seems. This is because of the timing of the two switches that connect the sampling capacitor in the sample phase. The switch which disconnects the sampling capacitor from the input voltage has a control signal which is delayed from the control signal for the other sample phase switch. This means that only the charge injection from the feedback sampling sample phase switch injects its charge onto the sampling capacitor. This charge is constant to a first order approximation because the voltage at the inverting input to the op-amp is fixed. Once the input switch is turned off, the other side of the capacitor is floating and its charge must be fixed. Therefore, the charge injection error is input-voltage-independent. The result is that the charge injection error creates a constant dc offset. This dc offset can be dealt with through calibration techniques. In Figure 7, the delay between the control signals for the two sample phase switches is created with a cascade of two inverters.

Shown in Fig. 13 is the top-level schematic of the system. Reading from left to right across the top one can see the input S/H, followed by pipeline stages, and terminated with a flash ADC, which matches the outline of Fig. 2. One can

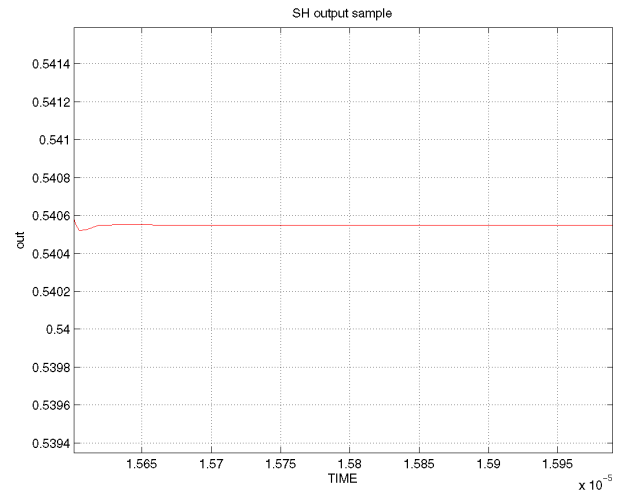


Figure 11: A “zoom-in” of the output voltage sample for the S/H circuit corresponding to the input voltage sample shown above. The offset error can be measured as the difference between the sampled input voltage and the output voltage sample.

also see latches at the bottom to store the bits determined by early stages so that the information does not get lost as new samples are fed into the first stage. Finally, one can see the digital error correction for the first three stages (four MSBs) at the end of the pipeline of latches.

## 2.3 Multiplying ADC (MDAC)

The MDAC implements the following relation:

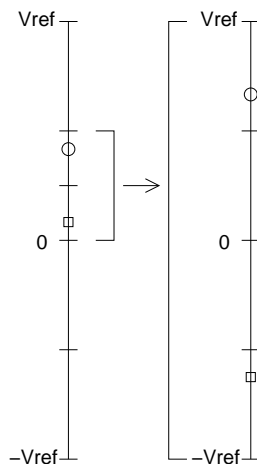
$$v[n + 1/2] = 4 \times (v_{IN}[n] - v_{DAC}[n])$$

$$v_{DAC}[n] = V_{REF} \left[ \frac{1}{2}(D[1] - \bar{D}[1]) + \frac{1}{4}(D[0] - \bar{D}[0]) \right]$$

where  $D[1 : 0]$  are bits determined from logic applied to the output of three comparators whose thresholds are  $(-V_{ref}/2, 0, +V_{ref}/2)$ .

This process is pictorially represented for two example inputs (circle and square) in Fig. 14. The code 0b00 indexes the lowest quarter segment and the code 0b11 indexes the uppermost quarter segment. Note, that the MDAC requires correct functionality of the 2bit ADC in order to subtract the appropriate  $v_{DAC}$  before amplifying by 4. Otherwise, the output residue will be outside the meaningful range of the comparator inputs for the next stage.

To mitigate the effect of comparator offset, the first two stages implement one bit out of two for error correction. This is accomplished by changing the gain of the MDAC from 4 to 2. Also the MSB of the subsequent stage is added to the LSB of the previous stage. This scheme relaxes the comparator offset requirement by a factor of two for each stage of error correction. Since we have two stages with error correction, our comparator offset requirement (roughly  $1.5\text{mV}$ ) is relaxed



fore, stage B is necessarily in  $\phi_1$ .

Figure 14: A pictorial representation of the standard MDAC operating for two example inputs (circle and square).

by a factor of four. The effect of the addition, introduces a systematic offset in the output codes which can be simply subtracted in the digital domain if necessary. In order to handle possible overflow conditions, three cascaded full adder circuits perform the addition and the final carry out bit is interpreted as an eleventh bit. Although the output codes are 11 bits long, they will exercise only  $2^{10}$  different possible values. The full adder connections are shown in Fig. 15.

Also, the standard gain of 4 MDAC and the error correction gain of 2 MDAC are shown in Fig 16. The opamp in the circuits produces the desired transfer function because the charge on all the unit capacitors is conserved.

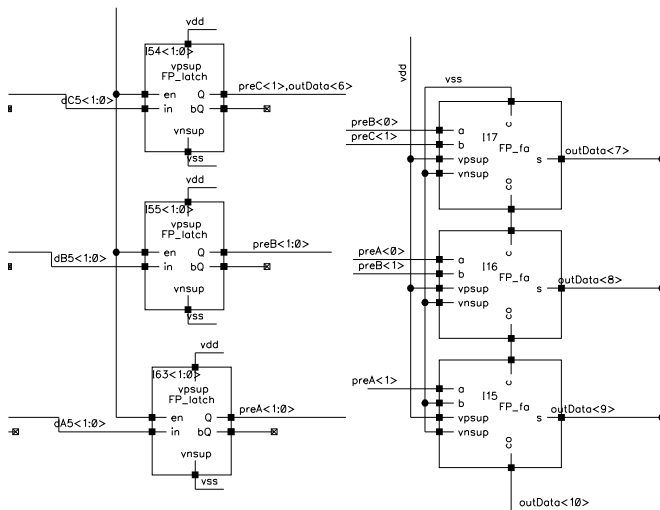


Figure 15: The digital error correction is implemented by three cascaded full adders at the final stage of raw digital output.

Finally, the stages are cascaded by alternating the clocking signals as in Fig. 17. When stage A is in  $\phi_2$ , it is driving an output value onto the sampling capacitors of stage B. There-

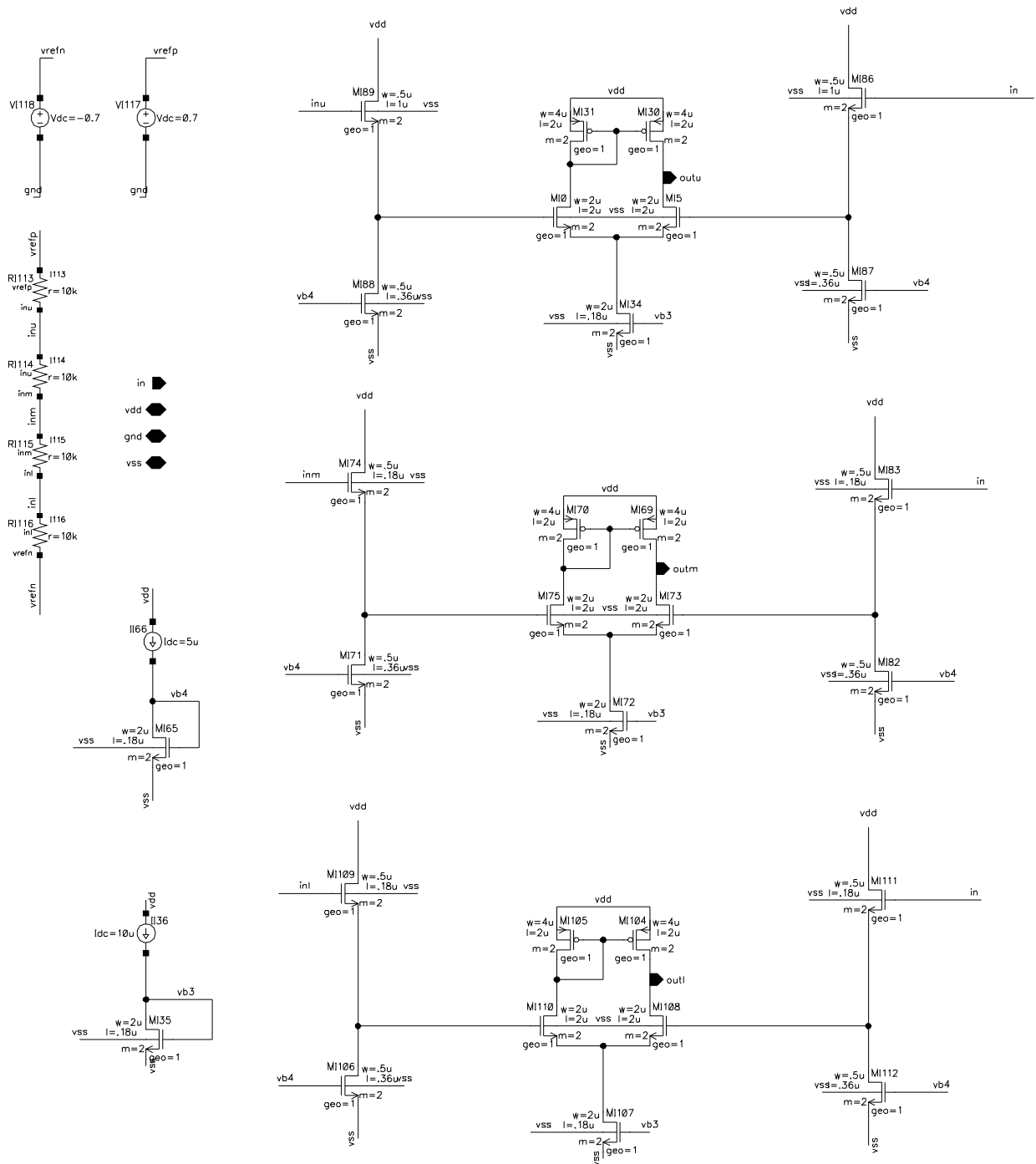


Figure 6: The full schematic of the Flash ADC. Three comparators compare the stage input voltage to fixed reference potentials.

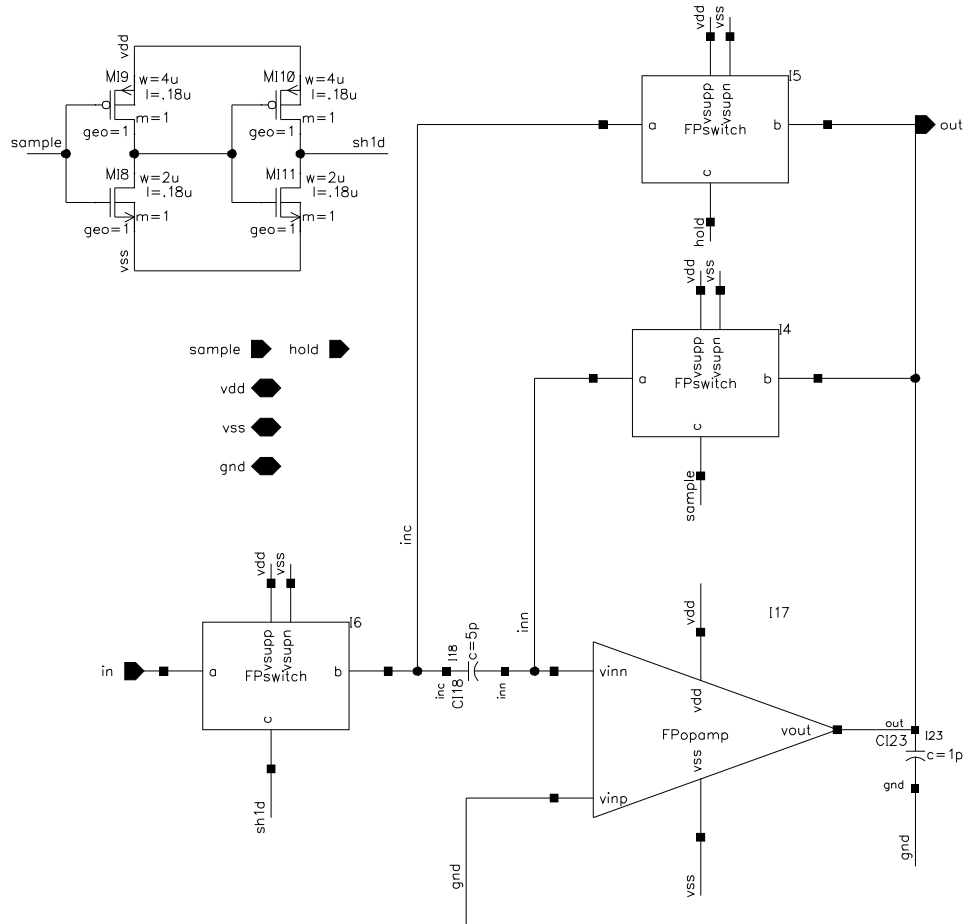


Figure 7: The schematic of the sample and hold circuit.

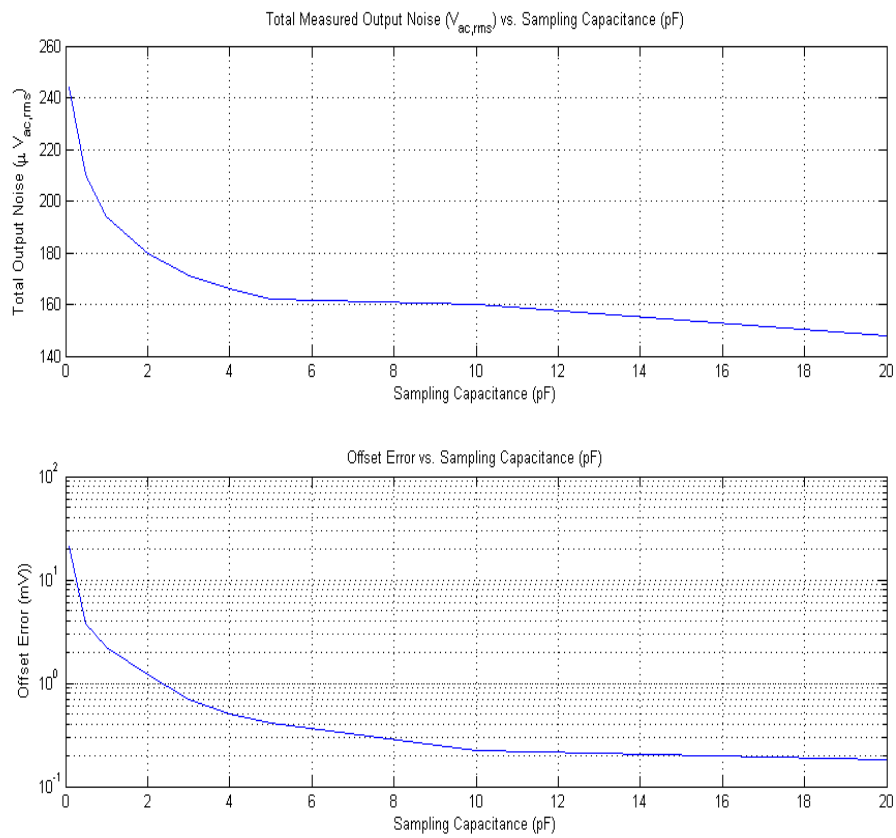


Figure 12: Plots of the measured  $kT/C$  total sampled thermal noise at the output of the S/H and the measured offset error due to charge injection for varying sampling capacitance values.

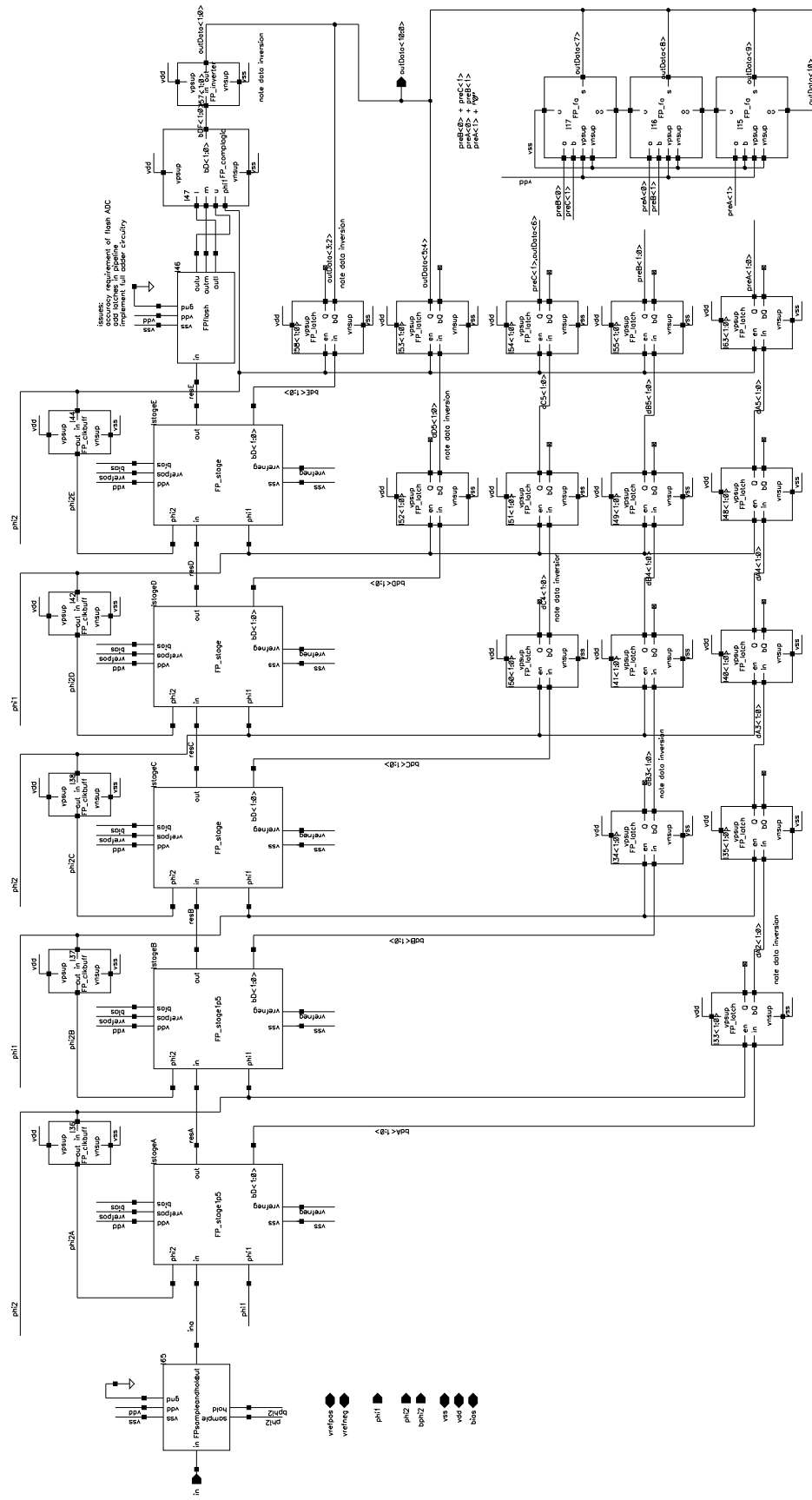


Figure 13: Shown is a top-level schematic of the ADC system

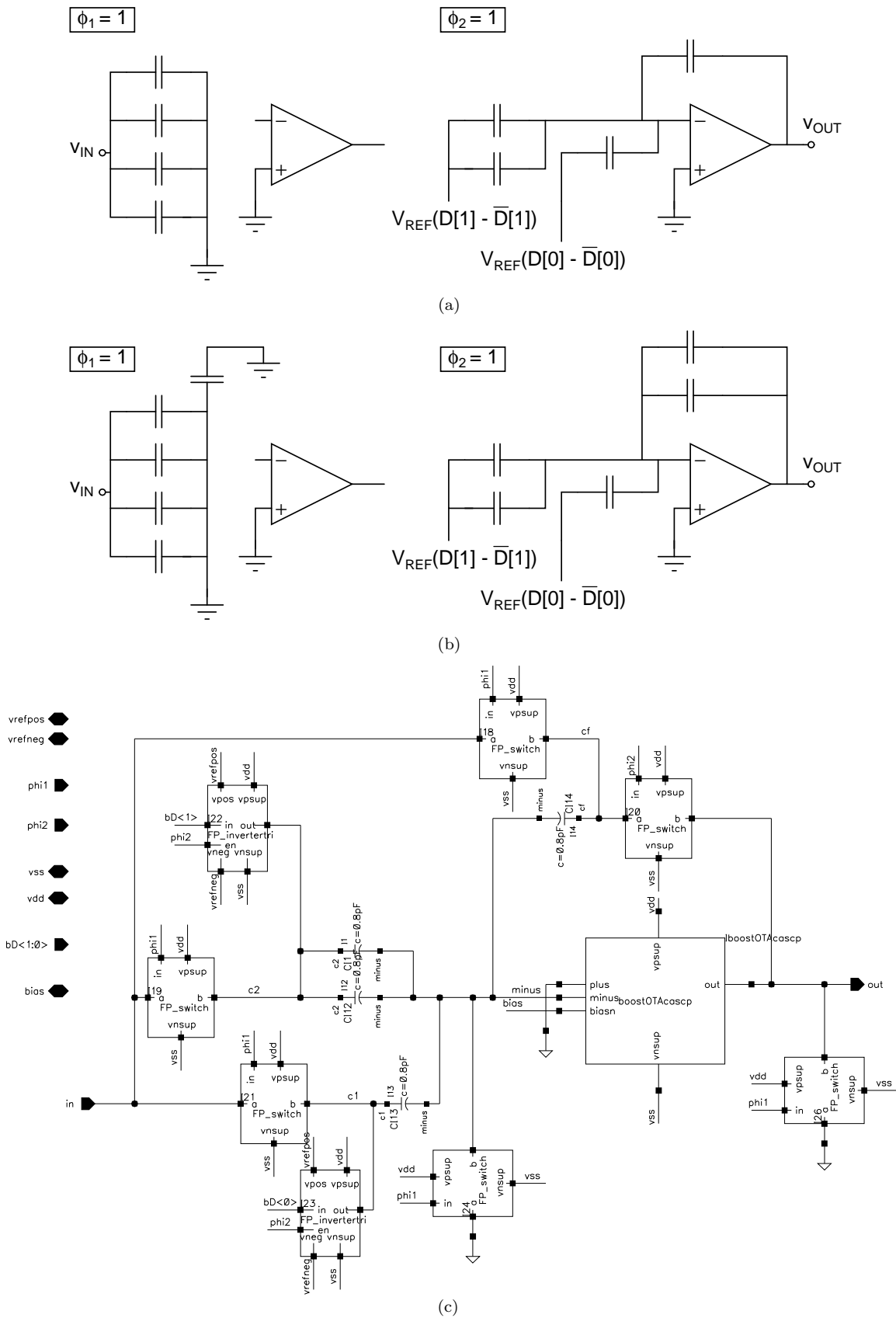


Figure 16: The “x4” MDAC (a) and “x2” MDAC (b) implement the discrete time relation between  $v_{OUT}[n + 1/2]$  and  $v_{in}$  by switching the sampling capacitors as shown. The actual circuit with switches is presented in (c).

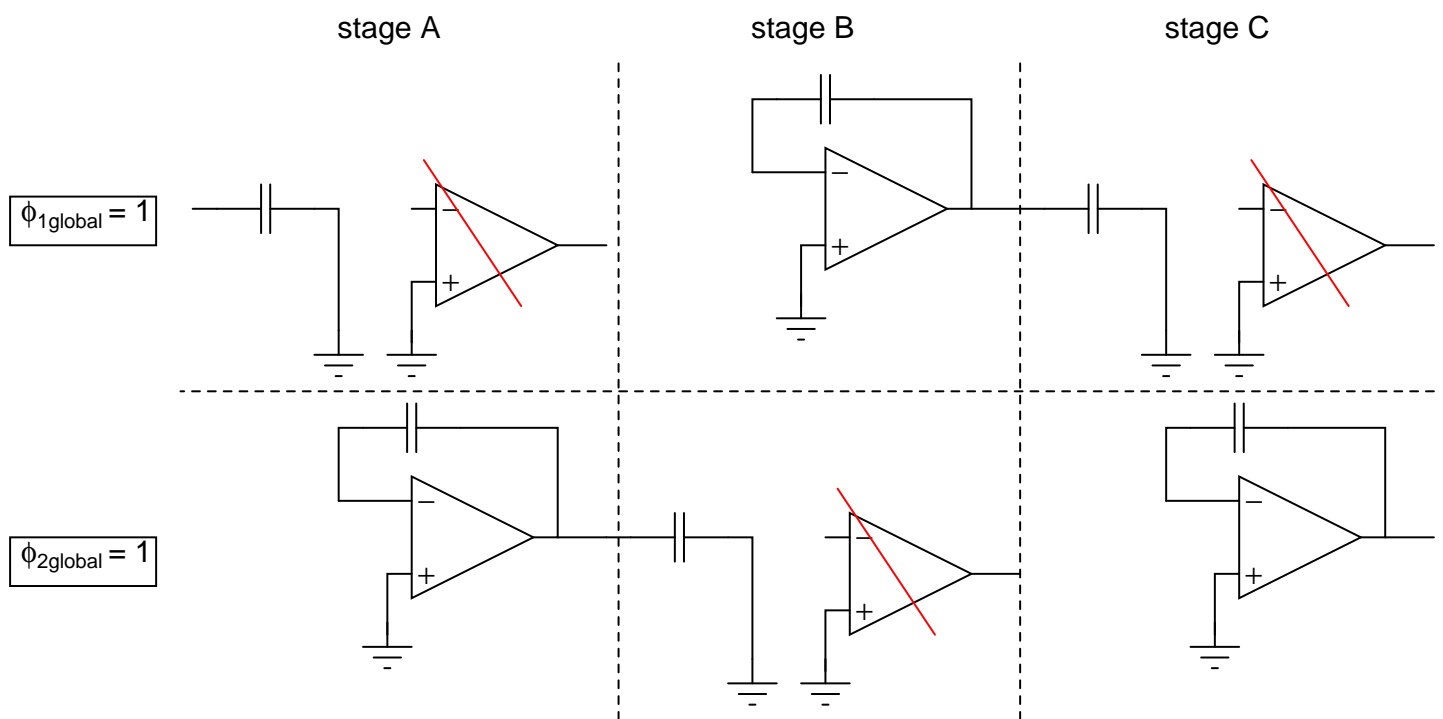


Figure 17: The stages are connected by alternating the clocking signals

### 3 Simulation Results

Shown in Fig. 18 is the result of a transient simulation of the full system on an input sinewave:

$$v_{IN} = 0.69 \sin(2 * \pi 100 \text{kHz} t)$$

Shown in Fig. 19 is a plot of the spectrum output for a test tone with  $f_{in} = \frac{1}{10} f_s$ . The SNDR was  $39.51 \text{dB}$  so the ENOB is:

$$\text{ENOB} = \frac{39.51 - 1.8}{6} \approx 6.29$$

The power consumption was  $2.7 \text{mW}$  and the sampling rate was  $1 \text{MS/s}$ . Therefore, the figure of merit is:

$$\text{FOM} = \frac{2.7 \text{mW}}{1 \text{MHz} \cdot 2^{6.29}} = 34.5 \text{pJ}$$

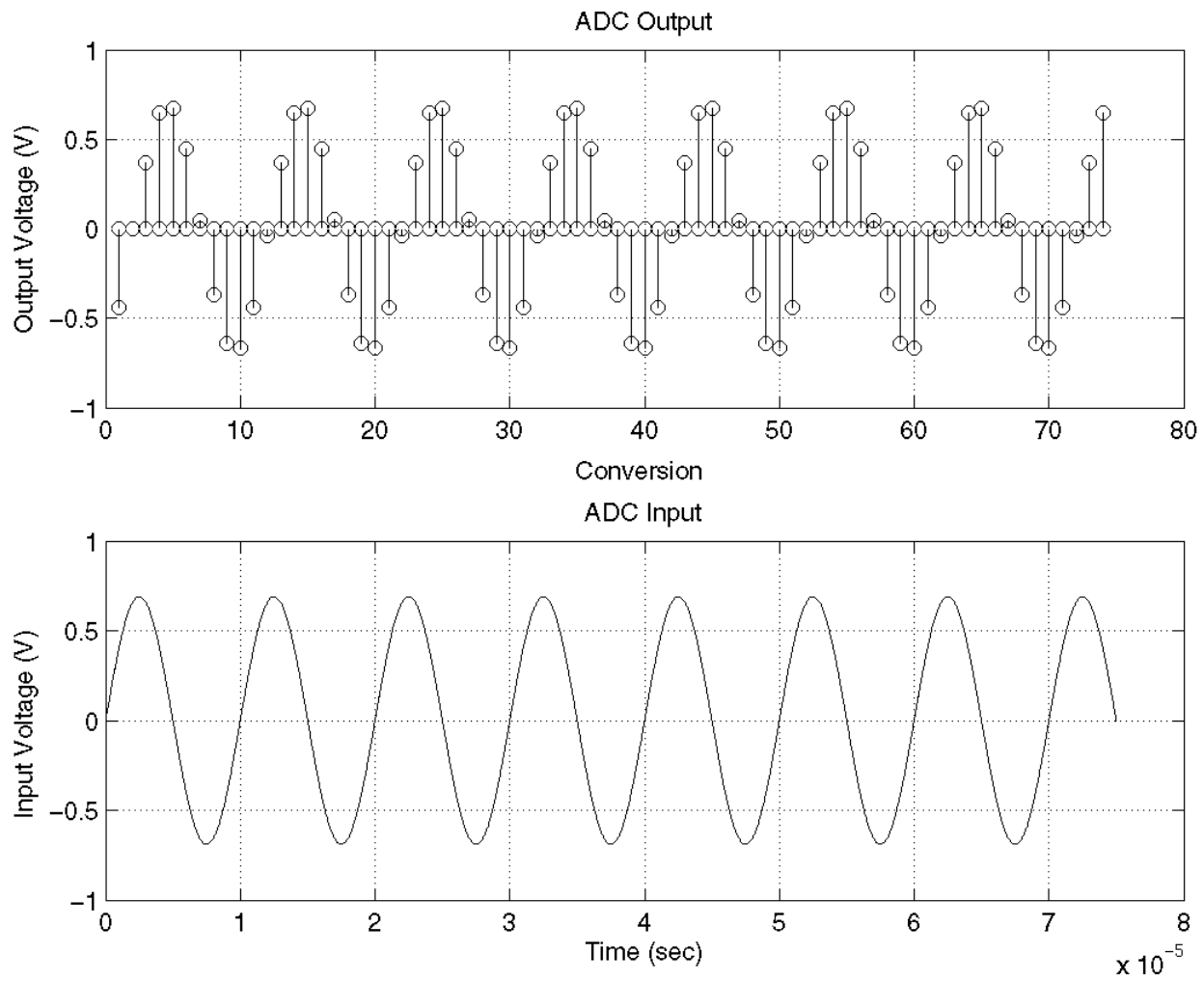


Figure 18: The sequence of digitized samples (above) form a good approximation to the input sinewave (below).

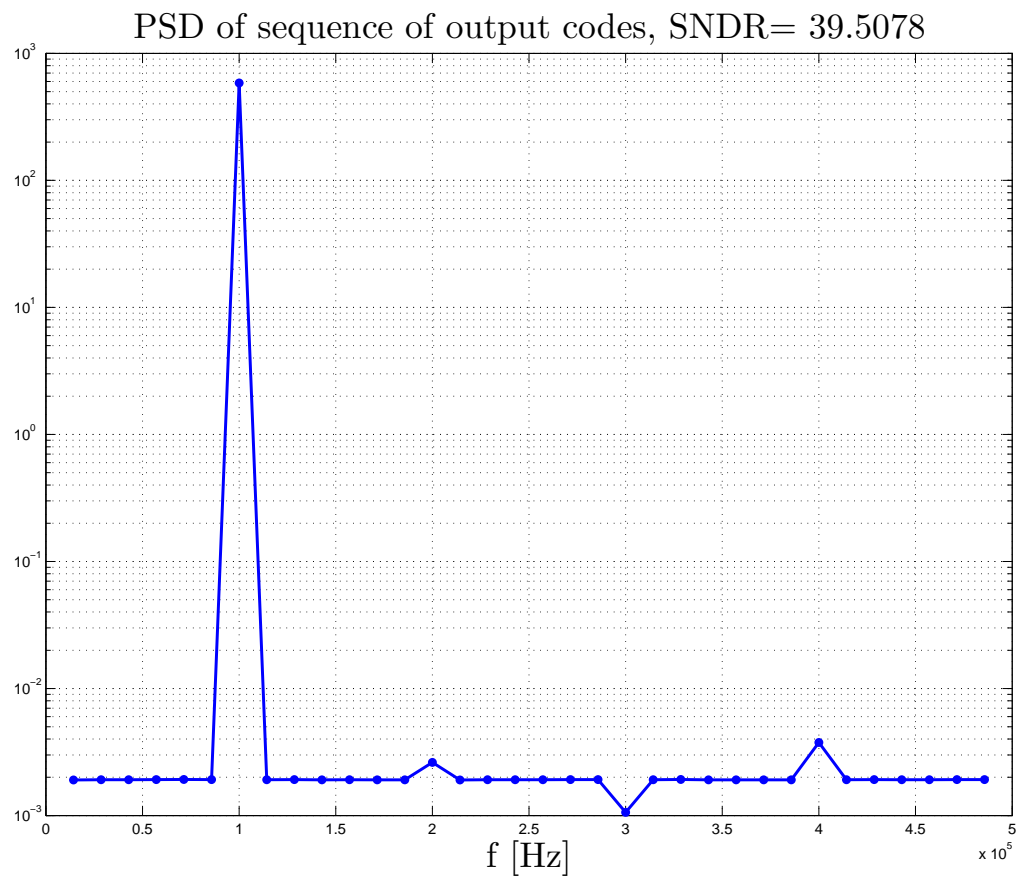


Figure 19: The PSD of the output codes shows good SNDR.

## References

- [1] S.-M. Yoo, J.-B. Park, H.-S. Yang, H.-H. Bae, K.-H. Moon, H.-J. Park, S.-H. Lee, and J.-H. Kim, "A 10 b 150 ms/s 123 mw 0.18  $\mu$ m cmos pipelined adc," 2003, pp. 326–497 vol.1, iS:.
- [2] Y.-J. Cho, K.-H. Lee, H.-C. Choi, Y.-J. Kim, K.-J. Moon, S.-H. Lee, S.-B. Hyun, and S.-S. Park, "A dual-channel 6b 1gs/s 0.18 $\mu$ m cmos adc for ultra wide-band communication systems," 2006, pp. 339–342, iS:.