All-Optical Processing for Ultrafast Data Networks Using Semiconductor Optical Amplifiers

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Ph.D. Thesis Defense

Thesis Committee: Professor Erich P. Ippen, Dr. Scott A. Hamilton, Professor Rajeev J. Ram
Today’s Data Networks

- Transmission over optical fiber
  - Wavelength division multiplexing (WDM): multiple wavelength channels per fiber
  - Erbium-doped fiber amplifiers (EDFAs): multi-wavelength amplification
  - Electronic regenerators with O/E/O conversion & demultiplexing
- Electronic routers with O/E/O conversion & demultiplexing

- WDM: 80+ channels, 10-40 Gb/s per channel
- EDFA: 60-80 km spacing
- Regenerator: Every 2-3 spans (120-240 km)
- Routers: 100+ ports with 1+ Tb/s throughput
Increasing Demand for Capacity

U.S. Internet Traffic*

Year

PB/month
0 100 200 300 400 500 600 700

*Odlyzko et al., “Internet Growth Trends and Moore’s Law”  
http://www.dtc.umn.edu/mints/igrowth.html

Global Projected Traffic Growth**

PB/month
0 10,000 20,000 30,000

**Cisco, “The Exabyte Era”, 2008

- Steady growth estimated at 50%-100% / year
- Increasing video traffic (YouTube, IPTV, Video on Demand)
- High-end users: storage networks, data centers, grid computing, scientific processing
- Growing number of internet users around the world

Increasing channel bit rates and number of channels
Outline

• Motivation/Background
• Ultrafast all-optical logic gates
• Routing: 40-Gb/s all-optical header processing
• Performance optimization of optical logic gates
• Regeneration
• Future SOA-MZI gates
• Conclusion
Motivation/Background: Why all-optical processing?
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
- Performance optimization of optical logic gates
- Regeneration
- Future SOA-MZI gates
- Conclusion
Optical Signal Processing

- Ultrafast performance
  - Capable of 100-Gb/s bitwise switching, 640-Gb/s wavelength conversion
- Channel-rate processing
  - No demultiplexing to lower bit-rates
- Fewer O/E/O conversions
- Network flexibility
  - Payload transparency to bit rate & modulation format

Decrease size, power, weight → COST
Outline

• Motivation/Background: Routing and Regeneration
  • Ultrafast all-optical logic gates
  • Routing: 40-Gb/s all-optical header processing
  • Performance optimization of optical logic gates
• Regeneration
• Future SOA-MZI gates
• Conclusion
**Routers: All Electronic**

- **Challenges with increasing bit rates:**
  - Limited electronic switch speeds (10-40 Gb/s)
  - Requires multiple lower-speed channels
  - Duplication of low-speed O/E/O, buffers, switches
  - Requires conversion and storage of every bit
Routers: All-Optical Header Processing

- **Router functions:**
  - Routing
  - Forwarding
  - Contention resolution
  - Buffering
  - Switching

- **All-optical payload path:**
  - High-speed optical switching capable of channel-rate processing
  - Reduce O/E/O conversions (reduce size, weight, and power consumption)
  - Offers payload transparency for flexible networking

- **All-optical packet processing:**
  - Reduce packet processing latencies
  - Minimize buffering requirements
The Need for Regeneration

- Linear and nonlinear effects in optical fiber
- Dispersion compensation cancels 2\textsuperscript{nd} order dispersion
- Amplifiers compensate for loss
- Amplitude variation
- Pulse shape distortion
- Timing jitter (not simulated)
  - Due to amplifier and transmitter noise
Electronic and Optical Regeneration

- All-optical regenerator
  - High-speed optical switching capable of channel-rate processing
  - Reduce O/E/O conversions
  - Size, weight, power improvements
Challenges for All-Optical Signal Processing

• Challenges
  – Electronic technology more mature and offers more functionality than optical switches
  – Optical switches still costly compared with electronic techniques

• This thesis
  – Demonstrate increased functionality for all-optical processing
  – Improve practicality of all-optical logic gates
Outline

• Motivation/Background

• **Ultrafast all-optical logic gates**

• Routing: 40-Gb/s all-optical header processing

• Performance optimization of optical logic gates

• Regeneration

• Future SOA-MZI gates

• Conclusion
Ultrafast Interferometric All-Optical Switching

- Interferometric switch: change index of refraction (phase)
- Ultrafast performance
- Spatial switching

**Fiber**
- Weak nonlinearity ($10^{-16}$ cm²/W)
- Fast response (~fs)
- No integration – long lengths required

**Photonic crystal fiber, highly nonlinear fiber**
- Fast, strong nonlinearity
- Integration potential?

**Semiconductor optical amplifier**
- Strong nonlinearity (~$10^{-12}$ cm²/W)
- Slow recovery time (~100 ps)
- Potential for integration (semiconductor processes)

**Quantum dot SOA**
- Fast recovery time (~10 ps)
- Strong nonlinearity?
SOA Operation

- Interaction of optical waves with SOA carriers
  - Stimulated recombination of electrons and holes creates gain
  - Optical waves change carrier distribution
  - Changes gain and index of refraction $\rightarrow$ optical switching
SOA Operation

- Interaction of optical waves with SOA carriers
  - Stimulated recombination of electrons and holes creates gain
  - Optical waves change carrier distribution
  - Changes gain and index of refraction $\rightarrow$ optical switching

- How does the incident light affect the carrier density?
  - Phenomenological model
  - Focus on time scales $\sim$ 10 ps (100 Gb/s)
A Phenomenological Model

Key assumptions:

\[ \text{gain} = a(N - N_o) \]
\[ \text{index} = \alpha \cdot \text{gain} \]

Rate equation describing carrier evolution:

\[
\frac{\partial N}{\partial t} = D \nabla^2 N + \frac{I}{qV} - \frac{N}{\tau_c} - \frac{a(N - N_o)}{\hbar \omega} |E|^2,
\]

- Carrier diffusion
- Spontaneous recombination
- Stimulated recombination
- Current injection

V = volume
N = carrier density

A Phenomenological Model

Key assumptions:

\[ \text{gain} = a(N - N_o) \]
\[ \text{index} = \alpha \cdot \text{gain} \]

Rate equation describing carrier evolution

\[ \frac{\partial N}{\partial t} = D \nabla^2 N + \frac{I}{qV} - \frac{N}{\tau_c} - \frac{a(N - N_o)}{\hbar \omega} |E|^2, \]

Wave equation describing optical propagation

\[ \nabla^2 E - \frac{\varepsilon}{c^2} \frac{\partial^2 E}{\partial t^2} = 0, \]
\[ \varepsilon = n_o + \chi(N) \]
\[ \chi(N) = -\frac{n c}{\omega_o} (\alpha + i) \cdot a(N - N_o) \]

Volume: \( V \)
Carrier density: \( N \)
Gain/Loss
Background index
Index of refraction

A Phenomenological Model

Key assumptions:

\[ \text{gain} = a(N - N_o) \]
\[ \text{index} = \alpha \cdot \text{gain} \]

Rate equation describing carrier evolution

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Wave equation describing optical propagation

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\]
\[ \varepsilon = n_o + \chi(N) \]
\[ \chi(N) = -\frac{n c}{\omega_o} (\alpha + i) \cdot a(N - N_o) \]

Coupled equations describing gain evolution, optical pulse amplitude and phase propagation

\[
h(\tau) = \int_0^L g(z, \tau)dz
\]
\[
\frac{\partial h(\tau)}{\partial \tau} = \frac{g_o L - h(\tau)}{\tau_c} - \frac{P_{\text{in}}(\tau)}{E_{\text{sat}}}(e^{h(\tau)} - 1)
\]
\[ P_{\text{out}}(\tau) = P_{\text{in}}(\tau)e^{h(\tau)} \]
\[ \Phi_{\text{out}}(\tau) = \Phi_{\text{in}}(\tau) - \frac{1}{2} \alpha h(\tau) \]

V = volume
N = carrier density
h(\tau) = integrated gain

A Phenomenological Model

Key assumptions:

\[ \text{gain} = a(N - N_o) \]
\[ \text{index} = \alpha \cdot \text{gain} \]

Rate equation describing carrier evolution

\[ \frac{\partial N}{\partial t} = D \nabla^2 N + \frac{I}{qV} - \frac{N}{\tau_c} - \frac{a(N - N_o)}{\hbar \omega} |E|^2, \]

Wave equation describing optical propagation

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Wave equation describing optical propagation

\[ h(\tau) = \int_0^L g(z, \tau) dz \]
\[ \frac{\partial h(\tau)}{\partial \tau} = \frac{g_oL - h(\tau)}{\tau_c} - \frac{P_{in}(\tau)}{E_{sat}} (e^{h(\tau)} - 1) \]
\[ P_{out}(\tau) = P_{in}(\tau) e^{h(\tau)} \]
\[ \Phi_{out}(\tau) = \Phi_{in}(\tau) - \frac{1}{2} \alpha h(\tau) \]

- Gain saturates and recovers
- Phase \( \propto \) gain

V = volume
N = carrier density
\( h(\tau) \) = integrated gain

Carrier Recovery Time Limitation

- Long carrier recovery time creates pulse patterning
- Limits switching speed to ~10 Gb/s
- Solution: balanced interferometer approach

- 2-ps pulses, 40 Gb/s
- 5 fJ input pulse energy
- $\tau_c = 80$ ps
- Initial gain: 30 dB
- $L = 1$ mm
- $E_{\text{sat}} = 1$ pJ
- $\alpha = 5$
Balanced Interferometer Design
Balanced Interferometer Design

\[ G_1 E(t) e^{\Phi_1} \]

\[ G_2 E(t) e^{\Phi_2} \]

Signal: \( E(t) \)

\( \Delta T \)

\( \Delta P \)

\( \text{SOA} \)

\( \text{BPF} \)
Balanced Interferometer Design
Balanced Interferometer Design
Balanced Interferometer Design

**Diagram:**
- **Signal Path:**
  - Control
  - Signal $E(t)$
  - Delay $\Delta T$
  - Power $\Delta P$
- **Processing Blocks:**
  - SOA
  - BPF
- **Output Signals:**
  - $G_1 E(t) e^{\Phi_1}$
  - $G_2 E(t) e^{\Phi_2}$

**Notes:**
- Slow carrier recovery cancels

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JPW 6/11/2008

MIT Lincoln Laboratory
Balanced Interferometer Design

\[ G_1 E(t) e^{\Phi_1} \quad \text{"Inverting"} \]

\[ G_2 E(t) e^{\Phi_2} \quad \text{"Non-Inverting"} \]

Slow carrier recovery cancels.
Balanced Interferometer Design

Inverting

Non-inverting
Outline

• Motivation/Background
• Ultrafast all-optical logic gates
• **Routing: 40-Gb/s all-optical header processing**
• Performance optimization of optical logic gates
• Regeneration
• Future SOA-MZI gates
• Conclusion
40-Gb/s All-Optical Header Processing

- **Goal:** Demonstrate ultrafast packet processing functionality for routing

- **Previous work***:
  - Ultrafast all-optical header processing of single packets
  - Applicable to add/drop nodes, ring networks

- **This work**:
  - Multi-packet all-optical header processing demonstration
  - Scalable topology: can be easily extended to larger switches
  - Applicable to wide variety of networks, including multi-degree mesh nodes
  - Increased packet processing functionality

Header Processing Logic

\[ E_k = \text{Empty/Full bit} \]
\[ A_k = \text{Address bit} \]

Header Processing Unit

Switch Matrix

\[ A_1 = 0, E_1 = 1 \]
\[ A_2 = 1, E_2 = 0 \]

0 = (Bar)
1 = (Cross)

\[ A_k = 0 \]
\[ A_k = 1 \]
**Header Processing Logic**

- \( E_k \) = Empty/Full bit
- \( A_k \) = Address bit

**Switch Matrix**

```
A_1=0 E_1=1
A_2=1 E_2=0
0 = (Bar)
1 = (Cross)
```

**Header Processing Unit**

```
A_k = 0
```

**Truth Table**

<table>
<thead>
<tr>
<th>( A_1A_2 )</th>
<th>( E_1E_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>X</td>
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<tr>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>X</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
</tr>
</tbody>
</table>

**Column headings**

- \( A_1A_2 \)
- \( E_1E_2 \)
Header Processing Logic

\[ E_k = \text{Empty/Full bit} \]
\[ A_k = \text{Address bit} \]

\[ E_k = \begin{cases} 0 & \text{Empty} \\ 1 & \text{Full} \end{cases} \]
\[ A_k = \begin{cases} 0 & \text{Address 0} \\ 1 & \text{Address 1} \end{cases} \]

Switch Matrix

Header Processing Unit

\[ R = A_1 \cdot E_1 + \overline{A_2} \cdot E_2 \]

\[ \begin{array}{c|cccc}
   & 00 & 10 & 11 & 01 \\
\hline
00 & X & X & X & X \\
10 & 0 & 1 & 1 & 0 \\
11 & X & 1 & X & 0 \\
01 & 1 & 1 & 0 & 0 \\
\end{array} \]
Header Processing Logic

$E_k = \text{Empty/Full bit}$

$A_k = \text{Address bit}$

$E_1 = $ Empty/Full bit

$A_1 = $ Address bit

$A_1 \cdot E_1$

$A_2 \cdot E_2$

$A_1 = 0, E_1 = 1$

$A_2 = 1, E_2 = 0$

Switch Matrix

$0 = (\text{Bar})$

$1 = (\text{Cross})$

$A_1 \cdot E_1 + \overline{A_2} \cdot E_2$

$R$

$E_1 E_2$

$A_1 A_2$

<table>
<thead>
<tr>
<th></th>
<th>00</th>
<th>10</th>
<th>11</th>
<th>01</th>
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</tr>
</tbody>
</table>

$E_k = \text{Empty/Full bit}$

$A_k = \text{Address bit}$
Header Processing Logic

- Multi-packet processing (2 incoming packets to 2 outgoing ports)
- Scalable: 2 optical logic gates for each 2x2 switch
- Potential for integration (SOA-based logic)

\[ R = A_1 \cdot E_1 + \overline{A_2} \cdot E_2 \]
Optical Logic Gate Implementation: Ultrafast Nonlinear Interferometer (UNI)


BRF = Birefringent Fiber
SOA = Semiconductor Optical Amplifier
BPF = Bandpass Filter
Optical Logic Gate Implementation: Ultrafast Nonlinear Interferometer (UNI)

Full System Experimental Schematic

- Packet Architecture
  - $2^7 - 1$ PRBS

MLFL = Mode-locked Fiber Laser
Tx = Transmitter
Full System Experimental Schematic

- **Packet Architecture**
  - $2^7$-1 PRBS
  - 4000 bits/packet
  - 100 ns packet

MLFL = Mode-locked Fiber Laser
Tx = Transmitter
EOM = Electro-optic modulator
Full System Experimental Schematic

- Packet Architecture
  - $2^7 - 1$ PRBS
  - 4000 bits/packet
  - 100 ns packet
Ultrafast All-Optical Header Processor

- Ultrafast operation: Header error rate of $1 \times 10^{-6}$ with 40-Gbit/s line rate
- Comparable with current electronic router error rates
- Low switching-energy: 60.5 fJ/packet

PER $1.7 \times 10^{-9}$

PER $3 \times 10^{-9}$

\[ R = A_1 \cdot E_1 + \overline{A}_2 \cdot E_2 \]
The Need For Integration

- Successful demonstration of 2-port forwarding using discrete all-optical logic gates.

- What is required to expand this functionality?
  - Integration: Discrete logic gates are infeasible for practical implementation
    - Size, weight, cost
    - Ease of installation & operation
  - Simple method for optimizing each logic gate for optimal performance
    - Currently requires time-intensive search over a large parameter space
Outline

• Motivation/Background
• Ultrafast all-optical logic gates
• Routing: 40-Gb/s all-optical header processing
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• Regeneration
• Future SOA-MZI gates
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SOA Mach-Zehnder Interferometer: An Integrated Optical Logic Gate

- Integrated optical logic gate: SOA-MZI
- Conceptually similar to the UNI: balanced interferometer
- Waveguide and coupling losses require amplifying SOAs
- Complex parameter space makes optimization difficult
SOA Mach-Zehnder Interferometer: An Integrated Optical Logic Gate

• Focus on single-ended operation to observe SOA dynamics
• Key operating parameters
  – $I_4$, $I_5$
  – Signal and control average power
  – Signal and control pulse power
  – Signal-control delay ($\Delta t$)

Developed by Alphion Corporation.
Bias map measurement:
- Sweep $I_4$ current at 1 Hz
  - Measure current on SOA using hall-effect probe
- Measure output power on oscilloscope
- Full 2D scan taken on the order of minutes
Static Interferometer Bias Map

- Bias map measurement:
  - Sweep $I_4$ current at 1 Hz
    - Measure current on SOA using hall-effect probe
  - Measure output power on oscilloscope
  - Full 2D scan taken on the order of minutes
• Bias map measurement:
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  – Sweep \( I_4 \) current at 1 Hz
    • Measure current on SOA using hall-effect probe
  – Measure output power on oscilloscope
  – Full 2D scan taken on the order of minutes
Switching Window Measurement

- Fix current bias ($I_4$, $I_5$)
- Measure average output power at every control-signal delay
Switching Window Measurement

- Fix current bias \( I_4, I_5 \)
- Measure average output power at every control-signal delay
Switching Window Measurement

- Fix current bias ($I_4$, $I_5$)
- Measure average output power at every control-signal delay
Switching Window Measurement

- Fix current bias ($I_4, I_5$)
- Measure average output power at every control-signal delay
Switching Window Measurement

- Fix current bias \( I_4, I_5 \)
- Measure average output power at every control-signal delay
- Continuous measurement can be obtained using a difference-frequency technique

\[ I_4 = 893.5 \text{ mA} \]
\[ I_5 = 470 \text{ mA} \]
Switching Window Measurement

• Fix current bias ($I_4$, $I_5$)
• Measure average output power at every control-signal delay
• Continuous measurement can be obtained using a difference-frequency technique
• Switching dynamics
  • Extinction, Recovery time
Combined Measurement: Dynamic Bias Scan

- Simultaneous pump-probe measurement at all bias points
  - At each signal delay, measure a bias map

MLFL = mode-locked fiber laser
Dynamic Pump-Probe Bias Scan

- Simultaneous pump-probe measurement at all bias points
  - At each signal delay, measure a bias map

- Measures the effect of optical control pulse on interferometer bias at all operating points: 4-dimensional plot

Dynamic Bias Scan

Extinction map: Extract extinction measurement from dynamic bias scan
Inverting mode gives higher extinction, but logic functions often require non-inverting operation
Wavelength Conversion at Selected Operating Point

- Demonstration of effectiveness of dynamic bias map: wavelength conversion
Wavelength Conversion at Selected Operating Point

- Demonstration of effectiveness of dynamic bias map: wavelength conversion
- Compare with nearby operating point found by typical manual optimization
Wavelength Conversion at Selected Operating Point

- Demonstration of effectiveness of dynamic bias map: wavelength conversion
- Compare with nearby operating point found by typical manual optimization

Achievements:
- Highly accurate characterization technique for optimization of ultrafast switch performance
- Improves practical, multi-gate functionality of integrated optical logic
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10,000-km, 100-pass All-Optical Regeneration

• Goal: Demonstrate all-optical error-free regeneration with the SOA-MZI logic gate

• Previous work*:
  – Error-free regeneration with paired SOA-MZI logic gates (inverting operation)

• This work:
  – Wavelength-maintaining regenerator
  – Non-inverting operation (requires only a single logic gate)
  – Polarization insensitive

100-km Recirculating Loop Experiment

- Simulates regenerator performance in real-world system
- Tests SOA-MZI in cascading operation
- Dispersion compensation cancels 2\textsuperscript{nd} order dispersion
- 10 Gb/s, $2^{31}-1$ pseudo-random bit sequence

100-km Recirculating Loop Experiment

- Wavelength converter + SOA-MZI = wavelength-maintaining regenerator
- Single SOA-MZI regenerator, non-inverting operation
- Optimal operating point found via dynamic bias map
- Very stable regenerator operation
Regenerator Results: Cross-Correlation and BER

- Cross-correlation & BER measured after regenerator
- 0.5-dB penalty after 100 passes (10,000 km)

Thus Far...

- Electronic techniques rapidly outgrowing size, weight, power limitations
- Optical signal processing techniques can help:
  - Ultrafast, multi-packet header processing
    - Scalable
    - Low switching energy
    - Network flexibility from payload transparency
    - Reduced O/E/O conversions
  - Practical, easily optimized integrated logic gates
    - Accurate, fast optimization
    - Insight into switching dynamics
  - Cascadable, single-gate wavelength-maintaining regeneration
    - Polarization insensitive
    - Potential for integration
    - 10,000-km, 100 pass demonstration
Outline

• Motivation/Background
• Ultrafast all-optical logic gates
• Routing: 40-Gb/s all-optical header processing
• Performance optimization of optical logic gates
• Regeneration
• Future SOA-MZI gates: What’s next?
Integration Platforms

• Hybrid Integration
  – Incompatible materials integrated on a wafer
  – Passive material: silicon, silica
  – Active material: InGaAsP (III-V semiconductors)
  – Challenge: Alignment and fabrication cost

• Monolithic integration
  – Compatible materials grown together for both active and passive devices
  – Challenge:
    • Silicon: active devices
    • InGaAsP: low loss
  – Challenge: high yields
Integration Platforms

• Hybrid Integration
  – Incompatible materials integrated on a wafer
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• Monolithic integration
  – Compatible materials grown together for both active and passive devices
  – Challenge:
    • Silicon: active devices
    • InGaAsP: low loss
  – Challenge: high yields

• Asymmetric twin waveguide approach

• Potential for close to 100% coupling
• Potential for high yield
• Tolerance for fabrication errors

• Collaboration with MIT Integrated Photonics Devices and Materials group
Multi-gate Integrated Optical Logic

- Previous work:
  - Simulation and design of SOA-MZI gates (A. Markina)
  - Fabrication of 1st and 2nd generation logic chips (R. Williams)

- This work:
  - Characterization of 2nd generation logic chip
  - Recommendations for next generation integrated chips

- Future work:
  - Fabrication and design of 3rd generation chips (T. Shih)
Integration Progress: Size, Power

Characterization results:
- Demonstrated SOA gain, active/passive coupling
- Loss is currently an issue
- Fabrication improvements will solve these issues

Enable complex logic on a single chip
Conclusion

- Demonstrated functionality of all-optical signal processing in routing and regeneration
  - 40 Gb/s multi-packet header-processing
  - 10,000-km, 100-pass error free regeneration
- Addressed practical implementation of all-optical signal processing
  - Developed a simple optimization technique for all-optical logic gate performance
  - Demonstrated potential of asymmetric waveguide design for integrated multi-gate logic on a single chip
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- Aleksandra Markina (graduated)
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- Ali Motamedi
- Reja Amatya

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- Boris Stefanov
- Leo Spiekman
- Hongsheng Wang
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## Rough Power Comparison

<table>
<thead>
<tr>
<th>Electronic 3R Regenerator*</th>
<th>Optical 3R Regenerator</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Total power: 10W</td>
<td>• 1 optical logic gate</td>
</tr>
<tr>
<td>• 2 channels</td>
<td>• 1 channel</td>
</tr>
<tr>
<td>• 2.5 Gb/s per channel</td>
<td>• Bias power: 600 mW</td>
</tr>
<tr>
<td>• 40 Gb/s</td>
<td>- 2 SOAs</td>
</tr>
<tr>
<td>- 8 modules</td>
<td>- 200 mA x 1.5 V = 300 mW per SOA</td>
</tr>
<tr>
<td>- 80 W</td>
<td>• Switching energy: 40 fJ/bit</td>
</tr>
<tr>
<td>• 100 Gb/s</td>
<td>- 40 Gb/s: 1.6 mW</td>
</tr>
<tr>
<td>- 20 modules</td>
<td>- 100 Gb/s: 4 mW</td>
</tr>
<tr>
<td>- 200 W</td>
<td>{ negligible }</td>
</tr>
</tbody>
</table>

But electronic regenerator offers more functionality than just 3R regeneration!

* Cisco WDM Transponder
Power Consumption Shortfall

Technology is falling behind demand

Shortfall is overcome by architectural innovation and trading off:
Performance, functionality, programmability, physical size/density
→ Very hard to sustain long-term

Commercial Electronic Routers

**Cisco CSR-1**
- Throughput: 1.2 Tb/s
- Power: 10.9 kW
- Weight: 1595 lb.

**Juniper T1600**
- Throughput: 1.6 Tb/s
- Power: 9.1 kW
- Weight: 680 lb.

**Power Consumption Allocation by Subsystems**

- Routing Engine: 61%
- CPU: 9%
- SP: 1%
- Fabric: 11%
- Misc.: 3%
- Power Conv: 15%