SYSTEMATIC DESIGN OF A PERMANENT MAGNET SYNCHRONOUS MOTOR DRIVE

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ABSTRACT

PM synchronous motors (PMSMs) operate at a high power factor, efficiency and reliability. To achieve the performance of dc machines, the PMSM drive is vector controlled. Such a drive is described in this paper. The instantaneous position of the rotor is used to determine the required currents which the controller forces into the motor. The actual current is compared to the required or commanded current, and hysteresis or ramp comparison current controllers used to force the actual current to follow the commanded. Detailed circuits are provided with experimental results. Operation in the flux weakening region is also shown.

1.0 INTRODUCTION

Permanent magnet ac motors have the advantage of not requiring any magnetising current in the constant torque region. Hence they can operate at a higher power factor and efficiency than an induction motor in the fractional to 30 kW region. Inverter-fed PM machines do not need slip rings or brushes, hence the reliability of the motor is higher than that of a wound rotor synchronous or induction motor. Similarly, the use of the permanent magnets tends to reduce the weight, when compared to other motors of equivalent power output. This leads to an increased torque to inertia ratio and power density [1]. These characteristics make PM ac motors suitable for robotics and aerospace applications [2].

2.0 VECTOR CONTROL OF A PMSM

Vector control enables ac motors to obtain performance characteristics similar to dc machines, such as tight control of speed and torque. This control technique takes into account the instantaneous rotor position and forces the motor currents to maintain some specified angle with respect to the rotor, by carefully controlling the switching of the inverter. Although once rotating, only the relative rotor position to an original known position is required, to ensure correct starting, the absolute rotor position must be known. A vector controlled PMSM system is illustrated in figure 1.

By controlling only the stator currents, the magnet flux in the airgap and stator can be controlled. Making use of the rotor position, the stator currents can be at any required phase angle with respect to the rotor flux, and hence with respect to the back-emf [3]. For a non-salient motor, the most efficient operation occurs when the stator flux is perpendicular to the rotor flux, that is when it is in phase with the back-emf. On the other hand, inset or buried PM machines produce maximum torque at angles larger than 90^{o}, where the input current is not in phase with the back-emf.

The upper speed limit of the motor is determined when the back-emf equals the supply voltage. If the phase of the stator currents is advanced with respect to the back-emf, there is a component of the stator flux which opposes the rotor flux, thereby causing the effect of flux weakening [4]. This reduces the back-emf, allowing the motor to operate at higher speeds. The arc of the magnet and leakage inductance of the motor play crucial roles in this operating regime. With the current at its rated value, the process of flux weakening reduces the torque producing component

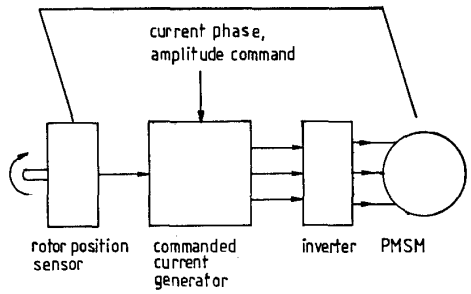

Figure 1. Vector controlled PMSM.

of the flux in phase with the back-emf, and hence the torque.

3.0 CURRENT CONTROL

For a permanent magnet synchronous machine, the back-emf is sinusoidal, and hence for smooth torque generation, the stator currents must also be sinusoidal.

Of the various methods of non-linear current control, the hysteresis method is one of the simplest conceptually. It also has the advantage of a fast transient response compared to other methods such as fixed sampling rate hysteresis and ramp comparison.

3.1 Hysteresis Current Control

The hysteresis controller compares the actual current with the commanded, and if the magnitude of the error is greater than a preset level, the inverter is switched appropriately [5]. Consequently, there is a dead band, known as the hysteresis band. This is shown for a single phase in figure 2.

If the hysteresis current controller operates on each phase individually, then the system in figure 2 applies. Although the actual current in any given phase depends on the instantaneous current in the other two, that is not taken into account in the controller.

A three phase inverter circuit is shown in figure 3. Each line is held at either the positive or negative rail voltage, either by direct switching on of a transistor or by a current path through the diodes.

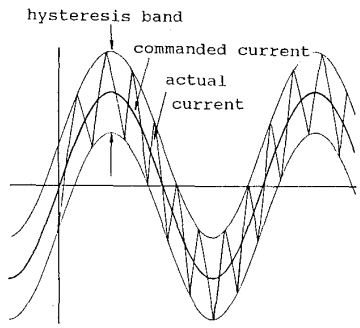

Figure 2. Single phase commanded and actual currents with hysteresis band.

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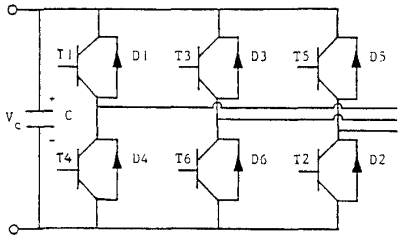

Figure 3. 3 phase inverter circuit.

For given phase, the transistor that requires to be switched is dependent on both the sign of the error and that of the commanded current (I^*). For a hysteresis bandwidth of h, the algorithm used for the inverter leg of T1/T4 and individual current control in each phase is:

if $I^*>0$ and $I>(I^* + h/2)$ then turn off T1

if $I^*>0$ and $I<(I^* - h/2)$ then turn on T1

if $I^*<0$ and $I>(I^* + h/2)$ then turn on T4

if $I^*<0$ and $I<(I^* - h/2)$ then turn off T4

The same applies to the other inverter legs.

A disadvantage of the hysteresis current controller is that the switching frequency is unknown and it depends on the motor parameters, speed and dc bus voltage. The frequency also varies over an electrical cycle.

3.2 Fixed Sampling Rate Hysteresis Current Control

A variation of the hysteresis current control method is to use a fixed sampling frequency of the current. This has the advantage of fixing the inverter switching frequency, but the disadvantage of a poorer transient response and current error when compared to the type discussed in 3.1. At set time intervals, the actual current is compared to the commanded current, and if the current error is larger than the hysteresis bandwidth, the appropriate hysteresis switching strategy occurs, as shown in figure 4. The problem of an uncertain switching frequency in 3.1 is transformed into a problem of uncertain current error in this implementation.

For a zero hysteresis bandwidth, this is known as delta modulation [8]. Note that the current error often increases beyond that of the hysteresis bands, but that the switching frequency is lower than if continuous hysteresis current control were to be used with the same hysteresis bands.

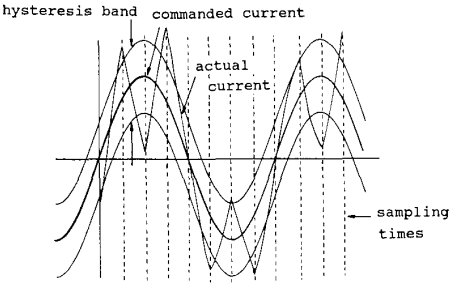

Figure 4. Fixed sampling rate hysteresis current controller.

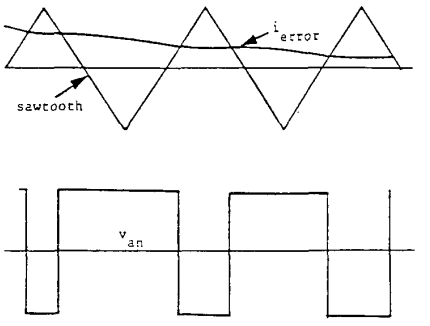

Figure 5. The ramp comparison controller.

3.3 Ramp Comparison Current Control

An alternative to the hysteresis current controller is to use the ramp comparison method [9]. Here the current error is compared to a triangular waveform and when the error crosses the triangle wave, a switching strategy is employed. This is demonstrated in figure 5.

The inverter transistor that is to be turned on or off is dependent on the sign of the commanded current waveform and the magnitude of the current error relative to the triangle wave. It is not necessary to use complementary transistor switching, since the current can decay through the diodes. The switching algorithm is given below.

1) if $I^* > 0$ and $V_{error} > V_{triangle}$ then turn on T1, or else turn T1 off,

2) if $I^* < 0$ and $V_{error} > V_{triangle}$ then turn on T4 or else turn T4 off.

As the error increases, the appropriate transistor remains on longer.

From the rotor position, it is possible to generate the waveform of the required currents in each phase of the motor. These waveforms can then be used to switch an inverter appropriately, to produce an approximation to the ideal current waveforms. To perform the current control, the actual current flowing is required to be measured.

4.0 DESIGN AND IMPLEMENTATION OF THE PMSM VECTOR CONTROLLER

It is possible to implement vector control of a PMSM using either software or hardware. A disadvantage of software is the length of time required for the processing. To achieve fast control, either a particularly fast processor would be required (such as a digital signal processor) or several processors would be required, with the attendant handshaking problems.

In this design a hardware solution is described, although a DSP-based [10] vector controller will be reported in the near future.

The design of the vector controller can be divided into the following sections:

1) determining the rotor position,
2) producing the commanded current waveforms,
3) producing the gating signals to the inverter.

The vector controller chosen is shown in figure 6, with a more detailed discussion of the various circuits commencing in section 5.

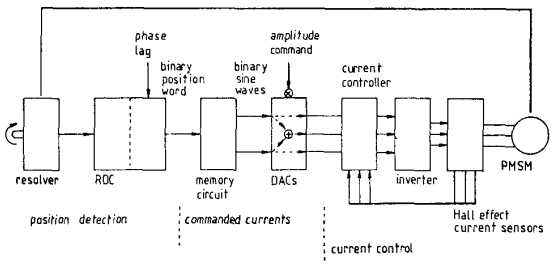

Figure 6. The vector controller implementation.

5.0 POSITION MEASUREMENT

To produce a reliable and low maintenance system, only brushless position measurement has been considered. This reduces the choice to either an optical position encoder or a resolver. The output of an optical encoder using the Gray encoding system is digital, but it is inherently sensitive to misalignment due to mechanical shocks and noise in the transmission of the position to the controller. The resolver has been chosen, since although it uses analogue signals, it is very rugged, being essentially a rotating transformer. It also has the advantage that the output changes continuously, allowing very high resolution if required. Since a resolver has two outputs, common mode noise can be substantially reduced.

5.1 Exciting the Resolver

A resolver consists in its simplest form of a primary winding and two secondary windings, which are placed perpendicularly to each other (known as sine and cosine windings).

By exciting the primary winding with a carrier frequency (in this case 4.5kHz), the secondary windings have an induced carrier waveform with a modulated amplitude, which varies sinusoidally with the rotor position. Since the secondary windings are placed perpendicularly to each other, the modulation amplitudes are 90^{o} out of phase to each other. This enables the position of the rotor to be uniquely determined. The resolver signals are shown in figure 7.

Figure 7 shows the reference, and the sine and cosine output signals from the resolver at a fixed position. The large amplitude signal is the reference signal, and the other two signals are the sine and cosine signals, clearly showing the 90^{o} phase shift in modulation amplitude.

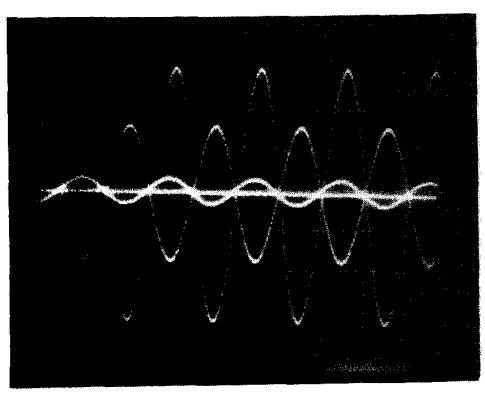

Figure 7. The resolver signals.

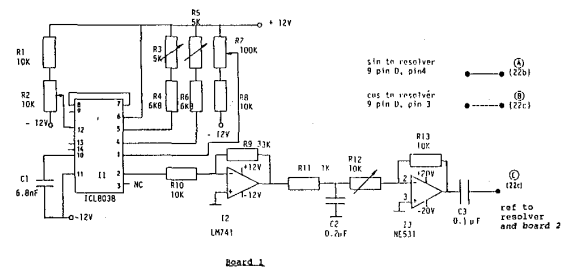

Figure 8. The resolver oscillator.

It was found that the resolver is particularly sensitive to the higher harmonics of the reference signal. At certain rotor positions when either the sine or cosine output had a low amplitude, significant distortion was to be seen on the output waveform. This was largely resolved by the use of a low pass filter. In order to prevent any saturation of the resolver, it was considered important to ensure that the reference signal had no dc component, and hence a series capacitor is used between the reference generator and resolver to block any dc. The low pass filter and series capacitor can be seen as (R11, C2) and C3 respectively, in the circuit diagram of the resolver oscillator in figure 8. As there is no information available on the equivalent circuit of the resolver, the capacitor was chosen experimentally.

The oscillator IC is an ICL 8038, which has three outputs for square, triangular and sinusoidal waveforms, the frequency/mark-space ratio being determined by R3 and R5. The specifications indicate that the sinusoidal waveform distortion is under 1%, however as mentioned earlier, this was found to be excessive. The application notes suggest the addition of R7 and R2 to reduce the distortion. This was partly successful, the solution being to apply the filtering mentioned earlier.

5.2 Resolver Position Detection

The rotor position is crucial in determining the commanded current waveforms. The decoded position is obtainable from a resolver to digital converter (RDC), which has the added benefit of allowing interfacing with computers at a later date if required. The circuit for the RDC board is shown in figure 9.

One of the advantages of using an RDC, such as Analog Devices 2S82KP, is that the number of output bits can be set from 10 to 16, with an accuracy of 4 arcminutes plus 1 lsb. There are also other outputs of use, such as velocity and direction of rotation. Since

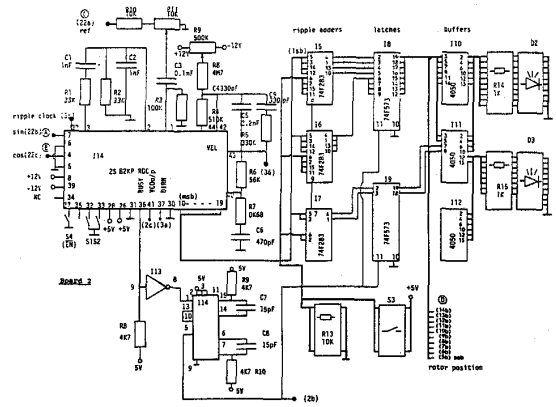

Figure 9. The RDC board.

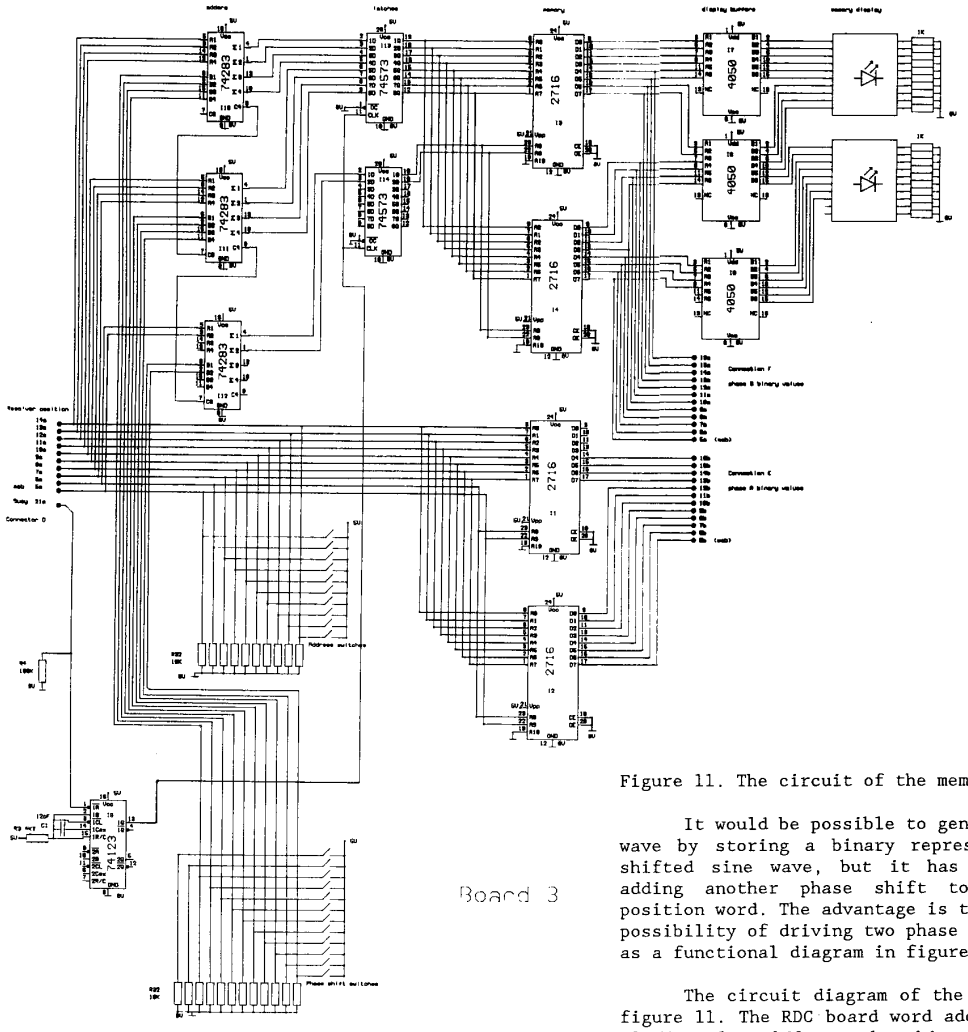

Figure 11. The circuit of the memory board.

the resolver used has eight poles, only the 10 bit position word has been used, giving a resolution of 5.3 arc minutes. Using only 10 bits, enables the the converter to operate at a tracking rate of 1040 rps. The position word is supplied as an input to 3 ripple adders (I5, I6, I7), the other summing input being formed from settable switches or an outer control loop. This represents a phase advance of up to 90^{o}, used for flux weakening operation of the PMSM. The output of the ripple adders is latched by I8 and I9, using a pulse generated 50 ns after the BUSY signal from the RDC is finished. The delay is sufficiently long to take into account the addition time of the adders. The output latches feed into buffers driving LEDs, so that the rotor position can be visually checked and the board tested.

6.0 GENERATION OF THE COMMANDED CURRENT WAVEFORMS

The sine wave commanded current waveforms are generated from the digital position word from the RDC. This has been implemented by using the digital position word (with the added offset for flux weakening) to address memory circuits, which store binary representations of sine waves. Since the system is neutral-less, only two sine waves of 120^{o} phase separation need to be generated, the third one being the inverted sum of the other two.

It would be possible to generate the second sine wave by storing a binary representation of a phase shifted sine wave, but it has been implemented by adding another phase shift to the digital rotor position word. The advantage is that it allows for the possibility of driving two phase motors. This is shown as a functional diagram in figure 10.

The circuit diagram of the memory circuit is in figure 11. The RDC board word addresses EPROMs I1 and I2 directly, while another binary number is added to it by ripple adders and the associated latches, before the word addresses EPROMs I3 and I4. The adders are used to produce a 120^{o} phase shift of one sine wave with respect to the other. The latches are operated by a pulse generated after a delay from the RDC BUSY signal (I6a - I6c).

The EPROMs store the binary representation of a sine wave. Since more than 8 bits resolution are required, they are paired so that one EPROM stores the 8 most significant bits and the other the next 8 most significant bits. An offset and scaled representation

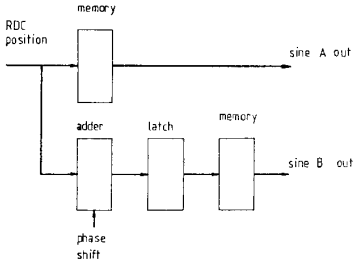

Figure 10. Functional diagram of the memory circuits.

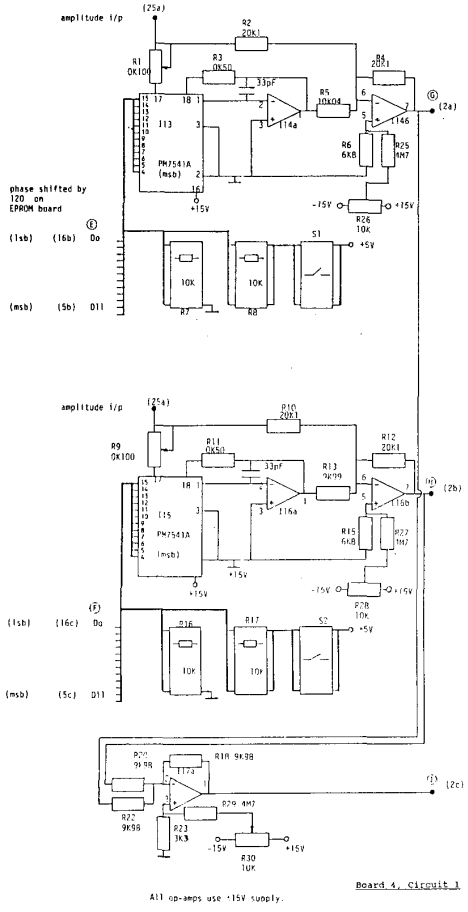

Figure 12. Circuit of the digital to analog converters.

is used, so that all numbers stored are positive or zero. The full range of values is used, ie. the maximum value of the sine wave stored is $(2^{16}-1)$. The output from the digital to analog converters is corrected to account for this. To facilitate testing of the circuit, the output of the EPROM which is addressed via the adders, is displayed on LEDs, and the address lines and one set of adder inputs, is settable by switches, hence allowing testing of both the adders and the EPROMs.

The binary sine wave representations are then fed to two multiplying digital to analog converters, which multiply the sine values from the EPROM with the magnitude of the commanded current vector, to yield the instantaneous commanded phase currents. The output of both converters are added and inverted with analog circuitry to produce the third sine wave.

In figure 12, the circuit for the digital to analogue stage is shown. I13 and I15 are the DACs, both of which are followed by a 2 stage amplifier circuit. Between pins 18 and 1 of the DACs is a 10 K resistor internal to the IC. The current output is from pin 1. The first amplifiers, I14a and I16a, convert this to a voltage output. Then, I14b and I16b subtract the dc component from the amplitude input at pin 17, and scale the output, to produce a sinewave with an average of zero.

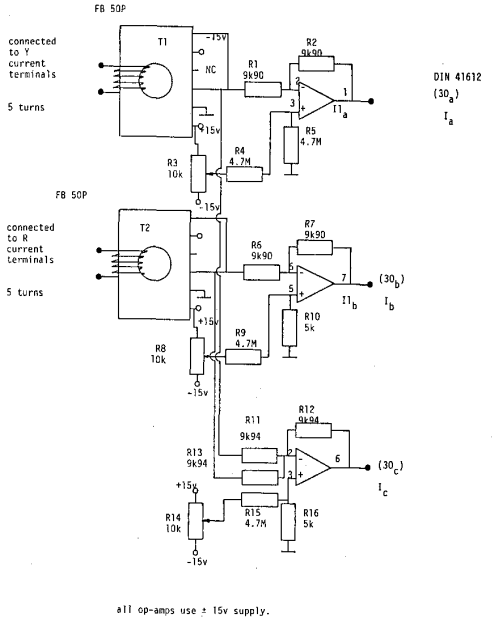

Figure 13. Current measurement circuit.

From the two sine waves reproduced by the DACs, IC 17a sums them and inverts the result, to produce a third sine wave of equal amplitude, and a phase shift of 120° with respect to the sine waves output from the DAC.

7.0 CURRENT CONTROLLER DESIGN AND PERFORMANCE

7.1 Design

The control signals for the inverter, are produced by comparing the commanded current waveforms with the actual current. The actual current is measured using Hall effect devices (T1 and T2) (see figure 13), since they have excellent high frequency response down to dc. The current is then buffered with a simple inverting unity gain amplifier (I1a and I1b).

The sensitivity of each Hall effect device is improved, without the difficulty of equalising the gains on the buffers, by using 5 turns through the sensor. The lack of a neutral means that only two phases need to be directly measured, the third being determined from the negative of the sum of the other two (I2).

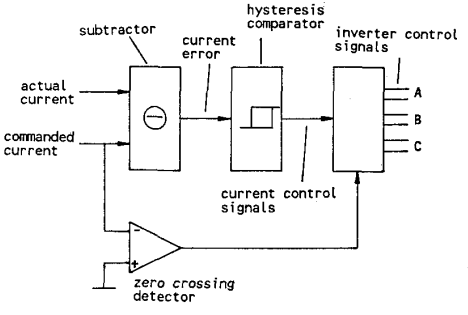

Figure 14. Functional diagram of the hysteresis current controller.

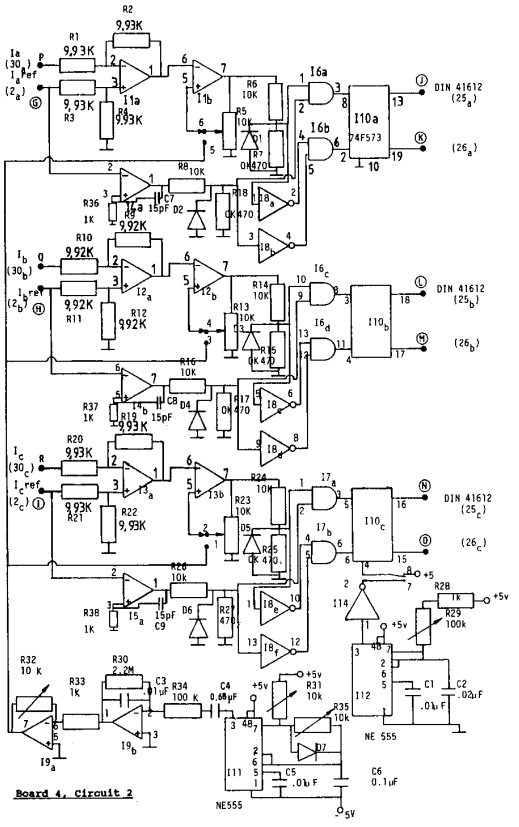

Figure 15. Circuit to produce the inverter control signals.

The basic hysteresis comparator has a hysteresis band around zero, and hence it is the current error that is required to be compared to the hysteresis band. In order to determine which transistor of each phase is to be switched, a simple logic circuit is used, with a signal indicating whether the commanded current waveform is above or below zero, as indicated in figure 14.

The circuit for the inverter control signals is shown in figure 15, where I1a, I2a and I3a perform the unity gain subtraction of (I^* - I_{actual}), to produce the current error signal for each of the 3 phases. In an attempt to reduce the number of different components used, op-amps have been used for comparators.

I1b, I2b and I3b perform the hysteresis comparison and I4a, I4b and I5a produce a signal to indicate whether or not the commanded current signal is greater or less than zero. To do this, op-amp comparators have been used with a little capacitive positive feedback to increase the switching speed. Using the logic discussed earlier, the NOT and the AND gates are used to generate the correct on/off signal for the inverter transistors. The resistor and diode combinations are to change the op-amp outputs into TTL levels, suitable for the logic circuits.

In addition to the hysteresis circuitry, provision has been made for hysteresis current control with a fixed sampling rate as well as ramp comparison current control. The fixed sampling rate is controlled by the latch (I10) and the latch enable signal generated by I12. The ramp comparison method requires

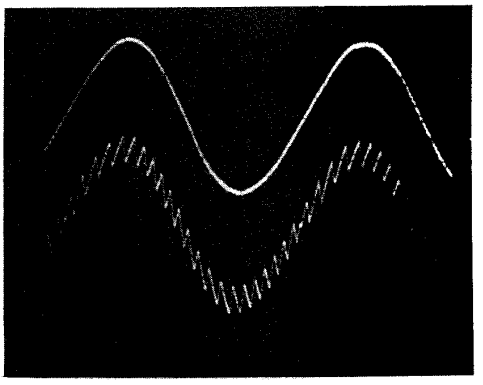

Figure 16. Phase current with hysteresis control.

that the current error signal is compared to a triangular waveform. This merely requires that the hysteresis comparator compares the error signal with the triangular waveform rather than the hysteresis band. This is achieved by a simple switch on pin 5 of ic I1b, I2b and I3b.

The ramp is generated by producing a square wave (I11) and then integrating (I9b). To allow for different frequencies, and hence amplitudes, a variable gain amplifier (I9a) follows on. The diode D7 connected to I11, is included to produce a 50 % duty cycle. Since the square wave tends not be symmetrical about zero, a dc blocking capacitor (C4) is used.

7.2 Current Controller Testing

The current controllers can be tested more easily using a fixed, 3 phase R-L load than using a PMSM, since the back-emf of the PMSM can distort the current waveforms. Therefore, the results presented in this section 7.2 are from an R-L load, and the PMSM results are presented in section 8.

7.21 Hysteresis Current Controller Waveforms

A hysteresis controlled current for a small bandwidth is shown in operation in figure 16. From the current waveforms, it can be seen that the switching frequency is high compared to the fundamental. As the hysteresis band is increased, the switching frequency decreases, as shown in figure 17.

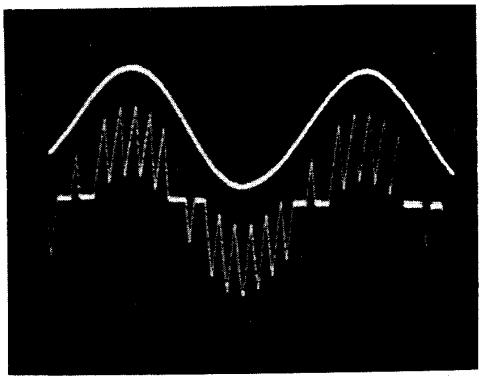

Figure 17. Phase current control with large hysteresis bandwidth.

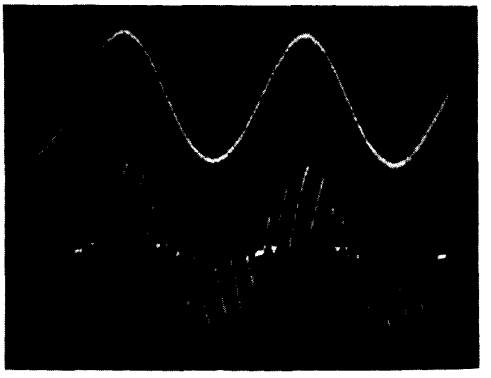

Figure 18. Phase current with fixed sampling rate hysteresis control.

7.22 Fixed Sampling Rate Hysteresis Controlled Current

An example of a fixed sampling rate, hysteresis controlled, current is shown in figure 18. As would be expected, although the hysteresis bandwidth is set to the same size as in figure 16, the effect is to increase the current error, and to reduce the switching frequency.

7.23 Ramp Comparison Controlled Current

An example of a ramp comparison controlled current is shown in figure 19. The switching frequency is clearly limited by the ramp. The triangular waveform is the ramp, on which is superimposed the error waveform. The bottom waveform is the current.

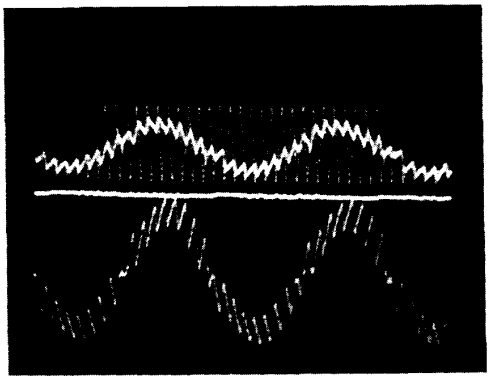

Figure 19. Phase current with ramp comparison control.

8.0 PMSM CURRENT WAVEFORMS

Current waveforms when the PMSM is fed are presented below, in each case with the top waveform being one of the commanded currents.

In figure 20, the interaction between the phases causes an uneven ripple magnitude on the fundamental waveform. With the fixed sampling rate hysteresis controller, the hysteresis band remaining as set for figure 20, the switching frequency falls significantly, as shown in figure 21. The waveform shows that in between inverter leg switchings, the current can fall to zero. This suggests that a higher sampling frequency should be used.

The ramp comparison controller is demonstrated in figure 22 and shows the constancy of the switching frequency. A higher switching frequency will ensure tighter control of the current.

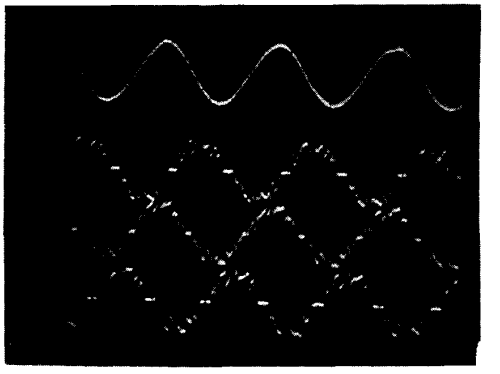

Figure 20. Hysteresis controlled PMSM current waveforms, with a commanded current waveform.

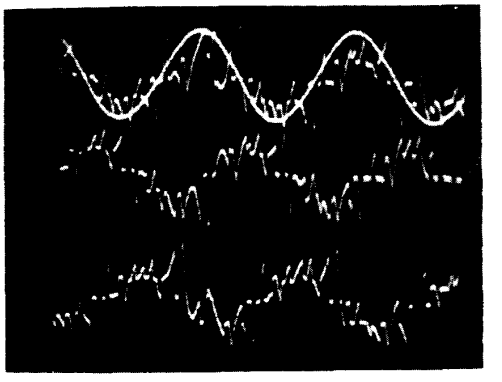

Figure 21. Fixed sampling frequency hysteresis controlled PMSM currents.

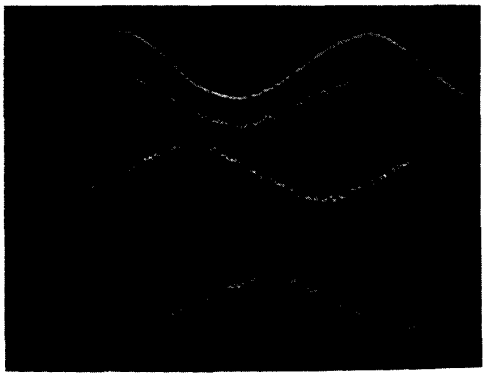

Figure 22. Ramp comparison controlled PMSM currents.

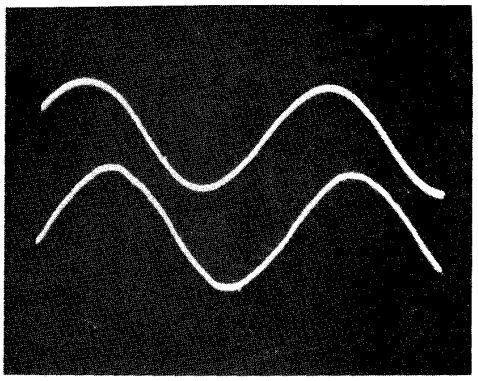

Figure 23. The commanded current leading the back-emf for flux weakening operation of the PMSM.

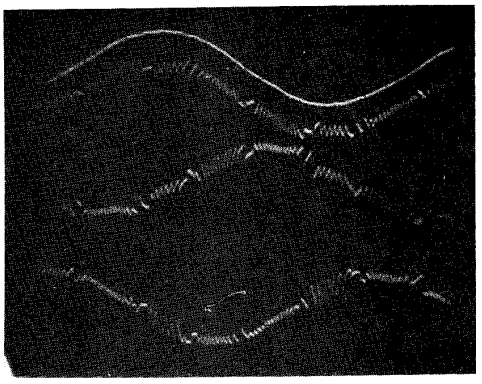

Figure 24. Hysteresis controlled currents in the PMSM during flux weakening operation.

For flux weakening operation of the PMSM, the commmanded current should be advanced with respect to the PMSM back-emf. Figure 23 shows this for the PMSM. Phase advanced currents to allow flux weakening of the PMSM are shown in figure 24.

9.0 CONCLUSION

The design of a versatile PMSM vector drive has been presented, including the current controllers and position measurement. The system is capable of implementing hysteresis, fixed sampling rate hysteresis and ramp comparison current control methods. Examples of currents controlled in these ways are given and the waveforms to be found at various stages of the circuit are provided.

To illustrate the current control methods, examples of the current waveforms are given for a fixed R-L load, and when driving the PMSM, both in the constant torque and flux weakening modes of operation.

Detailed circuit diagrams are provided to allow the reconstruction of this drive system. This drive can be used for the detailed examination of the performance of current controllers, both in the constant torque and flux weakening region, which will be the subject of future contributions in this area.

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