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Thermal Management and Control in Testing Packaged Integrated Circuit (IC) Devices

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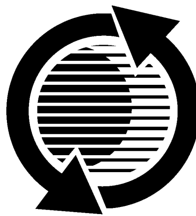

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ABSTRACT

This paper describes the thermal management and design challenges of testing packaged integrated circuit (IC) devices, specifically device thermal conditioning and device-under-test (DUT) temperature control. The approach taken is to discuss the individual thermal design issues as defined by the device type (e.g. memory, microcontroller) and tester capabilities. The influence of performance-parameter specifications, such as the DUT parallelism, test time, index time, test-temperature range and test-temperature tolerance are examined. An understanding of these performance requirements and design constraints enables consideration of existing test handler thermal processing systems (e.g., gravity feed, pick and place), future test handler thermal concepts, and future high-parallelism testing needs for high-wattage memory and microprocessor devices. New thermal designs in several of these areas are described.

INTRODUCTION

Conventional integrated circuit (IC) manufacturing requires each IC device be electrically tested at elevated and depressed temperatures (typically –60 degC to 160 degC) before shipment in order to properly classify the device performance (e.g. its clock speed). This final testing also determines general characteristics, such as whether a device is defective or meets minimal functional performance specifications.

Large production volumes, and therefore low manufacturing costs, are generally necessary to manufacture ICs economically and profitably. Final testing in the manufacture of an IC device is accomplished with automatic test equipment like that shown in Figure 1.

The test system in Figure 1 is typical in that the electrical tester includes a mainframe and test head connected by a very large cable bundle, providing the flexibility needed to mate with different handlers. The test handler automates the mechanical handling and presentation of the devices to the tester. The handler also includes the thermal system that thermally conditions the devices by bringing them to the particular test temperature and which then controls their temperature while under test.

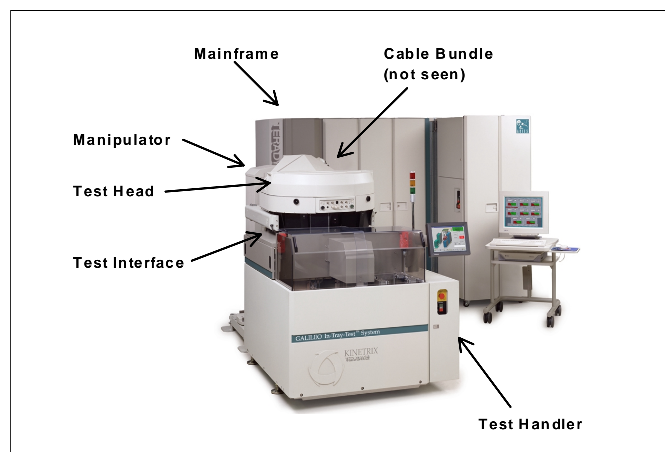

Figure 1. Test cell depicting a tester and handler.

Achieving a low manufacturing cost with test equipment requires that the complete system perform quickly and accurately. These basic requirements imply a system that is not delayed by the time to ramp a device to its test temperature, and one that can control the device-under-test (DUT) temperature to the specified tolerance while it is under test and dissipating electrical power. Test temperature tolerances can be less than ± 2 degC, and as many as 64 devices may be tested simultaneously.

The following sections describe the main thermal management and control challenges in designing and engineering the automated test handler thermal system. A final section focuses on practical considerations and hardware choices relating to the thermal system design.

THERMAL MANAGEMENT ISSUES

In the case of a test handler, the following five principal parameters influence the thermal-system design:

- Handler Type;
- Device Package and Carrier;
- Temperature Capability;
- Temperature Slew Time;
- Device-Under-Test (DUT) Count; and
- Throughput.

Many other issues and factors also play a role. Standards, regulations and certification procedures must be followed. Ergonomic factors must be considered, and also factory-related constraints. The factory floor space, environmental conditions (e.g. ambient temperature and humidity), and available utilities (e.g. voltage and current limitations, compressed air pressure and flow rate limitations) can restrict design choices or attainable thermal performance levels. Tradeoffs and ranking of specifications inevitably guide the final thermal design choices.

HANDLER TYPE – The two traditional types of handlers are gravity feed and pick-and-place handlers, which must be designed mainly for the challenges of DUT temperature control. New test-in-tray handlers, however, must also contend with the need to rapidly thermally condition devices and their carriers. Performance evaluations and descriptions of some commercial handlers can be found in the literature [1, 2]. In the following, though, the thermal systems for each of the three basic types of handlers are described.

Gravity-Feed Handlers – The earliest test-handler designs were gravity-feed types, which are handlers that accept devices from plastic shipping tubes. The tubes are typically loaded at the top of the machine and tilted down, so that the devices slide out of the tube and into the machine. To test the devices at a particular temperature, a series of mechanisms and slide tracks guide the devices into a thermal-conditioning chamber. From this "soak chamber", the devices are sent into a test chamber where they are positioned, aligned and placed against electrical test contactors. After the electrical testing is completed, the devices continue to a sorting section and are categorized according to the test results. The basic flow chart of this type of test handler is shown in Figure 2.

By moving individual IC devices through the machine with tracks, chutes or slides, this type of handler does not need a device carrier within the machine. Gravity-feed handlers can, therefore, pack more devices into a thermal soak chamber [23]. Also, the net thermal load from thermally conditioning the devices is lower, because the devices are not transported in a carrier as they pass through the machine and because the chambers are smaller. The thermal conditioning rates of devices are also often shortened by the additional conduction heat transfer from the thermal-conditioning chamber guide tracks.

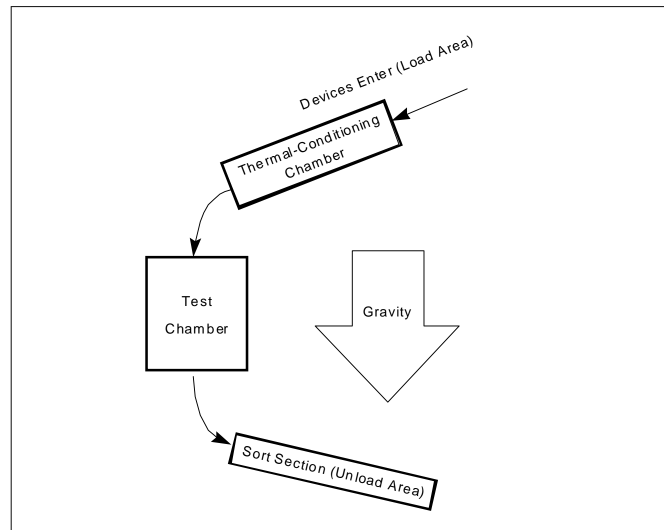

Figure 2. Diagram of the device flow through a typical gravity feed handler.

Pick-and-Place Handlers – The pick-and-place handler offers a means to handle the more fragile devices dominating the semiconductor industry today. These handlers have a loading area for carrier trays that hold the devices. Small vacuum cups mounted to a gantry system provide a means to pick up individual devices and place them on to a special test tray, known as a "boat". This test tray then moves through the thermal-conditioning chamber and into the test chamber, where it is pushed with the devices against the electrical-test contactors. Leaving the test chamber, the trays and devices are returned to a temperature close to ambient, and then enter a sorting section. Here, another pick-and-place robot system sorts the devices back into the shipping or process trays categorized according to the test results. An example of the flow process in a pick-and-place handler is given in Figure 3.

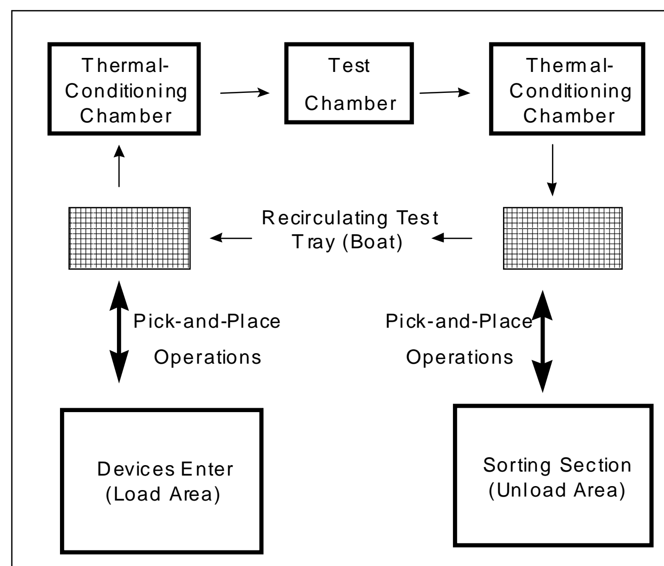

Figure 3. Diagram of the device flow through a typical pick-and-place handler.

The thermal conditioning systems in pick-and-place handlers must accommodate not only the devices but also the special carriers in which they circulate through the handler. This generally increases their size and reduces the thermal-conditioning performance of the handler thermal systems. Pick-and-place thermal systems are designed similar to gravity types; both use convection as the primary means for temperature control and heat transfer to the devices. A supply of liquid nitrogen and clean-dry compressed air often provides the means to cool the airflow for operation at the lower test temperatures below ambient. Mechanical refrigeration is another technique for cooling the airflow.

Test-In-Tray Handlers – A new approach taken by handler manufacturers is to separate the sorting system from the main handler. In addition, the special test trays common to pick-and-place handlers are redesigned as low-cost generic process trays. The general flow of trays in this "test-in-tray" type handler is similar to that of a pick-and-place handler. The trays of devices are placed in a load area, from which they are indexed into a thermal-conditioning chamber before entering the test chamber. The entire tray with the devices is then placed against the electrical test contactors. After testing the devices, the tray moves into a second thermal-conditioning chamber, where the devices are returned to a thermal state close to ambient. An "off-line" sorter (an entirely separate machine) sorts the devices into trays categorized according to the test results. A flow diagram of a test-in-tray handler is shown in Figure 4.

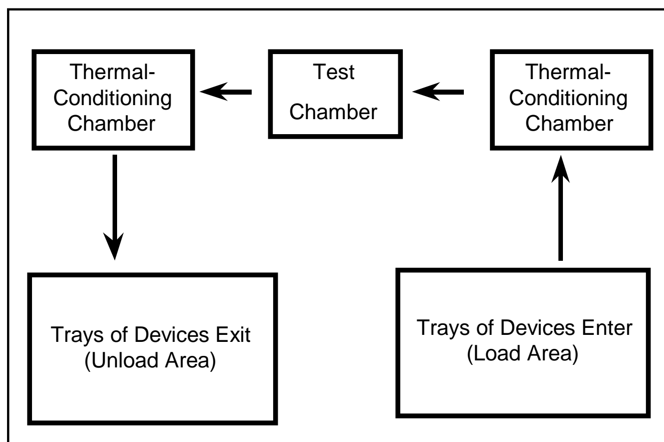

Figure 4. Diagram of the device flow through a typical test-in-tray handler.

The lack of pick-and-place operations, normally used to move the devices in and out of trays, can provide very high throughputs. A more complete discussion of throughput issues is given below. If the throughput advantage of this type of system is leveraged, for example for short test time (< 10 sec) and high DUT parallelism (> 8 or 16 sites) testing, the thermal system must thermally condition devices at a rate many times faster than in traditional handlers. The main driving factors in engineering the thermal system are, therefore, to decrease the thermal conditioning time of devices and optimize the thermal-conditioning chamber capacity and size.

DEVICE PACKAGE AND CARRIER – Test-handler thermal systems are governed by the type of device being tested and its carrier, because each device and each device-carrier combination has a unique thermal behavior. The thermal-conditioning chambers must heat or cool the device and its carrier at a particular rate to a specified temperature. The device and carriers therefore define the required heating and cooling capacity, and the required chamber buffer or storage capacity. Calculations for estimating transient response times of devices subject to different boundary conditions require an engineering model of the system. Under test, the junction temperature and package temperature control varies according to the thermal properties of the package. In each case, material properties are useful for engineering analyses and design calculations.

Device Package – The two most common device package types are "plastic-packaged" or "ceramic-packaged". The focus here is on the materials used for plastic packages. The body of the package encapsulates all the components of an IC device, particularly the chip (or die), providing an easier means to handle the chip and a protection against infiltration of detrimental environmental factors, such as moisture (hermeticity). The package-body material also plays an important role defining the thermal properties of the devices together with the general construction of a device and all its components, for example the lead frame, solder balls, or die.

Body or Encapsulant – The values of the key thermal properties are scattered and can vary greatly, depending on the exact molding-compound composition. Generally, the thermal conductivity is between 0.6 W/mK and 2.5 W/mK [13, 25, 8, 17], the density between 1790 kg/m^3 and 2070 kg/m^3 [13, 17], and the specific heat between 1200 J/kgK and 1170 J/kgK [17].

Lead Frame – The second main component of common IC devices is the lead frame, which provides the external connection points to send electrical signals to the chip embedded inside the device body. The shapes of the external leads vary according to whether the device is a "through-hole" or "surface-mount" type. Ball-grid array (BGA) type devices have solder balls in place of external leads.

Lead frames are made of different materials. The basic types of metallic lead frames are composed of Alloy-42 (42% Nickel, balance Fe) or a copper alloy for the higher thermal conductivity applications, such as Kovar, which is an Fe-Ni-Co alloy [25]. For pin-grid array (PGA) devices, the pins are sometimes made of a phosphor bronze [25]. Intel [13] provides thermal conductivity and density data for copper alloy MF 202 (160 W/mK and 8880 kg/m^3), Alloy 42 (15.7 W/mK and 8100 kg/m^3), and Kovar (17.5 W/mK and 8400 kg/m^3). Edwards et al. [8] list a similar

value for Alloy 42: 16.4 W/mK. Miyake et al. [17] provide more comprehensive data for Alloy 42 and a copper-based lead frame material. For Alloy 42, they list a thermal conductivity of 15 W/mK, a specific heat of 447 J/kgK, and a density of 8200 kg/m^3. For the copper-based lead frame material, the thermal conductivity is listed at 190 W/mK, the specific heat at 383 J/kgK, and the density at 8900 kg/m^3.

The thermal properties of the solder balls of BGA-type devices depend on the specific solder type, or blend of tin and lead. The density is around 8520 kg/m^3, the thermal conductivity around 50 W/mK, and the specific heat around 150 J/kgK [14].

Chip or Die – The third major component of the device is the chip or die. Material properties of the chip reflect the silicon content. For example, Miyake et al. [17] notes that the chip is considered silicon having a thermal conductivity of 150 W/mK, a specific heat of 699 J/kgK, and a density of 2330 kg/m^3. The thermal conductivity is in good agreement with that listed by Edwards et al. [8].

Device Carrier – Gravity-feed handlers are unique in that they do not require any separate internally-recirculating device carriers. Devices are transferred from shipping tubes and onto tracks, which further guide the devices through the rest of the machine. The thermal-conditioning chamber is constructed merely with lengths of track, relying on convection from the surrounding air and conduction from the tracks to thermally-condition the devices.

Pick-and-place handlers use special carriers to handle and transport the devices inside the machine. In these cases, devices are loaded into the handler in tray-type carriers such as common JEDEC-standard shipping trays. A pick-and-place robot then transfers the devices into internally-recirculating trays, also often called "boats". These trays have special mechanical features that align the devices so they properly engage with the electrical test contactors. The geometry and thermal mass of the boats impact thermal-conditioning rates.

The test-in-tray handler uses a test tray that is removed from the handler for sorting and other manufacturing operations. The construction resembles a JEDEC-standard shipping tray to facilitate easier transportation within the factory and integration with other manufacturing equipment.

Thermal Behavior – The material properties and construction information of the devices and their carriers are important in modeling the device-carrier thermal response and DUT temperature control.

No literature describes in detail the modeling of device or device carrier thermal responses for gravity or pick-and-place handlers. A prior paper by the authors [20] describes modeling, analyses, and testing of one type of test-in-tray device carrier that uses heat-transfer enhancing ribs.

Interestingly, the thermal modeling of powered IC devices is still the focus of industry and academic work [10]. Although figures of merits, like junction to ambient thermal resistances have been well described, they do not provide a means to accurately model the temperature field of powered devices in many applications, such as when mounted on computer motherboards or when pressed against contactors in test handlers. Detailed numerical simulations are still the main modeling tool and experimental testing for model verification, especially of the boundary conditions.

TEMPERATURE CAPABILITY – Handlers are generally classified according to their device thermal-conditioning capability: cold, ambient and hot, with those capable of doing all three called tri-temp handlers. Regardless of the package being tested, the test-temperature specification influences the design of both the thermal-conditioning systems and the test chamber thermal system. In the design of the thermal-conditioning chambers, an increase or decrease in the test temperature from ambient increases the thermal-conditioning time, and the required heating and cooling capacities. A more extreme test temperature further increases the time to change the machine from testing at one temperature to another (the temperature "slew time"). Finally, the required insulation thickness of the thermal chambers varies directly with the test temperature, so as to maintain a safe touch temperature on the outside during hot-temperature testing, and also to maintain a non-condensing temperature on the outside during cold-temperature testing. Similarly, the likelihood of condensation or moisture buildup on shafts protruding through a thermal chamber increases as test temperature becomes further below ambient.

The test temperature is specified by the end user (i.e. the chip manufacturer), and it varies greatly from product to product and among the different chip manufacturers. For a given product, the test temperature can further vary, depending on the type of testing being done for example:

- Engineering tests;
- New-product tests;
- Quality-control tests; and
- Production-run tests.

Production-run test temperatures generally depend on the end use of the particular product, be it industrial/commercial, automotive or military. One source [2] states that the automotive components generally need testing down to -55 degC and up to 135 degC. It further states that industrial-rated components are tested generally in the range of 0 degC to 80 degC. High-reliability Military parts need testing up to 125 degC [6]. A recent article by Solberg [24] provides a table documenting typical operating temperatures of devices according to their use. This information is exactly reproduced here in Table 1.

Table 1. Listing of operating temperatures of IC devices according to the category of their use [24].

Category	Temperature Range
Consumer	0 to 60 °C
Computer	15 to 60 °C
Telecom	-40 to 85 °C
Commercial Aircraft	-55 to 95 °C
Industrial/Automotive	-55 to 125 °C
Military Ground/Ship	-55 to 95 °C
Space	-40 to 85 °C
Military Avionics	-55 to 95 °C
Automotive Under the Hood	-65 to 150 °C

Directly related to the test temperature is its tolerance range, which further impacts the thermal-system design. The thermal conditioning chamber that brings the devices to the test temperature (e.g. “soak” chamber) must hold the devices within ±2 degC to ±3 degC of the test temperature. While at the test site, the device temperatures must be maintained to ±1 degC to ±3 degC of the test temperature, depending on the manufacturer and application. This task becomes quite difficult for high parallelism test systems relying on simple temperature control designs, such as single or dual control zones.

Finally, the handler test-site temperature control specification has traditionally reflected the temperature control accuracy of unpowered devices. With device power ratings and power densities increasing among microprocessor and even memory devices, further temperature-control requirements are being established for when devices are powered. Such specifications may include a maximum allowable junction or case temperature rise for a given power-dissipation level.

TEMPERATURE SLEW TIME – The temperature slew time effectively translates to the soak time of the handler. It defines the amount of time the thermal systems must be operating, after changing to a new test temperature, before device processing and testing can begin. The soak duration is on the order of tens of minutes, ranging more specifically from 20 minutes to 60 minutes. The time increases with increasing test temperature.

Estimating this temperature slew time in the design phase of a handler is difficult, because the final value is a function of the interaction and overall construction of the handler and its thermal chambers. A rough measure can be attained by considering the individual thermal chambers separately. The thermal mass and material properties of each thermal system and its associated net heating/cooling capacity are used in the analyses.

Design specifications for temperature slew times exist to minimize the handler idle times - the time during which a handler is not processing devices and which, therefore, negatively impacts the cost-of-ownership of the test equipment. Because most handlers have such a large temperature slew time (minutes are large compared to typical test times which are seconds), they are often set up on the production floor to do either hot or cold testing for as long as possible. The slew time also affects the time to return to a test-ready state after clearing a mechanical jam. If a malfunction occurs inside any of the main thermal chambers, the system must be returned to a safe operating temperature, the jam cleared, and the system returned back to the test temperature. These system jams at temperature have a significant detrimental impact on the throughput productivity (or utilization) of a test handler. Clearing a jam at cold temperature operation most often leads to moist-air ingress, contaminating the inside with light frost and thereby necessitating a time-consuming defrost cycle.

DEVICE-UNDER-TEST (DUT) COUNT – The number of devices that can be tested simultaneously (i.e. DUT parallelism or DUT count) is increasing far beyond the early days of single-site testing; simultaneously achieving tight test-temperature tolerances becomes much more difficult. As the footprint of the test-site area generally increases with the number of devices under test (DUTs), the heat transfer with the test head and the chances for temperature non-uniformity increase too.

The main factor determining the DUT count is the device type (memory, microcontroller (MCU), etc.) and the tester capabilities. Generally, the largest parallel testing possible is 32 devices at once for typical memory devices, and also for the very small (quad flat packaged (QFP)), MCUs. Now, 64 DUT testing is being introduced. The layout or matrix of the DUTs is mostly influenced by the available electrical-test contactor technology and the available mounting space on the handler-interface board (HIB). DUTs can be tested in different arrays, for example 2 x 16 or 4 x 8.

THROUGHPUT – The primary performance measure of a semiconductor manufacturing machine is its throughput, which indicates how much product it can process per unit of time when operating in a steady-state production condition. The basic machine throughput is calculated in a number of ways, depending on the performance and construction of the mechanical systems of the handler. However, this maximum performance of the machine can be compromised during testing at temperature if, for instance, the machine does not have sufficient buffer or queuing capacity to thermally condition the devices before they are tested. The size of this buffer capacity increases as the throughput requirement increases for a given thermal processing time. Also, as devices flow through the machine, they require greater heat input or cooling capacity.

During very short test times (under 10 seconds), gravity-feed and pick-and-place test handlers are often limited in the rate at which the devices can be processed through

the machine, and by the time necessary to sort the devices. During very long test times (over 30 seconds), the on-board sorting system in these handlers sits idle for most of the test time, because it finishes sorting early on. A test-in-tray system with off-line sorting system is limited though by the tray indexing times, the tray load and unload times, or the soak and desoak times, depending on the particular design.

Throughput at Ambient Temperature – A good summary of the calculation methods for ambient handler throughput for parallel IC handlers is given in [12]. Conventional gravity-feed and pick-and-place handlers load components into a track or tray that is used to test the devices yielding a load time, τ_{load}. Once ready for test, the devices must be placed against the test contactors and afterwards removed so the next set can be placed against the contactors. The time for the placement and removal operation is the index time, τ_{index}. The tested devices are then sorted according to the test results in an amount of time called the sort time, τ_{sort}. The time to test the device is the test time, τ_{test}. In the first scenario, if the test time is long as in most memory-device applications, τ_{sort} and τ_{load} have little to no influence on the throughput at ambient temperature:

$$UPH_{amb} = \frac{N_{dut}}{\tau_{index} + \tau_{test}} \frac{3600\text{s}}{\text{hr}}, \tag{2}$$

where the N_{dut} is the number of devices being tested. When the sorting or loading process take longer than the index and test time combined, the throughput becomes

$$UPH_{amb} = \frac{N_{dut}}{\tau_{sort} \text{ or } \tau_{load}} \frac{3600\text{s}}{\text{hr}}. \tag{3}$$

It is apparent from either of these equations that the throughput in any case is directly influenced by the number of devices being tested. The throughput limitations can change in temperature tests.

Throughput at High or Low Temperatures – During a temperature test, the handler thermal system can further reduce the effective throughput. The thermal system that primarily dictates the throughput at temperature under normal operating conditions is the "soak" thermal-conditioning chamber. The throughput at temperature is limited mainly by three factors for tray-based soak chambers:

- the soak time, τ_{soak},
- the number of devices per tray, N_{dpt}, and
- the number of buffered trays, N_{tis}.

The soak time is a characteristic of the heat transfer system and defines the amount of time it takes to warm a tray of devices. The number of devices per tray is important, since a whole tray of devices is warmed collectively. Finally, the number of buffered trays defines how many trays can fit into the soak chamber for thermal conditioning. The relationship among these factors to calculate the throughput is given by Equation (4):

$$UPH_{temp} = \frac{N_{dpt} N_{tis}}{\tau_{tray}} \frac{3600\text{s}}{\text{hr}}. \tag{4}$$

From Equation (4) the maximum throughput at temperature is determined. The tray capacity is determined by the tray design, layout and device type. Therefore, for a given device type and tray capacity, the thermal-throughput equation clearly shows the means to increase the thermal-throughput limit is by increasing the soak capacity or reducing the thermal-response time of the tray of devices. The soak capacity is strongly influenced by the design restrictions on the handler size, which stresses the importance of developing a compact soak chamber so the number of buffered trays can be maximized. The thermal-response time of devices is impacted greatly by the airflow conditions (turbulent or laminar) and device carriers.

To illustrate the differing thermal conditioning requirements among handler types, consider a 32-site handler with an index time of 2 seconds. The gravity-feed or pick-and-place handler we will argue has a sort time of 64 seconds, a soak chamber capacity of 400 devices, and a thermal-response time of 300 seconds for a group of 32 devices. The thermal throughput limit then becomes approximately 5000 uph (units or devices per hour) as shown in Figure 5.

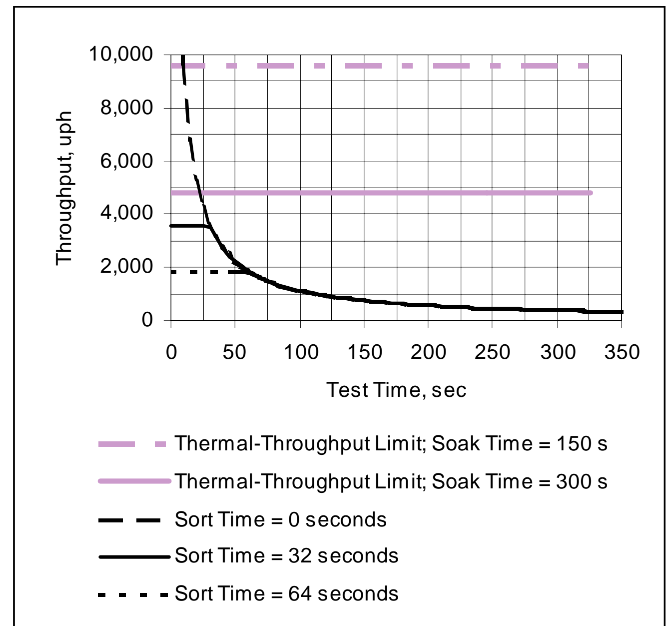

Figure 5. Throughput performance curves for a 32 site handler.

It is also clear that the mechanical throughput limit is below the approximately 5000 uph thermal throughput limit. In this particular instance, the soak chamber and thermal-response time are sufficiently large, even if the

mechanically limiting sort time is cut in half to 32 seconds. This is very typical of pick-and-place or gravity-feed handlers.

As the sort time decreases, the throughput performance steadily increases and becomes more only a function of the test time. For test-in-tray handlers, whose sort time is zero, the throughput will likely be limited by the soak time. As seen in Figure 6, this is true even if the soak time can be reduced to 150 seconds, because these types of handlers have a mechanical throughput limit defined by the index time generally over 10,000 uph. Of course, if the test time is relatively long, the throughput-limiting soak time becomes longer too.

THERMAL CONTROL TASKS

THERMAL CONDITIONING – Heating or cooling devices to the test temperature can be accomplished in a number of ways, including forced air convection or conduction with a temperature-controlled plate. However, design challenges arise in providing a means to continuously feed devices through the handler and in providing flexibility in the face of ever-changing device packages. Conventional systems rely mainly on air convection systems for specific reasons:

- Versatility;
- Known Technology; and
- Cost Effectiveness.

An airflow based thermal system can be designed to heat or cool a host of device and carrier types without requiring any hardware changes or reconfigurations. The flow design is based heavily on traditional HVAC (heating, ventilation, and air conditioning) principles, and most hardware components are commercially available: blowers, heaters, temperature sensors, thermostats and LN_2 valves just to name a few.

Airflow based thermal systems have specific drawbacks in temperature uniformity and control, and thermal capacity. The large and awkward thermal chamber designs, and low heat capacity of air make airflow systems prone to temperature gradients. Consequently, achieving the temperature tolerance requirements can be difficult. Systems must often be “tweaked” by adjusting duct-discharge vanes to redirect portions of the airflow to counter the widely varying thermal loads in the chambers. The low heat capacity of air also not only limits the thermally-conditioning rates of devices and carriers, but also of the entire machine. A handler must itself be “soaked” before it can begin testing or processing devices. Power consumption limitations further exacerbate this problem. Finally, thermal-conditioning chamber buffering of queued trays can lead to very large chambers, particularly for very high throughput handlers. Limitations on handler footprints exist and help chip manufacturers pack more test-cells (combined handler/tester systems) into a factory. This is important, because in factories with hundreds of handlers, small increases in footprint quickly translate to larger overall floor requirements. Each test cell must also have surrounding access areas for service personnel and test-head manipulators.

Temperature control is typically done by controlling the airflow to a fixed temperature or setpoint. A temperature calibration can provide the steady-state relationship of the device temperature to the probe or sensor temperature. Although the resulting thermal response of the device is an exponential climb to the final temperature, this control method ensures that the final temperature of the device is always known, by virtue of the calibration. An example of a test-in-tray soak chamber is shown in Figure 6, where a recirculating airflow thermally conditions trays of devices that enter the chamber.

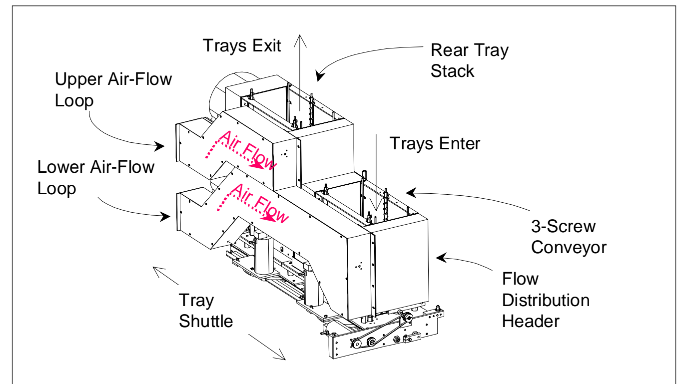

Figure 6. Ductwork and soak chambers of a Kinetrix, Inc. test-in-tray handler showing airflow paths.

The airflow temperature sensor is housed in the flow distribution header (Figure 6) and is used to maintain a fixed airflow temperature. The trays enter the chamber and are continuously exposed to the fixed airflow temperature. An example of the resulting exponential-type response is shown in Figure 7, which is from a Kinetrix, Inc. test-in-tray handler.

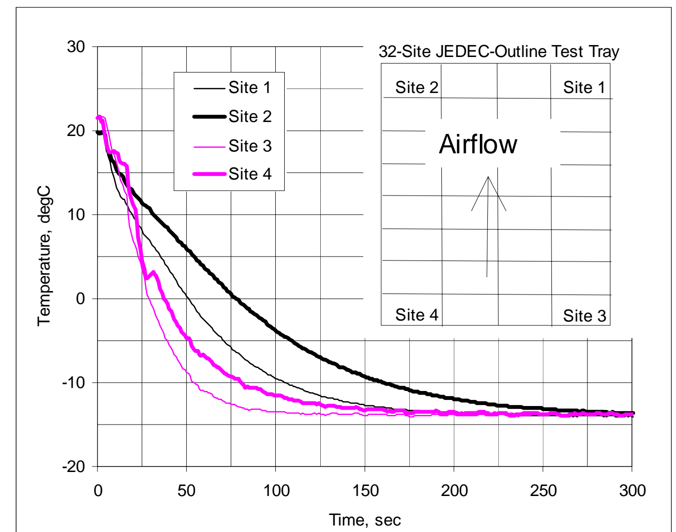

Figure 7. Thermal response of test tray with devices.

The temperature responses of the devices in the test tray (Figure 8a and 8b) clearly show a tendency for the downstream devices to respond slower than the upstream devices, and a tendency for the devices on the right to respond slower than the left side. The downstream devices respond slower because the airflow temperature downstream is heated by the initially warm trays of devices. As the trays of devices cool, the thermal load imposed by the devices reduces too, and hence the temperature gradient across the tray diminishes over time. The time-temperature response of the tray of devices can be accurately modeled [20]. The side-to-side variation is due to the relatively-low pressure drop of the tray stack. As the airflow turns the corner from the duct work into the flow distribution header (Figure 6), the relatively high dynamic pressure of the airflow causes the air velocity to increase at the outside of the turn (the right side of the tray). Screens and other pressure inducing components can be used to better distribute the flow at the exit of the flow-distribution header.

DUT TEMPERATURE CONTROL – Once a device has been brought to temperature it must be temperature controlled under test. Handler temperature uniformity control and powered DUT temperature control define the system's thermal performance. Most designs still rely on temperature-controlled airflows to temperature control the DUTs. But merely pressing a group of devices against a test contactor and ensuring the initial temperature tolerance is not sufficient. The DUTs could be within their defined temperature tolerance and have a relatively high thermal resistance path to the surrounding environment. When powered, the lack of a heat sink can cause the device temperature to rise beyond its test tolerance.

However, the options for heat-sink designs in test-site thermal systems can be limited. One means to implement a heat sink is to temperature control the contactor assembly and provide intimate contact between the DUT body and the contactor assembly (Figure 8) [21].

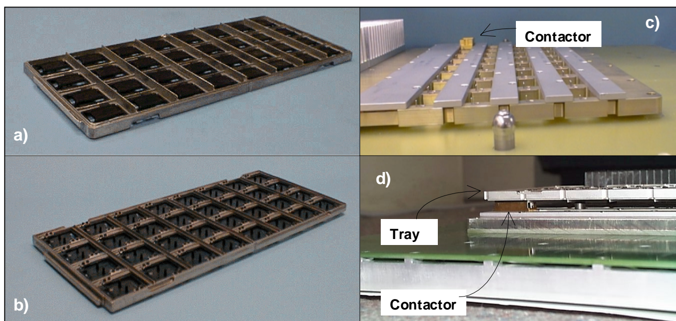

Figure 8. a) Top view of test tray; b) bottom view of test tray; c) side view of temperature-controlled contactor thermal plate; d) side view of tray placed against temperature-controlled contactor engaging one contactor.

In Figure 8d, individual spring-loaded plungers (not shown) press all the devices, captured in the plastic insert of the tray, against the electrical test contactors. The contactors (Figure 8c and 8d) are fastened to the temperature-controlled plate and are made of a high-thermal conductivity material such as aluminum. The entire contactor assembly therefore works as a fixed-temperature heat sink.

One could improve the heat transfer between the DUT body and the heat sink with an interface material. Almost all thermal greases and interface pad materials, however, do not offer a means to repeatedly remove a heat sink connected to sequentially tested devices (which in handlers can be thought of as the device pushers), without contaminating the DUT package or damaging the interface material. The tackiness of a pad tends to tear it when the heat sink separates from the DUT. Furthermore, heat-sink clamping forces are typically limited to a couple of pounds per device yielding at most 10 psi pressure, which is a very low clamping pressure. Some interface pads do exist that can be manufactured with an adhesive on only one side (that goes to the pusher). But, again, the inability to apply large clamping forces does not give any advantage to using these pads. Other options, which are not clearly documented for application in low-pressure microelectronic applications, include the use of coatings [26]. For plastic package devices, a significant contributor to high contact resistances is the low thermal conductivity of the molding compound.

Given the limitations on the achievable thermal contact resistance, the only other means to provide powered-DUT temperature control is to temperature control the DUT rather than the pusher or heat sink. In these cases, a means to rapidly cycle the pusher, heat sink and device inevitably means drastically cycling airflow temperatures or resorting to liquid thermal systems [15].

SUMMARY

The main thermal issues in DUT temperature control are presented and discussed. These include describing the different handler types, device and device-carrier construction and material properties, test-handler temperature capability requirements, test-handler slew times, DUT parallelism, and thermal throughput limitations.

The higher level thermal management tasks for device testing can be summarized as thermal conditioning and DUT temperature control. Compact thermal conditioning chambers capable of rapidly heating or cooling devices and their carriers are required. Also, DUT temperature-control systems capable of tight temperature tolerances even while the device is generating heat are required.

The systems and components described in Figures 6 and 8 are patent pending.

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