## FA 14.3: A Low-Power Differential CMOS Bandgap Reference

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The performance of many mixed analog/digital systems is limited by inaccuracies and power supply noise coupling errors in integrated voltage references [1, 2]. Reference circuitry also typically contributes a large fraction of the analog power consumption. The CMOS bandgap circuit described here provides a 2.0V differential voltage reference for a 10.24MHz oversampled data converter, and maintains high PSR and accuracy while consuming 2.2mW.

The bandgap reference is shown in Figure 1. A single bipolar core circuit establishes a PTAT reference current, a single-ended bandgap voltage, $V_{bg}$, with respect to ground, and an additional voltage, $V_x$, used in the differential reference. Both p-channel and n-channel devices, $M_{P1}$-$M_{P4}$ and $M_{N1}$-$M_{N2}$, are cascoded to improve the PSR. A conventional high-swing cascode current mirror, shown in Figure 2a, requires power-consuming cascode bias circuitry. A self-biasing high-swing cascode technique, illustrated in Figure 2b, uses a resistor to develop a bias voltage. The voltage drop across the resistor is maintained slightly larger than $V_{DSAT}$ of the cascode devices. This ensures that the mirror devices operate near the edge of the saturation region, providing low-voltage operation with high output impedance. Resistors $R_6$ and $R_7$, implemented in the bipolar core circuit of Figure 1, provide bias voltages for cascode devices $M_{P6}$-$M_{P10}$ and $M_{N3}$-$M_{N4}$, respectively.

The differential reference voltage is generated by sourcing a current with positive temperature coefficient from $M_{P5}$ and $M_{P10}$ into resistor $R_2$ and sinking a current with negative temperature coefficient into $M_{N6}$ from resistor $R_4$. The current in $M_{P5}$ and $M_{P10}$ is mirrored from the PTAT current flowing in bandgap core transistors $M_{P2}$ and $M_{P7}$. Resistor $R_2$ develops a voltage drop, $V_{R2}$, proportional to the thermal voltage of the bipolar transistors. The current in $M_{N6}$ is proportional to the base-emitter voltage, $V_{be4}$, of transistor $Q_4$ by using large matched devices for $M_{N5}$ and $M_{N6}$ to establish a voltage drop equal to $V_{be4}$ across resistor $R_3$. Resistor $R_4$ develops a voltage drop, $V_{R4}$, proportional to $V_{be4}$. Amplifier $A_2$ maintains equal voltages at the drains of $M_{P10}$ and $M_{N6}$ and establishes a temperature-independent voltage, $V_{ref}$, at its output equal to the sum of $V_{R2}$ and $V_{R4}$. Common-mode feedback in $A_2$ maintains a constant common-mode level in the output. Although the input common-mode level varies with temperature, the impact on $V_{ref}$ is less than 2ppm/°C with an amplifier CMRR of only 60dB. Direct scaling of $V_{ref}$ is by adjusting the values of $R_2$ and $R_4$ relative to $R_1$ and $R_3$, respectively. The ratio of $R_1$ to $R_3$ is adjusted to null the reference temperature coefficient, allowing $R_2$ and $R_4$ to have similar values for differential matching.

The PSR advantages of differential circuit implementation are obtained with little additional circuit complexity and power consumption. The simplicity of the amplifier feedback circuitry makes amplifier settling time independent of the high-frequency characteristics of the parasitic pnp transistors in the CMOS process. In contrast, many continuous-time reference circuits use parasitic pnp devices and current mirror circuitry in the feedback network around an operational amplifier. The settling time of switched-capacitor bandgap circuits is also typically limited by the parasitic pnp characteristics.

Supply regulation is added to improve the low-frequency PSR of the differential reference within the 40kHz signal bandwidth of the oversampled data converter. A 4V regulated supply is generated by amplifying the bandgap voltage, $V_{bg}$, using amplifier $A_1$. This feature is implemented at the minimal expense of a 500mV drop in the minimum 4.5V supply voltage and of 500μW of additional power consumption in amplifier $A_1$. Startup circuitry is added to ensure that $V_{bg}$ and the regulated supply do not remain at ground when power is applied. Comparator $C_1$ provides a power-up signal to amplifier $A_1$, forcing the amplifier output equal to $V_{DD}$ during startup conditions.

Supply regulation amplifier $A_1$ in Figure 3 uses a low-power output stage optimized for high PSR. Current in the drain of source follower device $M_{P14}$ is amplified using devices $M_{N9}$-$M_{N13}$ and mirrored back into the source of $M_{P14}$ to close the negative feedback loop. The resulting low-impedance Class AB buffer stage sources and sinks large output currents. The negative feedback maintains constant current in source-follower device $M_{P14}$, boosting its transconductance and decreasing its output impedance by a factor of $1+A_1$, where $A_1$ is the current gain of the feedback circuit. Capacitors $C_{C1}$ and $C_{C2}$ give frequency compensation without the high-frequency PSR degradation of conventional Miller-compensated two-stage amplifiers [3].

Differential reference amplifier $A_2$ uses complementary output buffer structures similar to those in $A_1$, with source follower buffer devices at amplifier outputs placed in local feedback for enhanced large-signal current drive, class AB operation, and reduced output impedance. Amplifier $A_2$ is for use with a 0.1μF regulation capacitor across the amplifier outputs for low output impedance at the 10.24MHz data converter clock rate.

Device matching errors contributing to reference variation are minimized by common-centroid layout. Devices are sized to minimize device variations and the reference sensitivities to these variations, and more layout area is allotted to devices causing greater reference variation. Table 1 summarizes performance of the bandgap reference. Statistics for the reference and regulated supply voltages are from a sample of 30 parts from the first wafer lot of an uncharacterized process.

Three sets of supply rejection data for the differential reference are given in Figure 4: reference by itself, reference with supply regulation, and reference with both supply regulation and 0.1μF output capacitor. Supply noise between 40kHz and 10.20MHz is removed by a filter following the data converter and does not affect system performance. Rejection is at least 79dB over frequencies of interest when the circuit is used with regulated supply and 0.1μF capacitor across reference outputs.

*Acknowledgments*

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*References*

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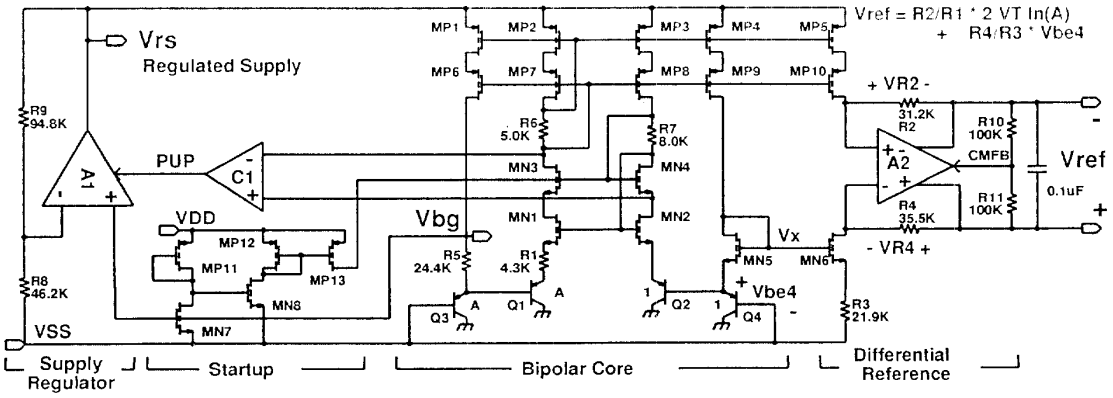


**Figure 1: Bandgap reference.**

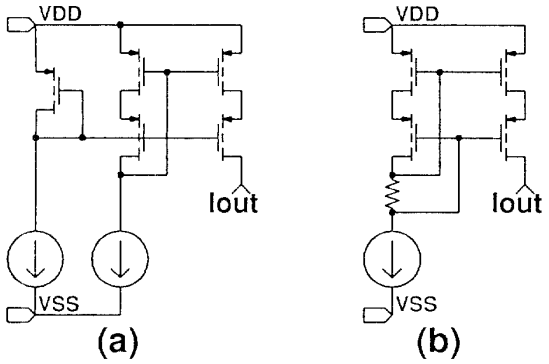


**Figure 2: High-swing cascode current mirror.; (a) conventional, (b) self-biased.**

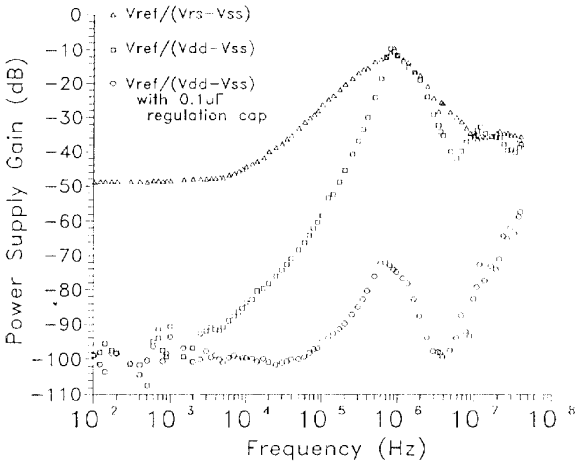


**Figure 4: Measured power supply rejection of differential reference.**

**Figure 5: See page 346.**

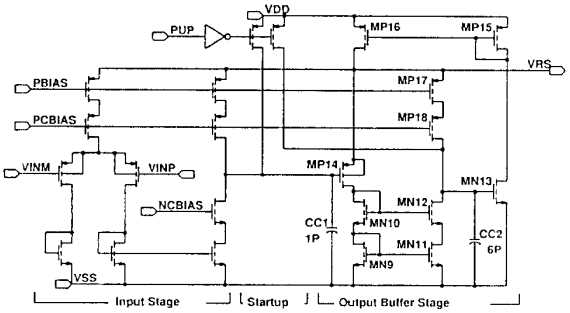


**Figure 3: Supply regulation amplifier A1.**

| | |
|---|---|
| Mean Vref at 25°C | 2.005V |
| Standard Deviation of $V_{ref}$ | 5.5mV |
| Temperature Coef. of $V_{ref}$ (first samples) | +115ppm/°C |
| Mean of regulated supply voltage at 25°C | 4.119V |
| Standard Deviation of regulated supply voltage | 21.7mV |
| Power dissipation: Bipolar core | 600µW |
| Supply regulator | 500µW |
| Differential reference | 990µW |
| Startup circuit | 110µW |
| TOTAL: | 2.2mW |
| Power Supply Rejection dc | 99 dB |
| Power Supply Rejection 100kHz | 58 dB |
| Power Supply Rejection 100kHz (0.1µF) | 95 dB |
| Supply Voltage | 5V±10% |
| Technology: CMOS n-well | 0.65µm |
| Active Area | 627mil² |

**Table 1: Performance summary.**