The Design of Low-Noise Bandgap References

Arie van Staveren, Student Member, IEEE, Chris J. M. Verhoeven, Member, IEEE, and Arthur H. M. van Roermund, Senior Member, IEEE

Abstract—The noise power of bandgap references is directly related to the current consumption of the bandgap reference. This paper describes the design of low-noise bandgap references. It is shown that for an idealized bandgap reference, a fundamental noise limit exists when the limited current consumption is a constraint. A design example is given of a 1 V bipolar bandgap reference with a current consumption of 5 μA. The output voltage is 200 mV and the mean temperature dependency is ≈20 ppm/K for 0 °C to 100 °C. The output noise density equals 166 nV/√Hz.

I. INTRODUCTION

A BANDGAP reference generates a dc voltage related to the bandgap energy at 0 K. Ideally the output voltage is temperature independent. Bandgap references are subcircuits which are widely used in electronics, e.g., A/D, D/A converters, measurement and instrumentation circuits, et cetera.

In the literature [1], [2], four main quality aspects of bandgap references can be found: the mean relative temperature dependency, the accuracy, the output impedance, and the power consumption. The mean relative temperature dependency is generally expressed in parts per million per Kelvin (ppm/K) and depends on the order of temperature compensation. Depending on the temperature range, first-order compensated references have a temperature dependency in the order of 10 ppm/K [3]–[5]. With a curvature correction or a second-order compensation, the temperature dependency can be decreased to only a few ppm/K [6]–[8]. Of course, when the temperature range of interest is larger, the temperature dependency is higher.

The accuracy is a measure of all the stochastic influences: matching errors of transistors and resistors and the variation of process parameters [9]. As a bandgap reference is a voltage source, its output impedance must be low to have a negligible influence of the load on the reference voltage. Finally, the power consumption has to be low because of self-heating effects and efficiency.

In electronic design systematics there are three fundamental limitations [10]: speed, noise, and power. These limitations also hold for the design of bandgap references and can be translated into design criteria or quality aspects with respect to bandgap references. The attainable bandwidth of the output impedance is limited by the speed of the devices used. The accuracy of the output voltage is limited by stochastic processes, e.g., matching errors, tolerances on absolute values, and noise generated in the devices (shot noise, thermal noise, et cetera). Generally, the performance of the circuit improves when the power consumption is increased.

In the literature, much attention is paid to all but one of these quality aspects. The influence of the noise, generated by the devices (shot noise, thermal noise, et cetera) on the output voltage is generally not treated explicitly.

A bandgap reference itself is not a signal-processing circuit, but the noise at the output can be very disadvantageous for signal-processing circuits that, e.g., refer their bias quantities to the bandgap reference voltage. Thus noise performance can be an important design criterion, especially in the growing area of low-power, low-voltage design.

This paper deals with the noise behavior of first-order compensated bandgap references. First, a general model for the bandgap reference is derived in order to be able to find a general expression for the noise behavior of an idealized bandgap reference. Subsequently, the minimum is derived for this expression, resulting in a fundamental limit for the noise behavior with a restricted current consumption. In the succeeding sections, an implementation of a low-voltage (1 V) low-power (5 μW) bandgap reference is described to see what prevents the bandgap reference in reaching the fundamental noise limit.

II. A GENERAL MODEL FOR A FIRST-ORDER COMPENSATED BANDGAP REFERENCE

The output voltage of a bandgap reference $V_{REF}(T)$, can be written as a Taylor series around a reference temperature $T_r$:

$$V_{REF}(T) = V_{REF}(T_r) + a_1(T - T_r) + a_2(T - T_r)^2 + \cdots$$

in which $V_{REF}(T_r)$ is the output voltage at the reference temperature $T_r$ and $a_1, \ldots, a_n$ are the Taylor coefficients. The simplest bandgap reference is the one in which just $a_1$ is made zero. This bandgap reference is called a first-order compensated bandgap reference. First-order compensation can be achieved with a suitable linear combination of only two base-emitter voltages. The remaining temperature dependency of this bandgap reference is of the second and higher-order.

For the output voltage of the bandgap reference can be written as:

$$V_{REF} = a_1 V_{BE1} + a_2 V_{BE2}$$

and

$$\frac{dV_{REF}}{dT} \bigg|_{T_r} = 0.$$
respective, and \( T \) the absolute temperature. Fig. 1 depicts a block diagram of a first-order compensated bandgap reference.

According to (2) and (3), four variables have to be set by the designer
- \( a_1 \);
- \( a_2 \);
- \( V_{BE1} \);
- \( V_{BE2} \).

In the following sections, the influence of a noise minimization upon these parameters is treated.

### General First-Order Compensation

In this paper, all the mathematics are done up to the first order. Therefore, a first-order model for the base-emitter voltage is also used. An expression for the \( V_{BE} \) can be derived in a few steps. The basic equation is the transistor equation

\[
I_C = I_S \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right]
\]

in which \( I_C \) is the collector current, \( I_S \) the saturation current of the transistor, \( q \) the electron charge and \( k \) the Boltzmann constant. Here the simplest model for the relation \( I_C - V_{BE} \) is used because the key item in this paper is not the accuracy of the bandgap reference, but the minimization of the noise performance. The saturation current depends on the extrapolated bandgap energy at \( T = 0 \) K, \( E_{G0} \), \((\approx 1.2 \text{ eV for silicon})\) as

\[
I_S = C \left( \frac{T}{T_r} \right) ^ \eta \exp \left( - \frac{E_{G0}}{kT} \right)
\]

where \( C \) is a constant and \( \eta \) the order of the temperature dependency of the saturation current.

Collector bias currents, which are easy to make in practice, are the constant current and the current proportional to the absolute temperature (PTAT). Both currents can be expressed by

\[
I_{BIAS}(T) = I_{BIAS}(T_r) \left( \frac{T}{T_r} \right) ^ \eta
\]

in which \( \eta \) is the order of the temperature dependency of the current. For a constant current, \( \eta = 0 \) and for a PTAT current, \( \eta = 1 \). When this type of current is used as the bias current for the transistors, the expression for \( V_{BE} \) found by combining (4), (5), and (6) and assuming that the \( -1 \) term in (4) is negligible, equals

\[
V_{BE}(T) = \frac{E_{G0}}{q} + \frac{kT}{q} \ln \left( \frac{I_C(T_r)}{C} \right) - \frac{(\eta - \theta)kT}{q} \ln \left( \frac{T}{T_r} \right)
\]

Rewriting (7), the two constants \( I_C(T_r) \) and \( C \) can be eliminated [11]. Taking the first two terms of the Taylor expansion of the resulting equation, a first-order model for \( V_{BE}(T) \) is found [11]

\[
V_{BE}(T) = V_{BE}(T_r) + \frac{E_{G0}}{q} - \frac{kT}{q} (\eta - \theta) \frac{T - T_r}{T_r}
\]

in which \( E_{G0} \) is the extrapolated bandgap energy at \( T = 0 \) K. To make the equation more compact an effective bandgap voltage \( (V_{G'}) \) is defined at the reference temperature \( T_r \) as

\[
V_{G'} = \frac{E_{G0}}{q} + \frac{kT_r}{q} (\eta - \theta)
\]

Substitution of (9) in (8) yields

\[
V_{BE}(T) = V_{BE}(T_r) + V_{BE}(T_r) - V_{G'} \frac{T - T_r}{T_r}
\]

Equations (2), (3), and (10) are the starting point for the derivation of the noise properties of the idealized bandgap references. Substitution of (10) in (2) for \( V_{BE1} \) and \( V_{BE2} \) yields

\[
V_{REF} = a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) + \left[ a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) - (a_1 + a_2) V_{G'} \right] \times \frac{T - T_r}{T_r}
\]

In this equation, the first two terms are the constant terms whose sum has to be made equal to the desired reference voltage. The terms between the straight brackets represent the first-order temperature behavior which must be made equal to zero. These two constraints result in the following two equations

\[
a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) = V_{REF}
\]

Solving these two equations for \( a_1 \) and \( a_2 \) results

\[
\begin{align*}
\frac{a_1}{V_{G'}} &= \frac{V_{REF} - V_{BE2}(T_r)}{V_{BE1}(T_r) - V_{BE2}(T_r)} \quad \text{(12)} \\
\frac{a_2}{V_{G'}} &= \frac{V_{REF} - V_{BE1}(T_r)}{V_{BE1}(T_r) - V_{BE2}(T_r)} \quad \text{(13)}
\end{align*}
\]

According to these two equations \( a_1 \) and \( a_2 \) have opposite signs. This is because the first-order coefficient of the \( V_{BE} \) is always negative, so a difference of two scaled base-emitter voltages must be taken to obtain compensation.

### III. Noise of the General Idealized Bandgap Reference

The first-order compensated bandgap reference contains five blocks: two base-emitter voltage generators, two blocks for scaling the base-emitter voltages, and an adder. The base-emitter voltage cannot be noise free. To obtain a nonzero base-emitter voltage, a nonzero collector bias current is required, and thus a base-emitter voltage is inherently deteriorated by the shot noise of the collector. Fundamentally, the scaler and the adder can be made noise free. So, the lower boundary of the noise is determined by the two base-emitter voltages.
Fig. 2. The noise sources in the VBE-source.

The sources 2qIc/β and 2kTβ/RB are the equivalent input noise sources of the collector shot noise transformed with the K-matrix of the transistor [10]. 2qIc represents the shot noise caused by the excess-noise corner frequency. The sources 2qIc/2 and 2kTβ/bar are the equivalent input noise sources of the base shot noise and the thermal noise due to the base resistance RB.

The two current-noise sources can be ignored because of the zero output impedance of the nullor used for the biasing (see Fig. 3). The base resistance must be made negligible to obtain the lowest noise level possible. For low-current applications, the base resistance can easily be made negligible because RB ≪ VREF/2kT is fairly simple to obtain. In cases where the currents are relatively high, more base contacts and several transistors in parallel can be used.

Thus the power density of the dominant voltage noise source (Sv) is given by

\[ S_v = 2kT \frac{kT}{qI_C}. \] (16)

Fig. 3 depicts a basic cell. It comprises the base-emitter voltage source and a scaler with scaling factor a. The transistor is properly biased by the nullor.

In order to find an expression for the noise at the output of the bandgap reference, the dominant noise source of the transistor is transformed to the output of the basic cell. For the noise power density Sout at the output of the basic cell holds

\[ S_{out} = 2kTa^2 \left( \frac{kT}{qI_C} \right) \] (17)

with a the scaling factor.

The general first-order compensated bandgap reference contains two basic cells, so the total noise density at the output of the bandgap reference (Sref) equals the sum of the noise contributions of the two basic cells

\[ S_{ref} = 2kT \left( a_1^2 \frac{kT}{qI_{C1}} + a_2^2 \frac{kT}{qI_{C2}} \right). \] (18)

Substitution of the expressions for a1 and a2 (14) and (15) results in

\[ S_{ref} = 2kT \frac{V_{BE1}^2}{V_g^2} \frac{[V_{G1} - V_{BE2}(T_r)]^{2} \frac{kT}{qI_{C1}} + [V_{G2} - V_{BE1}(T_r)]^{2} \frac{kT}{qI_{C2}}}{[V_{BE1}(T_r) - V_{BE2}(T_r)]^2}. \] (19)

Minimization of the noise level results in infinitely large currents, as the base-emitter voltages needs to be as large as possible. Therefore, (19) is written as a function of currents and a maximal current consumption, \( I_{\text{MAX}} \), is introduced

\[ I_{\text{MAX}} = I_{C1} + I_{C2}. \] (20)

Equation (19) changes into (21), shown at the bottom of this page.

This noise power density has been depicted as a function of \( I_{C1} \) for four different situations in Figs. 4-7. In Fig. 4, the saturation currents \( I_{S1} \) and \( I_{S2} \) are equal and the current consumption is limited to 1.25 \( \mu A \). Fig. 5 shows the noise power density in the case of equal saturation currents but with a current limitation of 12.5 \( \mu A \). Figs. 6 and 7 show the noise power density in the case of scaled emitter areas \( I_{S2}/I_{S1} = 10 \) with a current limitation of 1.25 \( \mu A \) and 12.5 \( \mu A \), respectively. In the four situations, for the constants the following values are used: \( V_{\text{REF}} = 0.2 \) V, \( V_G = 1.19 \) V en \( T = T_r = 300 \) K.

Clearly, the noise power has a minimum. The difference between Figs. 4 and 5 and between Figs. 6 and 7 is the level of the noise power; the shape of the functions is the same.

According to Figs. 4–7, the shape of the function is independent of \( I_{\text{MAX}} \), and thus the location of the minimum is also independent of \( I_{\text{MAX}} \).

A difference between Figs. 4, 5 and 6, 7 is that the peak in the middle of Figs. 4, 5 is shifted out of the middle as
in Figs. in 6, 7. This is due to the denominator of (21). The denominator contains a factor

$$\left[ \ln \left( \frac{I_{C1}}{I_{\text{MAX}} - I_{C1}} \frac{I_{S2}}{I_{S1}} \right) \right]^2. \quad (22)$$

When $I_{C1}$ equals

$$I_{C1} = I_{\text{MAX}} \frac{I_{S2}}{I_{S1} + I_{S2}} \quad (23)$$

the denominator of (21) is zero, which results in an infinite noise power density. Equation (23) is fulfilled when the two base-emitter voltages are equal. When the base-emitter voltages are equal, the scaling factors $a_1$ and $a_2$ become infinite (14), (15) and the noise of the two transistors is infinitely amplified. Thus the shift of the peak in Figs. 4-7 is caused by the change of the ratio $I_{S1}/I_{S2}$ resulting in a change of the collector current $I_{C1}$ at which the two base-emitter voltages are equal.

The peaks at both borders of the figures are caused by a collector current that is becoming very small. A very small collector current corresponds to a very large equivalent noise voltage at the input of the transistor (17), resulting in a very large noise voltage at the output of the bandgap reference.

Figs. 4–7 suggest that an optimal ratio of the two collector bias currents $I_{C1}/I_{C2}$ can be found. This ratio yields minimum noise power. This optimal ratio for a given scaling $I_{S1}/I_{S2}$ is independent of $I_{\text{MAX}}$ and will be derived in the next section.

The Fundamental Noise Limit of the Idealized Bandgap Reference

To find the optimal ratio $I_{C1}/I_{C2}$ for a given ratio of $I_{S1}$ and $I_{S2}$, it is convenient to replace $I_{C1}$ by $xI_{\text{MAX}}$

$$I_{C1} = xI_{\text{MAX}}. \quad (24)$$

Substitution of (24) in (21) yields (25), shown at the bottom of the next page.

To find a convenient expression for the minimum, some approximations have to be made for which two variables are
Substitution of these two variables in (25) results in a new expression for the noise power density

\[
S_{ref} = 2q \frac{V_{REF}^2}{V_G^2} \left( \frac{T}{T_r} \right)^2 \frac{x b_1 + (1-x)b_2}{x(1-x)I_{MAX} \left[ \ln \left( \frac{x}{1-x} \cdot \frac{I_{MAX}}{I_{S1}} \right) \right]^2}.
\]

(28)

For the calculation of the derivative with respect to \( x \), the following approximation is made

\[
b_1 + x \frac{db_1}{dx} - b_2 + (1-x) \frac{db_2}{dx} \approx b_1 - b_2.
\]

(29)

This approximation is valid if the following holds

\[
V_G' \gg \frac{kT}{q}.
\]

(30)

This condition is fulfilled in all practical situations. Using the approximation of (29), the derivative of (28) equals (31), shown at the bottom of the next page, in which \( A \) equals

\[
A = \frac{2q}{I_{MAX}} \left( \frac{V_{REF}}{V_G} \cdot \frac{T}{T_r} \right)^2.
\]

(32)

The relevant extremes are found from

\[
x(b_1 - b_2) \left[ x \ln \left( \frac{x}{1-x} \cdot \frac{I_{S2}}{I_{S1}} \right) - 2 \right] - b_2 \left[ (1-2x) \ln \left( \frac{x}{1-x} \cdot \frac{I_{S2}}{I_{S1}} \right) + 2 \right] = 0.
\]

(33)

The first term can be ignored with respect to the second term because \((b_1 - b_2)x \ll b_2\). The resulting equation to be solved is

\[
b_2 \left[ (1-2x) \ln \left( \frac{x}{1-x} \cdot \frac{I_{S2}}{I_{S1}} \right) + 2 \right] = 0.
\]

(34)

For \( b_2 \neq 0 \), the solution of this equation is

\[
\ln \left( \frac{x}{1-x} \cdot \frac{I_{S2}}{I_{S1}} \right) = -\frac{2}{1-2x}.
\]

(35)

This gives the optimal relation between \( I_{C1} \) and the total current consumption. The argument of the \( \ln \)-function on the left-hand side of (35) can be rewritten as

\[
\text{argument} = \frac{I_{C1}}{I_{C2}} \frac{I_{S1}}{I_{S2}}.
\]

(36)

This makes the following transformation of variables convenient

\[
y = \frac{I_{C1}}{I_{C2}} = \frac{x}{1-x}
\]

(37)

with \( y \) the ratio of the collector bias currents. This transformation leads to the final solution

\[
\ln \left( \frac{I_{S2}}{I_{S1}} \right) = -\frac{2 + y}{1 - y}.
\]

(38)

Only the ratio of the two bias currents \( y \) and the ratio of the two saturation currents appear in the expression. The sum of the two bias currents does not influence the location of the minimum.

Equation (38) is solved for the examples in Figs. 4–7. Table I gives the optimal ratios \((y_1 \text{ and } y_2)\) of collector currents for a given ratio of saturation currents at which the noise is minimal. The minimal noise level is also given.

<table>
<thead>
<tr>
<th>Figure</th>
<th>( I_{S2}/I_{S1} )</th>
<th>( y_1 )</th>
<th>( y_2 )</th>
<th>( n_\text{min} ) [nV/√Hz] at ( y_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1</td>
<td>11.0</td>
<td>1/11</td>
<td>70</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>11.0</td>
<td>1/11</td>
<td>20</td>
</tr>
<tr>
<td>6</td>
<td>10</td>
<td>3.5</td>
<td>0.01</td>
<td>33</td>
</tr>
<tr>
<td>7</td>
<td>10</td>
<td>3.5</td>
<td>0.01</td>
<td>9.3</td>
</tr>
</tbody>
</table>

This makes the following transformation of variables convenient

\[
y = \frac{I_{C1}}{I_{C2}} = \frac{x}{1-x}
\]

(37)

with \( y \) the ratio of the collector bias currents. This transformation leads to the final solution

\[
\ln \left( \frac{I_{S2}}{I_{S1}} \right) = -\frac{2 + y}{1 - y}.
\]

(38)

Only the ratio of the two bias currents \( y \) and the ratio of the two saturation currents appear in the expression. The sum of the two bias currents does not influence the location of the minimum.

Equation (38) is solved for the examples in Figs. 4–7. Table I gives the optimal ratios \((y_1 \text{ and } y_2)\) of collector currents for a given ratio of saturation currents at which the noise is minimal. The minimal noise level is also given.

To make a first-order compensated bandgap reference with a linear combination of two base-emitters voltages, the ratio of the collector currents must be approximately 11:1 for optimal noise performance, with two equal transistors and 3.5:1 when the ratio of the two emitter areas is 1:10. Furthermore, it is not possible to obtain a noise level below 20 nV/√Hz for a first-order compensated bandgap reference with scaling 1:1, a total of 12.5 μA collector current and \( V_{REF} = 200 \text{ mV} \). When a lower noise level is required, either the current consumption must be increased or the scaling ratio has to be made larger.

**IV. A DESIGN EXAMPLE OF A LOW-NOISE BANDGAP REFERENCE**

The noise behavior of an idealized bandgap reference was treated in the previous sections. In practice, bandgap references are always nonideal. In the remaining sections, a design...
example of a low-noise bandgap reference will be given to
determine which parts of the implementation contribute in
addition to the noise, so that the fundamental limit is not
reached. The bandgap reference to be designed is low-voltage
and low-power because in this application field the current
consumption is generally a limiting factor.

First some attention is paid to the block schematic of the
bandgap reference and in the following sections the blocks
are implemented one by one.

The Basic Diagram of the Design Example

To obtain a more simple circuit, one scaling factor is shifted
out of the bandgap reference. In Fig. 8, the block diagram of
the example bandgap reference is given. The block diagram
is derived from Fig. 1 by shifting scaler a2 through the summing
node and subsequently deleting this scaler at the output. As
the scaler a2 is temperature independent, the newly created
reference voltage is also temperature independent (V&F
= VREF/a2). Here it is assumed that scaler a2 is negative and
a1 is positive. Thus the summing node has to subtract VBE2
from the scaled VBE~. The noise optimization of the previous
sections still holds for this block diagram. Scaler a2 does not
contribute any noise in the optimization. So, when the ratio
of the reference voltage VREF and the noise voltage at the
output of a2 (Fig. 8) is optimal, the ratio at the input of a2,
V&REF/V&noise is also optimal.

But with shifting out one of the scaling factors the number of
degrees of freedom is reduced by one. This poses no problem
for this example because the noise behavior is the key issue
and not the value of the reference voltage.

The remaining scaling factor is totally determined by the
first-order compensation. The new scaling factor equals the
ratio of the two previously used scaling factors

$$a = \frac{V'_{G} - V_{BE2}}{V'_{G} - V_{BE1}} \quad (39)$$

and when the two base-emitter voltages are given, the reference
voltage is fixed (V&REF = aV&BE1 - V&BE2).

In Fig. 9, the first step down to a total implementation
is given. Transistor Qref1 and Qref2 are the transistors used
for the generation of the two required base-emitter voltages.
Nullor 1 forces the base-collector voltage of Qref1 to zero in
order to minimize the influence of the forward Early effect.
Furthermore, the input current of the nullor is zero, and thus
the current from source I1 flows completely through the
collector lead of Qref1. Finally, the nullor buffers the base-
emitter voltage such that load currents do not influence the
base-emitter voltage. Nullor 2 performs the same as Nullor 1
does, but now for transistor Qref2.

For this example, the scaling ratio of the two reference
transistors is chosen to be 1:10. The resulting optimal cur-
rent division follows from (38) as 1:0.28. When a current
consumption of 1.25 μA is chosen the two collector currents
needs to be approximately

$$I_{Gref1} = 1 \mu A \quad (40)$$
$$I_{Gref2} = 0.25 \mu A. \quad (41)$$

The biasing point is chosen somewhat beside the optimum in
order to get a convenient scaling ratio between the two bias
currents. But as the noise-versus-current-division graphic is
relatively flat, the influence up on the noise level is negligible
(Fig. 6). For transistor1 a transistor with a saturation current
of IS = 16 aA is used.¹ Now the reference voltage equals to

$$V_{REF}' \approx 206 \ mV. \quad (42)$$

The design is done for integration in the DIMES01 process
[12], which is a bipolar process. In the next section the two
base-emitter voltage generators will be implemented.

V. IMPLEMENTATION OF THE TWO
BASE-EMITTER VOLTAGE GENERATORS

The implementation for the first base-emitter voltage generator is given in Fig. 10. Although the differential pair seems
to be the obvious choice for the input stage of the nullor
implementation, it is not used here. As the voltage at the
emitter nodes of the two transistors becomes relatively low,
the implementation of the tail current source is hampered.
However, when a CE-stage is chosen as an input stage this

¹In this value the influence of a reverse Early voltage of V&AR = 4 V is
incorporated. IS-with-V&AR = IS-without-V&AR (1 - V&BE/V&AR). For small
variations in V&BE the last factor can be assumed to be constant.
problem does not exist. But now the base-collector voltage of $Q_{ref1}$ is in the order of 0.1 V. Fortunately, the error introduced via the forward Early effect is still negligible because of the relatively high forward Early voltage. A current mirror is used to obtain a negative loop gain. The noise introduced by the nullor implementation is negligible because of the gain of the reference transistor. Frequency compensation is obtained by the pole-splitting network $R_{sp1}$ and $C_{sp1}$.

The implementation of the second base-emitter voltage generator is depicted in Fig. 11. For this nullor implementation, the drawback of the use of a differential pair as input stage is not apparent because the common-mode voltage of this nullor is 200 mV higher than it is for nullor 1. As the differential pair has a noninverting output, no additional stage is needed to obtain a negative loop gain. The noise introduced by the nullor implementation is negligible because of the gain of the reference transistor. Frequency compensation is obtained by the pole-splitting network $R_{sp1}$ and $C_{sp1}$.

The implementation of the second base-emitter voltage generator is depicted in Fig. 11. For this nullor implementation, the drawback of the use of a differential pair as input stage is not apparent because the common-mode voltage of this nullor is 200 mV higher than it is for nullor 1. As the differential pair has a noninverting output, no additional stage is needed to obtain a negative loop gain. The noise introduced by the nullor implementation is negligible because of the gain of the reference transistor. Frequency compensation is obtained by the pole-splitting network $R_{sp1}$ and $C_{sp1}$.

The implementation of the first base-emitter voltage generator is depicted in Fig. 10. For this nullor implementation, the drawback of the use of a differential pair as input stage is not apparent because the common-mode voltage of this nullor is 200 mV higher than it is for nullor 1. As the differential pair has a noninverting output, no additional stage is needed to obtain a negative loop gain. The noise introduced by the nullor implementation is negligible because of the gain of the reference transistor. Frequency compensation is obtained by the pole-splitting network $R_{sp1}$ and $C_{sp1}$.

At this point of the design, the total noise power density of the bandgap reference equals (compare with Table I)

$$S_{output} = 2kT(a^2r_{e1} + r_{e2}) = 34^2 \text{nV}^2/\text{Hz} \quad (43)$$

with $r_e = kT/qI_C$. In the next section, an implementation shall be made for the scaler.

The Implementation of the Scaler

In Fig. 9, the scaler was implemented as a negative-feedback voltage amplifier. This voltage amplifier is depicted again in Fig. 12.

The voltage gain $A_u$ is set by the ratio of the two resistors as

$$A_u = 1 + \frac{R_1}{R_2}. \quad (44)$$

The input offset voltage of the nullor implementation, is directly added to the reference voltage. So, this offset voltage must be as small as possible. Consequently, for the input stage a differential pair is chosen.

The output of the scaler has to supply for the current through the feedback network and the input current of the $V_{BE1}$ generator. The current through the feedback network is related to $V_{BE1}$ and thus temperature dependent. The input current of the $V_{BE2}$ generator equals its load current, as the generator acts as a floating voltage source, plus an input offset current. Without additional frequency compensation components the circuit already showed an acceptable frequency behavior. As for the $V_{BE1}$ generator, the noise is predominantly determined by the collector shot noise of the reference transistor.

At this point of the design, the total noise power density of the bandgap reference equals (compare with Table I)

$$S_{output} = 2kT(a^2r_{e1} + r_{e2}) = 34^2 \text{nV}^2/\text{Hz} \quad (43)$$

with $r_e = kT/qI_C$. In the next section, an implementation shall be made for the scaler.

The Implementation of the Scaler

In Fig. 9, the scaler was implemented as a negative-feedback voltage amplifier. This voltage amplifier is depicted again in Fig. 12.

The voltage gain $A_u$ is set by the ratio of the two resistors as

$$A_u = 1 + \frac{R_1}{R_2}. \quad (44)$$

The input offset voltage of the nullor implementation, is directly added to the reference voltage. So, this offset voltage must be as small as possible. Consequently, for the input stage a differential pair is chosen.

The output of the scaler has to supply for the current through the feedback network and the input current of the $V_{BE1}$ generator. The current through the feedback network is related to $V_{BE1}$ and thus temperature dependent. The input current of the $V_{BE2}$ generator equals its load current, as the generator acts as a floating voltage source, plus an input offset current. Without additional frequency compensation components the circuit already showed an acceptable frequency behavior. As for the $V_{BE1}$ generator, the noise is predominantly determined by the collector shot noise of the reference transistor.

At this point of the design, the total noise power density of the bandgap reference equals (compare with Table I)

$$S_{output} = 2kT(a^2r_{e1} + r_{e2}) = 34^2 \text{nV}^2/\text{Hz} \quad (43)$$

with $r_e = kT/qI_C$. In the next section, an implementation shall be made for the scaler.
is. But as the voltages across those resistors are determined by the base-emitter voltages, the current consumption is directly related to their noise performance. For a lower noise contribution, a higher current consumption is required.

For the current consumption of the resistors as a function of the base-emitter voltages it holds that

$$I_D = \frac{V_{BE1}}{R_2}$$

in which $I_D$ is the current through the feedback network. The influence of the equivalent input noise voltage of the scaler on the noise at the output of the reference is found by multiplying by the scaling factor $a$.

$$a = \frac{V_G - V_{BE2}}{V_G - V_{BE1}}$$

and the practical base-emitter voltages are limited to a relatively small range, the factor is more or less independent of the base-emitter voltages.

Concluding, the noise contribution due to the feedback resistors can only be reasonably reduced by increasing the current consumption. A compromise has to be made between the current consumption and noise contribution. For the feedback resistors the following values are chosen

$$R_1 = 500 \ \text{k}\Omega$$
$$R_2 = 500 \ \text{k}\Omega \cdot (1 - a) \approx 86.2 \ \text{k}\Omega$$
$$I_D \approx 1.3 \ \mu\text{A}$$

Resistors of this value are readily available in current technologies. Because the resistors set an amplification factor, only the matching is important. For these resistors the current consumption is approximately equal to the current consumption of the two reference transistors. The noise contribution is of the same order.

Now that the feedback resistors are known, a noise minimization for the input stage can be performed. Doing so, an optimal collector current of 3.5 $\mu$A for each transistor of the input stage is found. In that case, the equivalent noise resistor of the input stage amounts to 15 $\Omega$, which is negligible. But the current consumption is relatively high and thus a lower collector current is chosen: 0.5 $\mu$A for each input transistor.

Now the equivalent noise resistor equals 100 $\Omega$ and the noise contribution is of the order of the noise due to the $V_{BE2}$ generator.

The high-frequency behavior of the scaler is compensated by a pole-splitting network.

VI. THE COMPLETE CIRCUIT

Now all the parts have been implemented, the bias circuitry is designed. The total schematic of the bandgap reference including bias circuitry is depicted in Fig. 13.

The bias currents are referred to a PTAT current generated by the difference of two base-emitter voltages $Q_{PTAT_1}$ and $Q_{PTAT_2}$, together with $R_{PTAT}$. The noise contribution of this part to the noise of the bias currents is given by

$$S_{PTAT} = \frac{4kT}{R_{PTAT}} \left( r_{e,PTAT_{1,2}} + 1 \right).$$

To realize a negligible contribution to the noise, the currents in the PTAT source need to be relatively large ($r_{e,PTAT_{1,2}} \ll r_{e,Q_{PTAT}}$) and a large difference in the base-emitter voltage is needed in order to be able to use a high value for $R_{PTAT}$. In contrast, the noise due to the current mirrors on the top of the PTAT source and the transistors implementing the current bias sources can not be made negligible because of the power supply voltage of only 1 V. For this design example, the 1 V power supply voltages is a constraint. Thus lowering the influence of the noise of the PTAT current source must be done by increasing its current consumption.

As a compromise between current consumption and noise contribution, the following values are used for the PTAT source

$$I_{PTAT} = 0.25 \ \mu\text{A}$$
$$\Delta V_{BE,PTAT} = 18 \ \text{mV} @ \ 300 \ K \ (\text{scaling 1:2})$$
$$R_{PTAT} = 71.7 \ \text{k}\Omega.$$
Fig. 14. Simulation of the temperature behavior of the total bandgap reference.

Fig. 15. Simulation of the noise at the output of the total bandgap reference.

<table>
<thead>
<tr>
<th>Part</th>
<th>Contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BB1}$ generator</td>
<td>15 nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>$V_{BB2}$ generator</td>
<td>30 nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Voltage amplifier</td>
<td>54 nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Biasing circuit</td>
<td>153 nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Total</td>
<td>166 nV/$\sqrt{\text{Hz}}$</td>
</tr>
</tbody>
</table>

voltage differs slightly from 206 mV as was calculated before. This is caused by the trimming that was required because of a small temperature-dependent input offset voltage of the voltage amplifier. This trimming resulted in a small change of the nominal value. The cause of the small input offset voltage is twofold.

First, the influence of the load current of the scaler is not totally negligible. This influence can be reduced by adding a third amplifying stage. But problems can be expected with the frequency compensation.

Second, the mismatch between the tail-current source and the current from the PNP current source of the differential pair is such that it results in a nonnegligible offset voltage at the input. This mismatch is predominantly caused by the error due to the base currents in the mirror factor of the NPN mirror $Q_{m1}$ and $Q_{m2}$. This error can be reduced to a negligible level by connecting $Q_{m1}$ via amplifier stages as a diode (compare to the reduction of the influence of base-currents in the $V_{BE}$ generator). But as this bandgap reference is only a demonstrator for low-noise design, these measures are not taken.

In Fig. 15, a simulation result of the total noise contribution of the bandgap reference is depicted. The total noise amounts to approximately 166 nV/$\sqrt{\text{Hz}}$. The contributions of the different parts of the bandgap reference are given in Table II.

Note that the noise contribution of the biasing circuit is relatively large. This is inherent in low-voltage design (in this case 1 V). All the transistors used for the biasing contribute at least $2qI_C$ noise to the bias currents and the PTAT current source makes an additional contribution to the noise. Noise contribution can be minimized when emitter resistors are used. With the emitter resistors, the noise contribution can be reduced to $2qI_B$. However, to reach this, very large resistors and thus very high voltages for a given current are needed. It can be calculated fairly simply that in order to obtain a noise contribution of $4qI_B$, which is still negligible, the voltage across the emitter resistors needs to be approximately 5 V. Thus, when a supply voltage of the order of 6 V is available (5 V for the emitter resistors and 1 V for the circuit) the noise voltage can be reduced by a factor of 2.5 and only the noise of the two $V_{BE}$ generators and the voltage amplifier remain. For this reduction, the power consumption increases by approximately a factor 6, and thus the ratio of noise power and power consumption reduces slightly.

As the noise power of the bandgap reference is more or less inversely proportional to the current consumption, the same reduction in the noise voltage is possible by increasing the current consumption by approximately a factor of $(2.5)^2 = 6.25$. Here the power increase is a factor 6.25. So, compared to the previous situation, slightly more power is used. For this circuit, it is not very advantageous to use a charge pump circuit.

In conclusion, one can say that the performance versus power consumption of bandgap references is not degraded that much by the 1 V power supply constraint. For 1 V design, the influence of the bias sources on the noise behavior can be accounted for by just a factor. Of course this factor depends on how the bias circuit is designed.

The bias circuit not only contributes to the noise by its own shot noise. Noise from the power supply penetrates through the practical bias sources to the output of the bandgap reference and contributes to the noise as well. The sensitivity of the bandgap reference to power supply noise is determined by the implementation for the bias sources (how much noise is injected) and the transfer of the injected noise to the
output (what is seen of the injected noise). At relatively high frequencies in particular, it is hard to make a good implementation of the bias sources such that the injected noise is kept low. When the injected noise is predominant at high frequencies, additional measures in the bandgap reference circuit have to be taken such that noise injected at different nodes cancel at the output of the bandgap reference or are attenuated in the bandgap reference. These measures can be done independently of the noise optimization as discussed in this paper.

Besides the noise contribution due to the bias circuit, the noise of the scaler prevents the bandgap reference from reaching the fundamental limit. As was pointed out, more current through the feedback resistors and input stage reduces the noise contribution of the scaler, but the noise of the idealized bandgap reference (the two base-emitter voltage generators) also decreases when larger currents are used. Thus in the division of the total current between the two base-emitter voltage generators and the scaler there is an optimum at which the total noise level is minimal. The noise optimization described by the strategy in this paper will not be far from this global optimum. This is because the noise performance of the scaler is only slightly influenced by the values of the base-emitter voltages of the reference transistors (via the scaling factor (39)). Thus when noise of the two base-emitter voltages and the scaler are minimized separately and their levels are comparable, the total noise level will be close to the global optimum.

VII. CONCLUSION

In this paper, the noise performance of first-order compensated bandgap references is discussed. It is shown that for this type of bandgap reference, a fundamental limit exists in the relation between the noise and the current consumption. The noise power is minimal for a given scaling ratio of the two reference transistors when the ratio of collector currents \( y \) fulfills

\[
\ln \left( \frac{I_{S2}}{I_{S1}} \right) = -2 \frac{1 + y}{1 - y}.
\]

(55)

The ratio \( y_{\text{optimal}} \) is independent of the current consumption.

This fundamental limit was calculated for the most general bandgap reference. To see how close this minimum can be reached, a design example is discussed. For this example, it was found that the noise contribution of the voltage amplifier is of the same order of magnitude as the noise contribution of the base-emitter voltage generators. The same holds for the current consumption.

Furthermore, it was found that the noise performance of the bandgap reference, for a specified power consumption, is not degraded significantly when low supply voltages are used (1 V in this case). But to the contrary, the relation between the noise and current consumption is deteriorated by the biasing circuit in the case of low supply voltages.

REFERENCES


Arlie van Staveren (S’95) was born in Hazerswoude, The Netherlands, on April 19, 1968. He received the M.S. degree in electrical engineering from the Delft University of Technology, The Netherlands, in 1992. He is currently working toward the Ph.D. degree at the Electronics Research Laboratory.

Chris J. M. Verhoeven (M’92) was born in Hazerswoude, The Netherlands, on February 25, 1959. He received the M.S. degree in electrical engineering from the Delft University of Technology, The Netherlands, in 1985, and the Ph.D. degree in electrical engineering from the Electronics Research Laboratory in 1990. He is currently the project leader of the "Structured Electronic Design" group of the Electronics Research Laboratory in which the synthesis of analog basic circuits is addressed. To date, the main topics are amplifiers, continuous time filters, bandgap references, oscillators and neural devices.
Arthur H. M. van Roermund (M'83–SM'95) was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in electrical engineering in 1975 from the Delft University of Technology, The Netherlands, and the Ph.D. degree in applied sciences from the K. U. Leuven, Belgium, in 1987. From 1975 to 1992, he was with Philips Research Laboratories, Eindhoven. Initially, he worked in the Consumer Electronics group on design and integration of analog circuits and systems, especially switched-capacitor circuits. In 1987, he joined the Visual Communications Group where he has been engaged in video architectures and digital video signal processing. From 1987 to 1990 he was project leader of the Video Signal Processor project and from 1990 to 1992 of a Multiview Television project. Since 1992, he has been a Full Professor with the Electrical Engineering Department of the Delft University of Technology, where he heads the Electronics Department. The research activities of his group are accommodated in DIMES: the Delft Institute of Micro Electronics and Submicron Technology, where he heads the Circuits and Systems Section.