A Switched-Current, Switched-Capacitor Temperature Sensor in 0.6-μm CMOS

Mike Tuthill

Abstract—A temperature-to-digital converter is described which uses a sensor based on the principle of switching accurately scaled currents in the parasitic substrate p-n-p in a standard fine-line CMOS process. The resulting PTAT $\delta V_{BE}$ signal is amplified in an auto-zeroed switched-capacitor circuit, sampled, and converted to a digital output by a low-power 10-bit SAR ADC providing a resolution of 0.25 °C from −55 °C to 125 °C with an error of less than 1 °C. A single adjustment of temperature error is provided at wafer probe. No further calibration is required. A switching bandgap reference circuit will also be described which uses similar techniques to generate an accurate low-noise reference voltage for the ADC. The circuits are part of a multichannel data-acquisition system where other input voltages must also be sampled and measured, and so the speed and power of the ADC is not determined by the temperature sensor alone. For continuous operation, the supply current is 1 mA, but a low-power mode is provided where the part is normally in shut down and only powers up when required. In this mode, the average power supply current at 10 conversions/s is 0.3 μA. The supply voltage is 2.7–5.5 V.

Index Terms—Analog–digital conversion, CMOS analog integrated circuits, current, differential amplifiers, switched capacitor circuits, temperature measurement.

I. INTRODUCTION

A multichannel data-acquisition system has been developed for applications where a customer needs to monitor several voltages in his system, and also needs to monitor temperature. To maintain temperature accuracy, power dissipation must be minimized to prevent self-heating while still providing the required resolution and speed for the other channels. The sampling requirements on the input voltages to be measured dictated the use of a SAR architecture for the ADC rather than as used in [1]. The resulting product definition was for a 100 kilosample/s, 10-bit ADC with four input channels plus temperature, as shown in the block diagram in Fig. 1. The conversion time when measuring temperature is extended to 25 μs. A digital comparator is used to activate an output when the result of a temperature measured exceeds that written to an on-chip register. Operation with internal reference is enabled by grounding the REFIN pin. The supply range is 2.7–5.5 V at room temperature. Thus, the circuitry that processes this signal on chip must have a low offset voltage and good noise performance. However, even with perfect follow-on circuitry, a significant error source remains in the $V_{BE}$ mismatch of the substrate p-n-p’s at different current densities. The technique of measuring temperature by comparing the difference in the base–emitter voltage of two transistors at different current densities is well known [2]. This technique normally needs isolated bipolar transistors, but has also been implemented in CMOS by using the parasitic substrate p-n-p transistors in an n-well process [1]. This difference signal is proportional-to-absolute-temperature or PTAT and may be written as

$$\delta V_{BE} = (kT/q) \cdot \ln\left(\frac{I_{C1} \cdot A_2}{I_{C2} \cdot A_1}\right)$$

where $A$ is a scale factor relating to the emitter area, $I_{C1}$ and $I_{C2}$ are the collector currents in the two transistors, $k$ is Boltzmann’s constant, $q$ is the electronic charge, and $T$ is the temperature in degrees kelvin. A current density ratio of 8 has been used in many published circuits, giving a $\delta V_{BE}$ of 53 mV at room temperature. Thus, the circuitry that processes this signal on chip must have a low offset voltage and good noise performance. However, even with perfect follow-on circuitry, a significant error source remains in the $V_{BE}$ mismatch of the substrate p-n-p’s at different current densities. The error is also a scale-factor error which cannot be corrected by a single temperature adjustment, and is the dominant error source when this type of sensor is used in a precision bipolar

Fig. 1. Block diagram of multichannel ADC with temperature sensor.

1 μW at 10 conversions/s. The ADC used is a conventional switched-capacitor circuit, so this paper will focus on the design of the temperature sensor and bandgap reference, and will present the performance data.

II. INTEGRATED TEMPERATURE SENSORS
As a continuous output is not required from a temperature sensor when used with an ADC, a single p-n-p may be used at switched currents as in Fig. 2, thus removing this matching requirement. The $\delta V_{BE}$ signal is $(kT/q) \cdot \ln(N)$, where $N$ is the current ratio. This equation only remains accurate if the current gain of the p-n-p is constant over the range of switched currents used as the collector current is not available. The signal is subtracted from $V_{BE}$ and amplified in the switched capacitor circuit. The absolute value of the current used is not critical; only the ratio is important, and so, precision, low-temperature coefficient resistors are not required. The dominant error sources now are the accuracy of the ratio $N$ and the amplifier offset voltage. The accuracy to be expected for $N$ may be predicted from the manufacturing yield of current–source digital-to-analog converters where 9-bit linearity is easily achieved. With 0.2% accuracy in $N$ and the same ratio of 8, the resulting error is a mere $51 \mu V$. The offset voltage and $1/f$ noise of the CMOS amplifier may be eliminated by normal switched-capacitor techniques as a static or continuous-time output is not required. This is dealt with later in the paper.

Fig. 3 shows a development of the basic circuit where two p-n-p’s are used to generate a $2 \cdot \delta V_{BE}$ signal from one switching action of the current sources, while maintaining a constant supply current. As the $V_{BE}$ of one transistor switches from a low to a high value, the $V_{BE}$ of the other transistor switches from high to a low value. The two $\delta V_{BE}$ signals are summed in a differential switched-capacitor circuit. Although two transistors are now used, there is no matching requirement between them. Only the $\delta V_{BE}$ of each transistor at the switched currents is summed in the amplifier. Generating a $2 \cdot \delta V_{BE}$ signal from currents $I$ and $N(I)$ provides the same total signal level as the single transistor circuit if run at $I$ and $(N)^2 \cdot I$, and so provides a significant improvement in power dissipation. The amplifier is auto-zeroed to remove offset and $1/f$ noise by the action of switches $S_3$–$S_6$. In auto-zero, $C_3$ and $C_4$ are connected to the common-mode bias voltage $V_{CM}$ which is also fed to the common-mode control input of the amplifier, and $S_3$ and $S_4$ are closed. When $S_3$ and $S_4$ open, the offset voltage is stored on the feedback capacitors, which are then connected to the amplifier outputs by control signal CLK2 and its complement CLK2B. CLK3 then switches the bias currents to create the $\delta V_{BE}$ signals. When switches $S_3$ and $S_4$ open, the charge injection is common mode, and so is rejected.
A further improvement in performance may be achieved by taking multiple \(2 \cdot \delta V_{BE}\) samples by switching the \(I\) and \(N(I)\) currents back and forth several times and summing the samples. This will give an average value of temperature during the time taken. Switches are added at the right-hand side of the input capacitors such that as the current in the p-n-p’s is switched back and forth, the resulting \(\delta V_{BE}\) samples are integrated as shown in the circuit and timing diagram of Fig. 4. The current is switched back and forth four times, giving a further factor of two improvement in noise and a reduction by four of the required amplifier gain. This technique requires more complex offset cancellation as the amplifier must be chopped in phase with the current switching. The output voltage of the final circuit is

\[V_{out,off} = \left(8 \cdot kT/q\right) \cdot \ln(N) \cdot \left(C_{IN}/C_F\right) \text{ or} \]

\[\left(8 \cdot k/q\right) \cdot \ln(N) \cdot \left(C_{IN}/C_F\right) \text{ V/degree.}\]

III. CURRENT RATIO

There is a degree of freedom in the choice of current ratio and capacitor ratio for a given sensor sensitivity. The output is to be measured by a 10-bit ADC using a 2.5-V reference voltage, and should have a resolution of 0.25 °C per LSB or four LSB’s, \((4) \cdot \left[\frac{2.5}{1024}\right]\) per degree. The resulting expression for capacitor ratio may be calculated as follows:

\[(8 \cdot k/q) \cdot \ln(N) \cdot \left(C_{IN}/C_F\right) = (4) \cdot \left[\frac{2.5}{1024}\right]\]

giving

\[C_{IN}/C_F = \left[\frac{(1.25) \cdot (q)}{(4) \cdot \left(1024\right) \cdot (k) \cdot \ln(N)}\right].\]

Using the values for \(k\) and \(q\) stored in our SPICE simulator, for \(N = 8\), this gives \(C_{IN}/C_F = 6.812443\), difficult to manufacture accurately. A search for a better ratio leads to the discovery that with \(N = 17\), the capacitor ratio is exactly 5.000003, less than 1 ppm from an integer number that is easy to lay out and manufacture with good repeatability. A value of 10 pF is chosen for \(C_{IN}\) based on \(kT/C\) noise considerations. After SPICE optimization, the currents are chosen as 2 and 34 \(\mu\)A as a compromise among speed, power, noise and accuracy.

IV. CURRENT SOURCES

The 17:1 ratioed current sources are made using an array of unit PMOS devices laid out with the same care and techniques used for 8- and 10-bit current–source DAC’s, with a full ring of dummy devices. Thus, the matching data on such structures can be predicted, and are well within the requirements of the temperature sensor as verified in simulations. For this reason, current-copier techniques were not considered necessary. Also, as shown in Fig. 5, a different unit PMOS device is selected for each of the four switching phases, thus averaging the error in the current–source ratio. MP1 is chosen as the unit for the first \(\delta V_{BE}\) sample, then MP2, and so on. The four unit devices are in the center of the current source array, surrounded by the rest.

V. OFFSET

With the values chosen of \(N\) and \(C_{IN}/C_F\), the sensor output is in volts per kelvin. To convert this to volts per degree Celsius, an offset must be subtracted to center the output within the range of the ADC for the required temperature range of \(-55\) °C to \(125\) °C. This offset is chosen such that at ambient temperature, 25 °C, the ADC output is at midscale, 1.25 V, resulting in code 192 at \(-55\) °C and 912 at \(125\) °C. Code 0 occurs at \(-103\) °C and full scale at 152.75 °C. This is done by adding capacitors \(C_7\) and \(C_8\), switches \(S_{10}\) and \(S_{14}\), and using an offset voltage \(V_{OFF}\), tapped from the ADC reference. This offset voltage is adjusted at probe by poly fuse trimming to give the correct digital output at the measured chuck temperature. The scale factor must be good by design as calibration at multiple temperatures is too expensive.

VI. AMPLIFIER

Fig. 6 shows a schematic of the amplifier used in the sensor. Two gain stages are used which allow for the chopping switches at the amplifier inputs and between the first and second stages. Continuous-time common-mode feedback is used through \(C_{CM1}\) and \(C_{CM2}\). The associated switches MN9 and MN11 are on in auto-zero, reducing the gain to that of the
first stage only, which is high enough at 60 dB for the offset cancellation to be effective.

**VII. SIMULATION**

Fig. 7 shows a transient analysis of the complete sensor at −55 °C, 25 °C, and 125 °C. The settling time allowed for each sample is 4 µs. The sensor o/p is sampled at 18 µs by the ADC, and produces a digital result in 25 µs. The error predicted in simulation is approximately 2° at room temperature due mainly to the SPICE term VAR, the reverse Early voltage of the p-n-p’s. This is removed in the final circuit by a small change in $V_{OFF}$ and a tweak in the capacitor ratio. The resulting nonlinearity versus temperature in simulation is less than 0.1 °C.

**VIII. ADC REFERENCE**

Another source of error in a temperature-to-digital converter is the temperature coefficient of the reference voltage used in the ADC. Operation with a precision 2.5-V external reference is enabled by the comparator in Fig. 1, which detects its
presence and shuts down the internal reference circuitry. Grounding the REFIN pin enables internal reference operation. Continuous-time CMOS bandgap references suffer greatly from amplifier offset voltage and $1/f$ noise. Even with isolated bipolar devices available for the amplifier, there remains the mismatch of the devices in the PTAT core which can result in hysteresis effects after temperature cycling. A solution has been proposed [3], [4] where a stable reference voltage is not required at all times—as is the case in an ADC—where a single bipolar device is used at switched currents as in the temperature sensor. Fig. 8 shows the circuit used where, again, two $\delta V_{BE}$ signals are generated and added to the $V_{BE}$ of one of the p-n-p’s. The circuit has two operating modes. In auto-zero, the output is at $V_{BE}+V_{CE}$ and the current in $Q_5$ is $I$. When the circuit switches to valid-reference mode, the offset is stored on $C_F$, and the current in $Q_5$ switches to $N(I)$ while the current in $Q_6$ switches to $I$, causing two $\delta V_{BE}$ signals to be summed on $C_{TN}$ and bringing the output to the desired bandgap voltage. A further amplifier is used to raise the voltage to 2.5 V. An array of $5 \times 5$ PMOS current sources is used, giving $N = 24$.

IX. RESULTS

The four-channel ADC plus temperature-to-digital converter is fabricated on 0.6-μm DPDM CMOS with a die area of 1.62 mm $\times$ 2.05 mm. The die area of the sensor alone is 0.7 mm $\times$
0.35 mm, dominated by the two 10-pF poly–poly capacitors. In
the die photo of Fig. 10, the sensor occupies the bottom right
and the reference is on the bottom left. The supply voltage
is 2.7–5.5 V, with a supply current of 1 mA with external
reference and 1.25 mA when the internal reference is enabled.
The ADC achieves 61 dB SNR and 76 dB THD when sampling
the voltage input channels at 100 ksamples/s. The conversion
time when measuring the temperature is increased to 25 μs.
At wafer probe, the pretrim error of the temperature sensor is
centered at +3 °C, with all devices contained within ±1 °C to
+5 °C. This mean value may be adjusted to zero with a small
mask change. Posttrim, all are within ±0.5 °C. The variation in
sensor error over temperature is shown in Fig. 9, and is within
±1 °C from −55 °C to 125 °C using external reference. Units
have been tested up to ADC full scale at 152 °C, and remain
within 1 °C. With internal reference operation, the bandgap
curvature shows at high temperature, but the error band is still
within ±1 °C.

When the part is run in auto-shutdown mode the supply
current is reduced to approximately 0.2 μA, the drain current
of one weak PMOS device in the power-on reset circuit. When
asked for a conversion, the part powers up to full supply
current in 2 μs, performs a conversion on temperature in 25
μs, and then goes back to sleep. The resulting average power
dissipation depends on the conversion rate, and is measured at
1 μW at 3 V and 10 conversions/s.

ACKNOWLEDGMENT

The author would like to thank all members of the project
team at Analog Devices B.V. who contributed to this develop-
ment, including N. McNamara, M. Jennings, L. McHugh, A.
Collins, J. Grubb, B. Cawley, and T. Corbett, in particular
for overcoming the difficult task of measuring temperature
accurately in a production environment at probe and final test.

REFERENCES

with digital output,” IEEE J. Solid-State Circuits, vol. 31, pp. 933–937,
July 1996.
interface for thermocouples with reference junction compensation,”