AN IMPROVED CURRENT-MODE CMOS VOLTAGE REFERENCE

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ABSTRACT

An improved current-mode CMOS voltage reference derives its temperature independent characteristic from two temperature dependent currents which are summed together into a resistor to generate the reference voltage. A CMOS proportional to absolute temperature (PTAT) current generator using substrate bipolar transistors creates the current that increases with temperature. A CMOS threshold voltage extractor circuit creates the conversely proportional to absolute temperature (CTAT) current that decreases with increasing temperature. The reference operates over a temperature range of 0 to 100°C with a power supply voltage between 3.3 and 7 V. Simulations show that over these conditions, the output voltage varies by less than 1% over the specified temperature range while using less than 75 μA of current.

I. INTRODUCTION

An ideal voltage reference provides a constant output voltage independent of temperature, power supply voltage, and other operating conditions. Voltage references can be found in a wide range of applications, including linear and switching regulators, A/D and D/A converters, voltage-to-frequency converters, power supply supervisory circuits, and other circuits requiring a precision reference voltage [1]. As the industry trend toward less expensive, basic CMOS processes continues, IC designers are challenged with designing circuits that perform equally as well as their bipolar predecessors. Many variations of bandgap references utilize the temperature dependence of the base-emitter junction voltage (V_{BE}) of bipolar transistors. The Brokaw bandgap cell, for example, is a widely used bipolar reference [2]. The voltage reference described in this paper achieves performance comparable to bandgap references using a circuit that can be fabricated in a standard CMOS technology.

The reference uses a current-mode topology. Two currents are generated, one proportional to absolute temperature (PTAT) and the second conversely proportional to absolute temperature (CTAT). The two currents are scaled so that the linear components of the two temperature coefficients are equal in magnitude, but opposite in sign. The currents are then summed into a resistor to create a first-order voltage reference. Figures 1 and 2 describe this graphically.

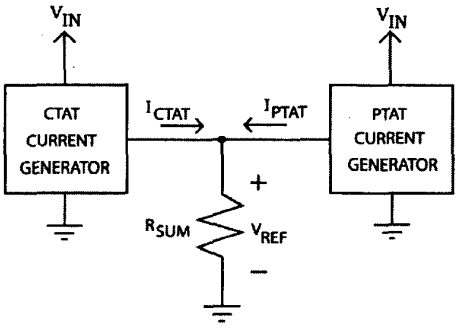

Figure 1. Temperature dependent currents summed into a resistor.

In Figure 2(a), the PTAT and CTAT currents have temperature coefficients of +7 nA/°C and −7 nA/°C, respectively. Figure 2(b) shows the resulting reference voltage when these currents are summed into an 80 kΩ resistor. The sum of the two currents is not entirely independent of temperature. Every first-order voltage reference exhibits this characteristic, which is due to the fact that both the PTAT and CTAT circuits have smaller nonlinear temperature dependencies. Techniques for designing second- and third-order curvature corrected references exist, but these references are considerably more difficult to trim and to test.

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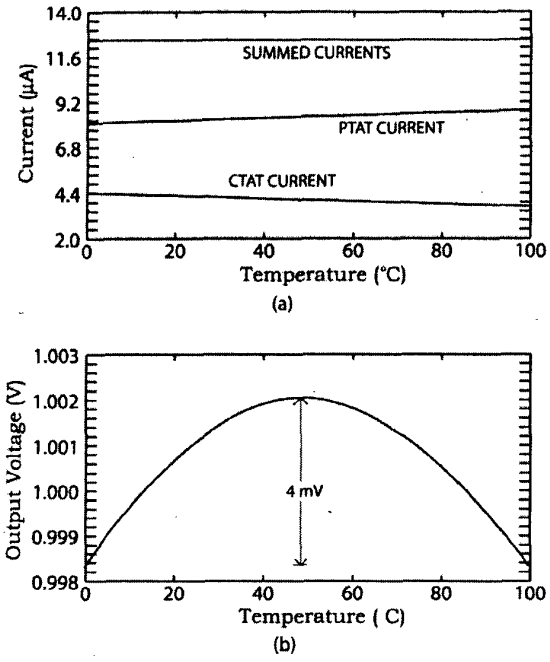

Figure 2. (a) PTAT and CTAT currents, and the sum of the two, (b) Output Voltage vs. Temperature for a typical first-order reference.

II. CIRCUIT DESIGN

A. PTAT Generator

A PTAT current generator similar to the one in [3] is used with the inclusion of cascoded current mirrors to improve line regulation and power supply rejection (PSR). Modifications to the aspect ratios of the MOSFETs are required to allow enough headroom for operation at 3.3 V. The modified circuit is shown in Figure 3.

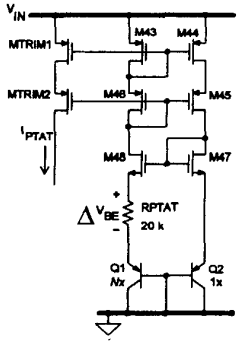

Figure 3. A CMOS PTAT current generator with cascoded p-channel MOSFET current mirrors.

Diode-connected substrate pnp BJTs are used to create the bandgap of silicon voltage dependence. MOSFETs M_{45} through M_{48} form a feedback loop forcing the sources of the n-channel FETs to be at equal potentials [4]. The voltage across resistor R_{PTAT}, ΔV_{BE}, can be found by solving the loop equation,

$$\Delta V_{BE} + V_{EB1} = V_{EB2}, \qquad (1)$$

which reduces to

$$\Delta V_{BE} = \frac{kT}{q} \cdot \ln(N), \qquad (2)$$

where k is Boltzman's constant, q is the charge of an electron, T is absolute temperature, and N is the emitter area ratio of Q_1 to Q_2. The current through resistor R_{PTAT} is simply $\Delta V_{BE}/R_{PTAT}$. Therefore, the generated PTAT current is mirrored to M_{TRIM} and with proper matching must be

$$I_{PTAT} = T \cdot \frac{(W/L)_{TRIM}}{(W/L)_{46}} \cdot \frac{k}{qR_{PTAT}} \cdot \ln(N), \qquad (3)$$

which is proportional to absolute temperature, T.

The start-up circuit provides an initial transient current into the drain of M_{47} during power-up causing the PTAT generator to settle in the correct state and to be self-biasing.

B. CTAT Generator

The left side of the CTAT current generator, the "V_{tp} extractor" [5], shown in Figure 4, is unchanged from [3] except for device geometries which were condensed to reduce chip area and power consumption.

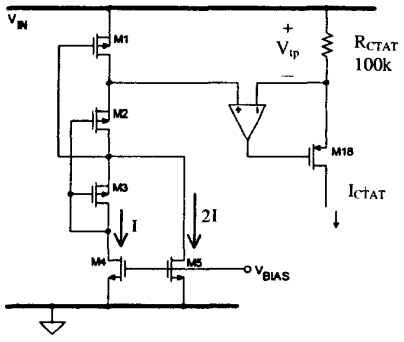

Figure 4. CTAT current generator.

The extracted PMOS threshold voltage is buffered and applied across R_{CTAT} to create the CTAT current,

$$I_{CTAT} = \frac{V_{tp}}{R_{CTAT}} . \quad (4)$$

In testing the voltage reference of [3] over temperature, oscillations sometimes occur; this is attributed to phase margin headroom in the buffer amplifier. The new amplifier, shown in Figure 5, includes a nulling resistor implemented with a p-channel FET in series with the compensation capacitor to cancel the effect of the drop in phase due to the second pole [6]. Different MOSFET aspect ratios and the addition of the nulling resistor increase the open-loop DC gain and more than doubles the phase margin to approximately 85°, respectively, in the new amplifier. These improvements to the two stage open-loop amplifier prevent oscillations at the output when the temperature changes and improve the rejection of AC voltages at the input.

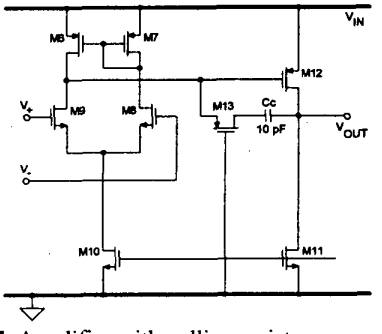

Figure 5. Amplifier with nulling resistor.

C. PTAT Trim Network

A 6-bit binary weighted trim network is used to allow for fine adjustments to the amount of PTAT current that flows into the summing resistor; this is represented above in Figure 3 by a single cascoded transistor pair, M_{TRIM1} and M_{TRIM2}. The trim network enables centering of the reference voltage verse temperature curve for minimal variation. Thus, the trim network lessens the problem of the temperature dependence of V_{tp} on processing variations.

Figure 6 illustrates how the trim range is positioned for increased utilization of adjustment. The trim resolution is also increased by changing the ratio of mirrored FETs in the trim network to mirroring FETs in the PTAT current generator. A least significant bit (LSB) voltage, V_{LSB}, of 2 mV now allows a trim resolution of approximately 8°C/LSB. Shown in Figure 7, the redesigned trim network includes a branch of MOSFETs that are always ON. These transistors, M_{19}, M_{26}, and M_{33}, allow the trim range to be offset in order to better position the range for more usability.

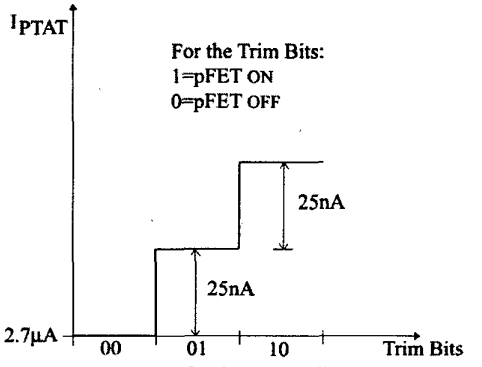

Figure 6. Illustration of "always ON" PTAT current and the effect of the trim bits.

D. Biasing Improvement

Ideally, variations at the output of the voltage reference should not affect the reference voltage. Therefore, the CTAT generator is now biased from the PTAT generator instead of from the output. Small variations in PTAT current negligibly affect the mirrored bias currents to the CTAT current generator. A "gate bias branch", shown in Figure 7 sets the gate voltage of the n-channel MOSFETs that supply current to the "V_{tp} extractor" and the buffer amplifier.

The final expression for the output voltage is

$$V_{REF} = (I_{PTAT} + I_{IPTAT})R_{SUM} = \frac{R_{SUM}}{R_{PTAT}} \cdot \frac{kT}{q} \cdot \ln(N) \cdot \left(1 + \frac{1}{64} \sum_{i=0}^{5} 2^i b_i \right) + \frac{R_{SUM}}{R_{IPTAT}} \cdot V_{tp} \quad (5)$$

where b_i is the ith trim bit. $b_i = 0$ if the mirror is OFF, and 1 if the mirror is ON. Note that the resistors only appear as ratios in the final equation for the output voltage. Therefore, the temperature coefficients of the matched resistors approximately cancel, and do not affect the temperature coefficient of the output voltage [7]. Low sheet resistance (LSR) polysilicon resistors are used throughout to obtain good matching [8].

32X 16X 8X 4X 2X 1X

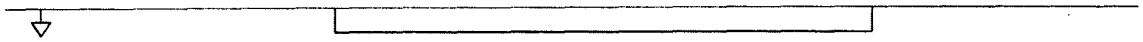

Figure 7. The complete voltage reference circuit.

III. SIMULATION RESULTS

Figure 8 shows the output voltage verse temperature for the optimum trim setting.

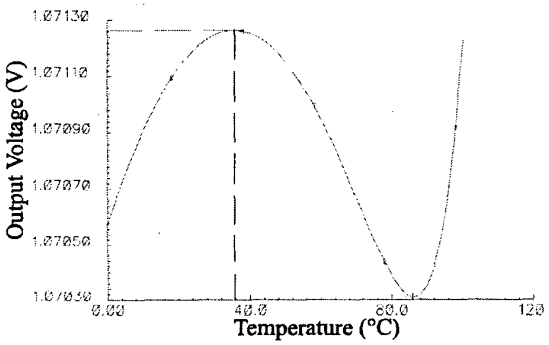

Figure 8. Reference Output Voltage vs. Temperature.

At this setting the temperature drift is ±0.5 mV and the temperature coefficient (TC) is 9.3 ppm/°C. A comparison of simulated performance between the design presented in [3] and the design presented in this paper is shown in Table 1.

The circuit modifications and redesign to [3] improved the voltage reference performance in every category except power consumption. There was approximately a factor of four improvement in temperature drift and in temperature coefficient. The line regulation improved by a factor of 25. The 13 dB improvement in PSR(1 kHz) also represents an improvement of approximately a factor of 4.

Parameter	Design 1	New Design
V_{REF} (25°C, V_{IN} = 5 V)	1.085 V	1.071 V
Temperature Drift (0-100°C, V_{IN} = 5 V)	±2 mV	±0.5 mV
TC	36 ppm/°C	9.3 ppm/°C
Line Regulation (3.3-7 V)	18.9 mV/V	778 µV/V
PSR (1 kHz)	36.4 dB	49.4 dB
Chip Area	0.913 mm^2	0.609 mm^2
Supply Current (V_{IN} = 5 V)	40 µA	73.6 µA

Table 1. Performance Comparison.

IV. EXPERIMENTAL RESULTS

The voltage reference was fabricated through the MOSIS service in the AMI 1.5 micron ABN CMOS process. The measured output voltage variation with temperature is shown in Figure 9, note that maximum PTAT current is active. Because no more PTAT current is available, the output temperature drift cannot be minimized for this particular fabricated chip.

The other measured parameters, which do not depend on trimming, show a great improvement over the initial design in [3]. Table 2 shows a comparison between simulated results and measured data.

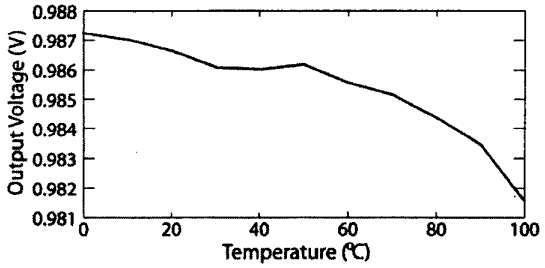

Figure 9. Measured Output Voltage vs. Temperature with maximum PTAT current.

Parameter	Simulation	Measured
V_{REF} (25°C, V_{IN} = 5 V)	1.071 V	0.986 V
Temperature Drift (0-100°C, V_{IN} = 5 V)	±0.5 mV	±2.8 mV
TC	9.3 ppm/°C	57 ppm/°C
Line Regulation (3.3-7 V)	778 µV/V	6.2 mV/V
PSR (1 kHz)	49.4 dB	43.2 dB
Supply Current (V_{IN} = 5 V)	73.6 µA	89.0 µA

Table 2. New design comparison.

V. CONCLUSIONS

Overall, the new design proves to exhibit many improvements with only the compromise of larger supply current requirements due primarily to the different W/L ratios between the trim network and the PTAT current generator.

The biggest challenge with the design of this circuit is setting the trim resolution and offset PTAT current to obtain maximum performance. The "always ON" branch in the trim network which supplies the offset current must be set so that variation of the p-channel MOSFET threshold voltage will not inhibit trimming to obtain minimum temperature drift. Comparison of the simulation results and experimental results show the problems with the process dependence of the p-channel MOSFET threshold voltage, both its nominal value and its temperature coefficient.

Similar to many available voltage references, the improved design could be packaged in a SOT-23. The circuit could also be scaled down and used inside another integrated circuit. Constraints such as channel length modulation and good transistor matching would have to be taken into account in order to maintain performance.

References

[1] Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw-Hill, 1998.

[2] A. P. Brokaw, "A Simple Three Terminal IC Bandgap Reference," IEEE J. Solid State Circuits, vol. s.c. 9, pp. 388-393, Dec. 1974.

[3] Richard Stair, J. Alvin Connelly, and Mark Pulkin, "A Current Mode CMOS Voltage Reference," *2000 Southwest Symposium on Mixed-Signal Design*, pp. 23-26, 2000.

[4] W. T. Holman, "A Low Noise CMOS Voltage Reference," pg. 34, Georgia Institute of Technology, Ph.D. Thesis, August 1994.

[5] I.M. Filanovsky, "Two Temperature Sensors Realized in BiCMOS Technology," ISCAS 1998.

[6] Randall L. Geiger, Phillip E. Allen, and Noel R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill, 1990.

[7] G. A. Rincon-Mora, "Current Efficient, Low Voltage, Low Dropout Regulators," pg. 81, Georgia Institute of Technology, Ph.D. Thesis, November 1996.

[8] Alan Hastings, *The Art of Analog Layout*, Prentice Hall, 2001.