A Detailed Analysis of Power-Supply Noise Attenuation in Bandgap Voltage References

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***Abstract*—This paper discusses the power-supply noise attenuation (PSNA) in the frequency domain of four kinds of bandgap voltage reference that represent the basis of typical voltage references. This performance parameter becomes a fundamental design criterion in high-frequency applications where, due to the reduction in the loop gain, spurious signals coming from the power supply cannot be adequately rejected. Precise and simple models, useful for pencil and paper analysis are hereby developed for the four analyzed topologies and, where possible, compensation techniques are discussed. Moreover, the four topologies are compared in detail highlighting both their main features and drawbacks.**

***Index Terms*—Bandgap voltage reference, circuit analysis, CMOS analog integrated circuits, frequency-domain analysis, power-supply noise attenuation.**

I. Introduction

BANDGAP voltage references have been extensively used in a wide range of applications such as A/D and D/A converters, voltage regulators, measurements and instrumentation circuits, memories, etc. [1]–[5]. The bandgap reference generates a dc voltage that is ideally independent of temperature. This is achieved by adding a voltage, which is proportional to the absolute temperature (PTAT), to a base–emitter voltage in order to compensate for its first-order temperature dependency [4], [5].

In the literature, the performance of bandgap references has been expressed in terms of relative temperature dependency and other characteristics such as accuracy [9]–[18], power consumption [15]–[24], and noise [25]. However, an important parameter, such as power-supply noise attenuation (PSNA), has not yet been analyzed explicitly in terms of its frequency behavior [22], [26], [27]. This is despite the fact that in high-frequency applications, this performance parameter becomes a fundamental design criterion. Indeed, due to the reduction in the loop gain with frequency, spurious signals coming from the power supply cannot be adequately rejected and this problem becomes more prominent in RF or digital environments where disturbances due to cross talk or to substrate noise arise [28]–[31]. In these environments, a detailed knowledge of bandgap frequency behavior is fundamental in affording the designer a better understanding of the possibilities and main limitations of the adopted voltage reference [32], [33].

In this paper, we focus our attention on four main topologies of bandgap voltage references because they represent the basis for typical structures. The circuits examined are shown in Figs. 1–4 and are referred to as Type A, B, C, and D, respectively. In the following, the gain (or better, the attenuation) between the power supply and the output is analyzed in the frequency domain. Specifically, Sections II–V will briefly describe the large signal equations that govern the voltage references, describe an equivalent small-signal model and analyze PSNA behavior in the frequency domain for Types A, B, C, and D, respectively. Moreover, where possible, comments on those compensation techniques that improve the PSNA will be also

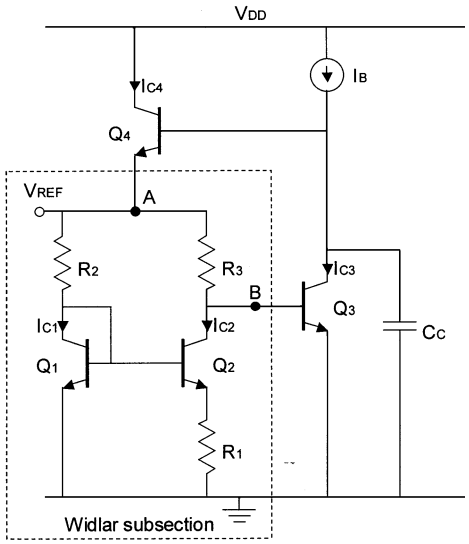

Fig. 1. Type A voltage reference.

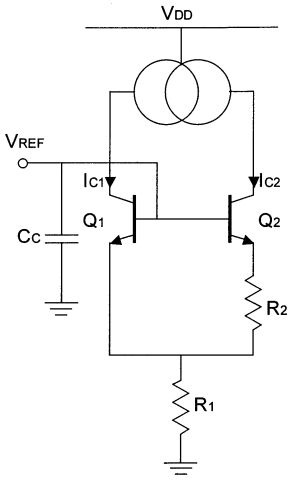

Fig. 2. Type B voltage reference.

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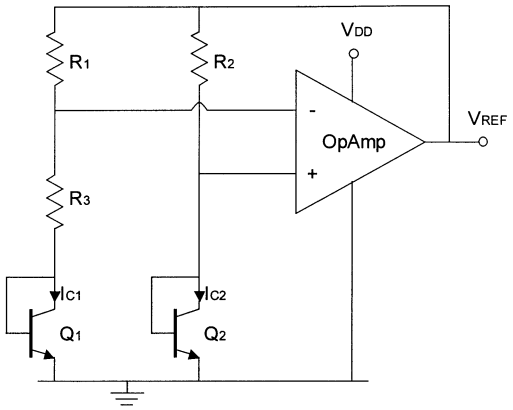

Fig. 3. Type C voltage reference.

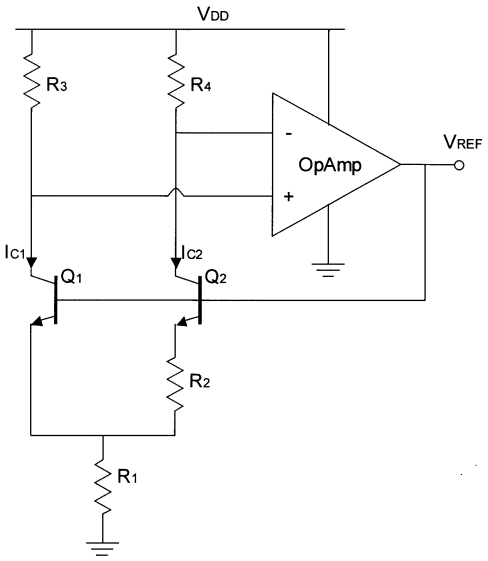

Fig. 4. Type D voltage reference.

given and discussed. Section VI validates the results by comparing the PSNA of the four voltage references with their respective models derived from the previous sections. Finally, in Section VII some remarks are reported and conclusions drawn.

II. Analysis of Type A Voltage Reference

The circuit in Fig. 1 is designed so that current I_{C1} is equal to I_B [6], [13]. This is done by setting R_2 properly, because its voltage drop is about 1.26 V minus a base–emitter voltage. Inspecting the Widlar current mirror the current I_{C2} results in

$$I_{C2} = \frac{V_T}{R_1} \ln\left(\frac{A_{E2}}{A_{E1}} \frac{I_{C1}}{I_{C2}}\right) \tag{1}$$

where A_{E1} and A_{E2} are the emitter area of transistors Q_1 and Q_2, respectively, and V_T is the thermal voltage. Since the voltage drop across R_3 is the same as R_2 ($V_{BE3} = V_{BE1}$), the current ratio I_{C1}/I_{C2} is equal to R_3/R_2. Substituting this value in (1) and considering that $V_{\rm REF}$ is equal to $V_{BE3} + I_{C2}R_3$ we obtain the output of the voltage reference as follows:

$$V_{\rm REF} = V_{BE3} + \frac{R_3}{R_1} V_T \ln\left(\frac{A_{E2}}{A_{E1}} \frac{R_3}{R_2}\right). \tag{2}$$

A. Small-Signal Model and Analysis

To find a small-signal model that will closely approximate the circuit in Fig. 1, we analyze the Widlar subsection shown in the same figure. In the process, we separate this circuit from the rest of the bandgap and apply the voltage source v_s to node *A* and connect a load resistor equal to $r_{\pi 3}$ to node *B* to account for the loading effect of transistor Q_3. Defining the current flowing across the generator v_s as i_s and the voltage seen at node *B* as v_o, the dc analysis shows that, after simplification, the input resistance and the voltage gain of this subsection can be closely expressed by [32]

$$\frac{v_s}{i_s} \approx R_2 || (R_3 + r_{\pi 3}) \tag{3a}$$

$$\frac{v_o}{v_s} \approx \frac{r_{\pi 3}}{r_{\pi 3} + R_3} \tag{3b}$$

that is, transistors Q_1–Q_2 and resistor R_1 can be neglected in the small-signal model of the Type A circuit. As far as frequency behavior is concerned, it can be seen that only the collector-substrate capacitance of Q_2, namely C_{cs2}, has to be taken into account. In fact, not only is this capacitor larger compared to the others (generally the emitter area of Q_2 is eight times the size of the emitter areas of Q_1 and Q_3) but it is also the only one connected to a relatively high impedance node. Hence, an accurate small-signal model for a Type A voltage reference can be derived as illustrated in Fig. 5.

The current reference I_B is modeled by means of resistor R_B and capacitor C_B, which are responsible for an additional path from the power supply to the output. Moreover, capacitor $C_{\pi 4}$ can be neglected because, as is well known, in a common collector configuration it gives rise to a pole–zero doublet which negligibly contributes to the overall frequency response (both of them are in the order of $g_{m4}/C_{\pi 4}$). Finally, C_C compensates the circuit.[1]

The PSNA of the circuit in Fig. 5 can be assumed to have a two-pole two-zero transfer function expressed by

$$\text{PSNA}(s) = \text{PSNA}(0) \cdot \frac{1 + b_1 s + b_2 s^2}{1 + a_1 s + a_2 s^2} \tag{4}$$

where the dc component and the coefficients are approximately given by

$$\text{PSNA}(0) = \frac{R_3 + r_{\pi 3}}{\beta_{F3}(R_B || \beta_{F4} r_{c4})} \tag{5a}$$

$$b_1 = (R_B || \beta_{F4} r_{c4}) \cdot \left[\frac{C_C}{g_{m4} r_{c4}} + C_B + (C_{cs2} + C_{\pi 3}) \frac{R_3 + r_{\pi 3}}{R_B}\right] \tag{5b}$$

[1]Note that capacitor C_C was used for a dominant-pole compensation of the loop gain. Although a Miller compensation could also be adopted by inserting a capacitor between the base and the collector of Q_3, this does not appear to be a good choice in terms of PSNA. In fact, in the case of dominant-pole compensation, at high frequency, the base of Q_4 is grounded because of capacitor C_C that can be considered as short circuited. Since the emitter of Q_4 (that is voltage $v_{\rm ref}$) follows the base voltage, capacitor C_C stabilizes the output with respect to disturbances coming from the current reference I_B [32].

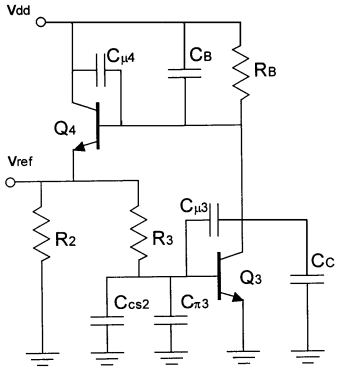

Fig. 5. Small-signal model of the Type A voltage reference.

$$b_2 = (R_B \| \beta_{F4} r_{c4})(R_3 \| r_{\pi 3})(C_{cs2} + C_{\pi 3}) \cdot \left(\frac{C_C}{g_{m4} r_{c4}} + C_B \right) \tag{5c}$$

$$a_1 = C_C \frac{R_3 + r_{\pi 3}}{\beta_{F3}} + R_3 C_{\mu 3} \tag{5d}$$

$$a_2 = \frac{R_3}{g_{m3}} C_C (C_{cs2} + C_{\pi 3} + C_{\mu 3}). \tag{5e}$$

From (5a) we note that the PSNA dc value is mainly limited by the parallel between R_B and the collector resistance, r_{c4}, of transistor Q_4 multiplied by β_{F4}. It is apparent that the implementation of the bias current plays an important role in terms of PSNA. The minimum PSNA dc value is achieved for an ideal bias current (that is $R_B = \infty$) and from (5a) it results equal to $(R_3 + r_{\pi 3})/\beta_{F3}\beta_{F4} r_{c4}$. This value can be assumed as an intrinsic one for the bandgap topology. In actual implementations, I_B is often the output stage of a current mirror that, depending on the technology adopted (bipolar or BiCMOS), can be made in several ways. Better performances in terms of PSNA can be achieved by using a current mirror with an output resistance in the order of $\beta_{F4} r_{c4}$, i.e., by adopting cascode or Wilson topologies. Unfortunately, these circuits require higher power supplies than their simple counterparts so they have to be chosen carefully if a less than 3-V power supply is to be used.

For real and well-spaced zeroes, a fairly good approximation of numerator roots in (4) can be found by evaluating the polynomial coefficient ratios [1], [2], yielding

$$z_1 = -\frac{1}{b_1} \approx -\frac{1}{(R_B \| \beta_{F4} r_{c4}) \left(\frac{C_C}{g_{m4} r_{c4}} + C_B \right)} \tag{6a}$$

$$z_2 = -\frac{b_1}{b_2} \approx -\frac{1}{(R_3 \| r_{\pi 3})(C_{cs2} + C_{\pi 3})} \tag{6b}$$

where approximations hold under the assumption of $R_B \gg (R_3 + r_{\pi 3})$. The same approach can be adopted to evaluate the poles in (4) and results in

$$p_1 = -\frac{1}{a_1} \approx -\frac{g_{m3}}{C_C \left(1 + \frac{R_3}{r_{\pi 3}} \right)} \tag{7a}$$

$$p_2 = -\frac{a_1}{a_2} \approx -\frac{1}{(R_3 \| r_{\pi 3})(C_{cs2} + C_{\pi 3})} \tag{7b}$$

where approximations hold if the contribution of $C_{\mu 3}$ can be considered negligible.

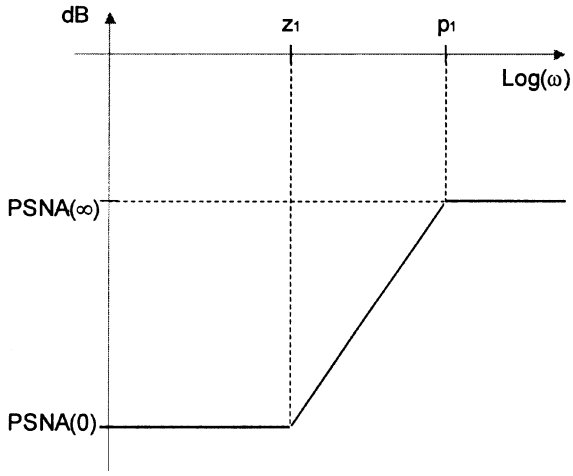

Fig. 6. Frequency behavior of the PSNA(s) in the Type A voltage reference.

Comparing (6) and (7), we note that a pole–zero cancellation is achieved between z_2 and p_2. As a consequence of the above, the PSNA can be approximated by the following transfer function:

$$\text{PSNA}(s) = \frac{R_3 + r_{\pi 3}}{\beta_{F3}(R_B \| \beta_{F4} r_{c4})} \cdot \frac{1 + s(R_B \| \beta_{F4} r_{c4}) \left(\frac{C_C}{g_{m4} r_{c4}} + C_B \right)}{1 + s \frac{C_C}{g_{m3}} \left(1 + \frac{R_3}{r_{\pi 3}} \right)} \tag{8}$$

which is asymptotically depicted in Fig. 6.

Let us study the behavior of (8) with respect to variations in either the bias current or the compensation capacitor. Transistor intrinsic resistances (that is, r_c and r_π in bipolar junction transistors (BJTs) or r_d in MOSFETs) are inversely proportional to bias current. Whether R_B models a MOS or BJT based current reference, we can assume that it is inversely proportional to the bias current, as well. Moreover, even resistor R_3, can be assumed as being inversely proportional to the bias current, because the voltage across its terminals is constant ($V_{R3} = V_{\text{REF}} - V_{BE3}$). Therefore, considering β_{F3} constant with respect to I_B, we note that the PSNA(0) does not change for different values of the bias current. This means that the only way to improve the PSNA(0) is to increase R_B, that is to chose a proper topology for the generator I_B. In contrast, considering that g_m terms are proportional to I_B, analysis of both the pole and the zero shows that both increase linearly with the bias current. Consequently, increasing the bias current means shifting the curve in Fig. 6 to the right or, which is the same, to higher frequencies, thus improving the PSNA.

Increasing the compensation capacitor, C_C, will mainly only affect the pole in (8) because, for typical values, C_B, can be considered dominant with respect to the term $C_C/g_{m4} r_{c4}$. Hence, it will also decrease the value of the PSNA at high frequencies, represented in Fig. 6 as PSNA(∞) and given by

$$\text{PSNA}(\infty) \approx \frac{R_3 + r_{\pi 3}}{\beta_{F3}(R_B \| \beta_{F4} r_{c4})} \cdot \frac{(R_B \| \beta_{F4} r_{c4}) \left(\frac{C_C}{g_{m4} r_{c4}} + C_B \right)}{\frac{C_C}{g_{m3}} \left(1 + \frac{R_3}{r_{\pi 3}} \right)} = \frac{1}{g_{m4} r_{c4}} + \frac{C_B}{C_C}. \tag{9}$$

Increasing C_C would mean decreasing the PSNA(∞) but only until term C_B/C_C becomes similar to $1/g_{m4}r_{c4}$. A good choice of C_C could be to set it so that C_B/C_C equals $1/g_{m4}r_{c4}$. However, considering that $g_{m4}r_{c4} = V_A/V_T$, if the early voltage of Q_4 is in the range 50–100 V, this would mean setting C_C from two to four thousand times capacitor C_B, which could result in too large a value that would prohibitively increase the startup time of the bandgap or would require a considerable amount of area.

III. Analysis of Type B Voltage Reference

Without any loss of generality, assume a PMOS pair, M_3–M_4, to implement the generic current mirror in Fig. 2. This is because in Section VI, we shall validate our analytical results by assuming that the Type B voltage reference can be realized in a BiCMOS technology. Nevertheless, the use of such a current mirror does not introduce any significant changes in the analysis carried out.

The Type B voltage reference sets the output, $V_{\rm REF}$, to $V_{BE1} + 2R_1I_{C1,2}$ [8], [23]. Since $I_{C1,2}$ depends on R_2 and the emitter areas ratio as $I_{C1,2} = (V_T/R_2)\ln(A_{E2}/A_{E1})$, the following relationship holds for the output voltage:

$$V_{\rm REF} = V_{BE1} + 2V_T\frac{R_1}{R_2}\ln\left(\frac{A_{E2}}{A_{E1}}\right). \tag{10}$$

A. Small-Signal Model and Analysis

The simplified small-signal model of the Type B voltage reference is shown in Fig. 7. As mentioned above, the current mirror, which sets I_{C1} and I_{C2} equal, is implemented with a PMOS pair, M_3–M_4, whose main parameters are: a mirror input impedance (modeled with $1/g_{m4}$ and $C_G = 2C_{gs3,4} + C_{db4}$), an output resistance in parallel to a voltage controlled current source (modeled with M_3) and a capacitor that connects the supply line to the output of the mirror (modeled with C_{db3}). Capacitors $C_{\mu 1}$, $C_{\pi 1}$, and $C_{gd3,4}$ are ignored because of their small value and, despite its large value (the emitter area of Q_2 is usually eight times larger than A_{E1}s), capacitor $C_{\pi 2}$ can be ignored as well.[2] Capacitor C_C represents a compensation capacitor. Even if the circuit does not require any compensation, we will see in the following that inserting a capacitor at the output will improve PSNA behavior.

Initially, let us consider capacitor C_C as equal to zero. Neglecting nondominant terms, we can assume the PSNA transfer function to be in the form given by (4), where the dc component and the coefficients are

$$\text{PSNA}(0) = \frac{R_1}{r_{d3}\left\|\left(\frac{k}{2}r_{c2}\right)\right.} \tag{11a}$$

$$b_1 = \left[r_{d3}\left\|\left(\frac{k}{2}r_{c2}\right)\right.\right]\left[2C_{\mu 2} + \left(1+\frac{2}{k}\right)C_{cs2}\right] \tag{11b}$$

$$b_2 = \left[r_{d3}\left\|\left(\frac{k}{2}r_{c2}\right)\right.\right]\frac{C_GC_{\mu 2}}{g_{m3,4}}\left(1+\frac{2}{k}\right) \tag{11c}$$

[2]After applying the Miller theorem to $C_{\pi 2}$ and assuming in rough approximation that Q_2 acts as a voltage follower, its contribution can be demonstrated as being negligible.

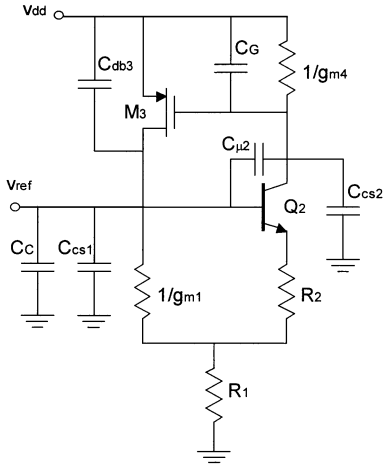

Fig. 7. Small-signal model of the Type B voltage reference.

$$a_1 = \frac{C_G}{g_{m3,4}}\left(1+\frac{1}{k}\right) \tag{11d}$$

$$a_2 = \frac{R_1}{g_{m3,4}}C_G\left[C_{db3} + C_{cs1} + C_{\mu 2}\left(1+\frac{2}{k}\right)\right] \tag{11e}$$

and where k is defined as

$$k = g_{m1,2}R_2 = \ln\left(\frac{A_{E2}}{A_{E1}}\right). \tag{12}$$

A first look at (11a) shows that the PSNA dc behavior mainly depends on process parameters and is independent of the bias current, $I_{C1,2}$. In fact, for the bandgap to work properly, the voltage across R_1 must be kept constant and equal to about 0.5 V, that is R_1 must be chosen almost inversely proportional to $I_{C1,2}$. Moreover, since both r_{d3} and r_{c2} are also inversely proportional to $I_{C1,2}$, for typical technological parameters, a gain of less than -40 dB can hardly be achieved. A slight improvement in the dc gain can be accomplished by using a cascode current mirror instead of the simple mirror M_3–M_4, so that the term $kr_{c2}/2$ dominates in (11a). A further improvement can be obtained by cascading transistor Q_2, as well. However, both solutions require a higher power supply to allow the circuit to work properly.

Poles and zeroes are evaluated by means of the polynomial coefficient ratios

$$z_1 = -\frac{1}{\left[r_{d3}\left\|\left(\frac{k}{2}r_{c2}\right)\right.\right]\left[2C_{\mu 2} + \left(1+\frac{2}{k}\right)C_{cs2}\right]} \tag{13a}$$

$$z_2 = -\frac{g_{m3,4}}{C_G}\left(\frac{2k}{k+2} + \frac{C_{cs2}}{C_{\mu 2}}\right) \tag{13b}$$

$$p_1 = -\frac{g_{m3,4}}{C_G\left(1+\frac{1}{k}\right)} \tag{13c}$$

$$p_2 = -\frac{1+\frac{1}{k}}{R_1\left[C_{db3} + C_{cs1} + C_{\mu 2}\left(1+\frac{2}{k}\right)\right]}. \tag{13d}$$

As far as the ac behavior is concerned, from (13) we note that the first zero, z_1, gives the dominant contribution and depends on both r_{d3} and r_{c2} (as well as the dc gain) and on the parasitic capacitors of Q_2. A pole–zero cancellation is obtained between the second zero, z_2, and the first pole, p_1, because they are very

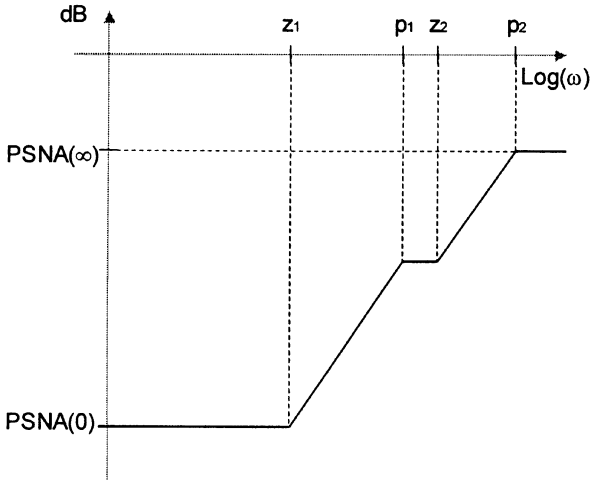

Fig. 8. Frequency behavior of the PSNA(s) in the Type B voltage reference.

close to each other, while the last pole, p_2, makes its contribution at very high frequencies.

Hence, the PSNA can be approximated as

$$\begin{aligned}\text{PSNA}(s) = &\frac{R_1}{r_{d3}\left\|\left(\frac{k}{2}\,r_{c2}\right)\right.} \\ &\cdot \frac{1+s\left[r_{d3}\left\|\left(\frac{k}{2}\,r_{c2}\right)\right.\right]\left[2C_{\mu 2}+\left(1+\frac{2}{k}\right)C_{cs2}\right]}{1+s\,\frac{R_1\left[C_{db3}+C_{cs1}+C_{\mu 2}\left(1+\frac{2}{k}\right)\right]}{1+\frac{1}{k}}} \\ &\cdot \frac{1+s\,\frac{C_G}{g_{m3,\,4}}\cdot\frac{1}{\frac{2k}{k+2}+\frac{C_{cs2}}{C_{\mu 2}}}}{1+s\,\frac{C_G}{g_{m3,\,4}}\left(1+\frac{1}{k}\right)}\end{aligned} \tag{14}$$

whose Bode diagram is qualitatively shown in Fig. 8. Note that this bandgap appears to have poor performance if its first zero is located at low frequencies.

The high-frequency PSNA can be found by means of the ratio between b_2 and a_2. Specifically, dividing (11c) by (11e), we have

$$\begin{aligned}\text{PSNA}(\infty) &\approx \frac{r_{d3}\left\|\left(\frac{k}{2}\,r_{c2}\right)\right.}{R_1}\cdot\frac{C_{\mu 2}\left(1+\frac{2}{k}\right)}{C_{db3}+C_{cs1}+C_{\mu 2}\left(1+\frac{2}{k}\right)} \\ &= \frac{1}{\text{PSNA}(0)}\cdot\frac{1}{\frac{C_{db3}+C_{cs1}}{C_{\mu 2}\left(1+\frac{2}{k}\right)}+1}.\end{aligned} \tag{15}$$

Note that the product of the dc PSNA value and its high-frequency value is almost constant and depends on a parasitic capacitance ratio. The lower the PSNA(0) the higher will be its high-frequency counterpart. Minimizing this constant term means acting on the parasitic capacitor, $C_{\mu 2}$, by adding, for example, a further capacitance in parallel. Unfortunately this would degrade the frequency response by decreasing the first zero and the second pole. Moreover, the final result would yield the above product at most equal to 1.

Even in this case, increasing the current will shift the plot in Fig. 8 to higher frequencies, that is, the value of PSNA(0) does not change while the poles and zeroes increase with the current.

If a compensation capacitor, C_C, is connected between the output node and ground, a better ac performance can be obtained in terms of PSNA. Specifically, assuming C_C to be dominant with respect to other capacitances, coefficients b_1 and b_2 remain unmodified while coefficients a_1 and a_2 turn into

$$a_1 = R_1 C_C\left(1+\frac{1}{k}\right) \tag{16a}$$

$$a_2 = \frac{R_1}{g_{m3,\,4}}\,C_G C_C\left(1+\frac{1}{k}\right). \tag{16b}$$

Consequently, the poles p_1 and p_2 become

$$p_1 = -\frac{1}{R_1 C_C\left(1+\frac{1}{k}\right)} \tag{17a}$$

$$p_2 = -\frac{g_{m3,\,4}}{C_G}. \tag{17b}$$

A pole–zero cancellation can be obtained by choosing C_C so that $p_1 = z_1$, that is

$$C_C = \frac{1}{\text{PSNA}(0)}\cdot\frac{2C_{\mu 2}+C_{cs2}\left(1+\frac{2}{k}\right)}{1+\frac{1}{k}}. \tag{18}$$

In this way, we get a flat-band PSNA over a wide range of frequencies, because the main frequency limitations are given by the pole and the zero in (17b) and (13b), respectively, which are very close each other. A larger value of C_C would lead to a decrease in the PSNA for high frequencies but it would also lead to a prohibitive startup time when the bandgap is switched on.

Choosing C_C as in (18) the frequency behavior of the PSNA becomes

$$\text{PSNA}(s) = \frac{R_1}{r_{d3}\left\|\left(\frac{k}{2}\,r_{c2}\right)\right.}\cdot\frac{1+s\,\frac{C_G}{g_{m3,\,4}}\cdot\frac{1}{\frac{2k}{k+2}+\frac{C_{cs2}}{C_{\mu 2}}}}{1+s\,\frac{C_G}{g_{m3,\,4}}}. \tag{19}$$

The compensation capacitor improves the high-frequency PSNA, too. In fact, in this case the ratio between b_2 and a_2, that is the ratio between (11c) and (16b), becomes

$$\begin{aligned}\text{PSNA}(\infty) &\approx \frac{r_{d3}\left\|\left(\frac{k}{2}\,r_{c2}\right)\right.}{R_1}\cdot\frac{C_{\mu 2}\left(1+\frac{2}{k}\right)}{C_C\left(1+\frac{1}{k}\right)} \\ &= \frac{1}{\text{PSNA}(0)}\cdot\frac{C_{\mu 2}(k+2)}{C_C(k+1)}.\end{aligned} \tag{20}$$

Even in this case, value PSNA(0) plays its role in determining PSNA(∞). However, as shown in (20), increasing C_C means decreasing the high-frequency PSNA.

IV. Analysis of Type C Voltage Reference

The circuit topology shown in Fig. 3 was designed to be fully compatible with CMOS technology [4], [5], [7]. Specifically transistors Q_1 and Q_2 can be easily replaced with diode-connected parasitic p-n-p transistors.

Assuming the circuit to be properly biased, we have voltage V_{REF} set to $V_{BE1} + (R_1 + R_3)I_{C1}$. Considering the virtual ground of the OpAmp, current I_{C1} can be found by inspection and results in $I_{C1} = (V_T/R_3)\ln[(A_{E1}/A_{E2})(I_{C2}/I_{C1})]$. The virtual ground also forces voltage drops across R_1 and R_2 to be equal, that is $I_{C1}/I_{C2} = R_2/R_1$. Consequently, V_{REF} is expressed by

$$V_{\text{REF}} = V_{BE1} + V_T\left(1+\frac{R_1}{R_3}\right)\ln\left(\frac{A_{E1}}{A_{E2}}\,\frac{R_1}{R_2}\right). \tag{21}$$

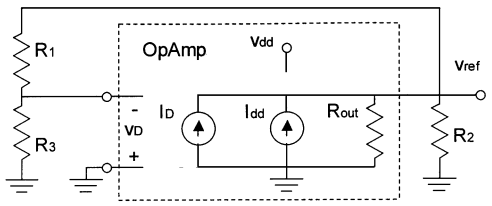

Fig. 9. Small-signal model of the Type C voltage reference.

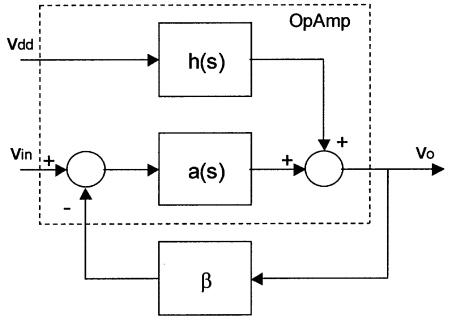

Fig. 10. Block schematic of the Type C bandgap voltage reference.

Generally, transistor Q_1 is equal to Q_2 so that their emitter ratio is unitary and the output voltage mainly depends on resistive ratios.

A. Small-Signal Model and Analysis

The small-signal model of the Type C voltage reference is shown in Fig. 9. Given the small resistance offered by the diode-connected transistors, both Q_1 and Q_2 can be considered as short-circuited, resistor R_2 appears as an OpAmp load and the series partition of R_1–R_3 is fed back the amplifier. The amplifier is modeled with an output resistor, $R_{\rm out}$, and two voltage-controlled current sources (VCCSs), I_D and I_{dd}, driven by the differential voltage of the OpAmp, v_D, and the power supply voltage, v_{dd}, respectively. The first current generator represents the differential gain of the amplifier while the latter represents the gain of the supply line. Both the current generators are expressed in the Laplace domain as $I_D(s)$ and $I_{dd}(s)$. The whole system can be viewed as a feedback amplifier with an input noise in the direct path of the loop as depicted in Fig. 10.

Referring to Fig. 10, the PSNA is evaluated by setting the input $v_{\rm in}$ to zero, and results in PSNA$(s) = h(s)/[1 + \beta a(s)]$. The product $\beta a(s)$ is the loop gain of the circuit, often denoted as $T(s)$, while the term $h(s)$ is the transfer function between the output and the supply line, evaluated when the loop in broken. This suggests that the PSNA can be determined by cutting the loop, and evaluating both $T(s)$ and $h(s)$. Specifically, evaluating the output for v_{dd} grounded yields $T(s)$, while the output evaluated by short circuiting $v_{\rm in}$ yields $h(s)$.

Obviously in this bandgap, the PSNA strongly depends on the OpAmp characteristics, but by taking some general assumptions for the OpAmp, a good analysis can be carried out.

The open-loop gain, for example, can be approximated with a single pole transfer function by assuming that $I_D(s) = G_{MD}v_D/(1 + s/p_a)$ [3]–[5]. Evaluating the open-loop gain yields

$$T(s) = \frac{G_{MD} \cdot [R_{\rm out}||(R_1 + R_3)||R_2]}{1 + \frac{s}{p_a}} \cdot \frac{R_3}{R_1 + R_3}. \quad (22)$$

In a similar manner, the term $h(s)$ can be well approximated by assuming a pole–zero transfer function which models $I_{dd}(s)$, that is, $I_{dd}(s) = G_{Mdd}v_{dd}(1 + s/z_b)/(1 + s/p_b)$ [37], [38], so that

$$h(s) = h_0\frac{1 + \frac{s}{z_b}}{1 + \frac{s}{p_b}} = G_{Mdd} \cdot [R_{\rm out}||(R_1 + R_3)||R_2] \cdot \frac{1 + \frac{s}{z_b}}{1 + \frac{s}{p_b}}. \quad (23)$$

Taking into account (22) and (23), the PSNA(s) results after a few manipulations as

$$\text{PSNA}(s) = \frac{h_0}{1 + T_0} \cdot \frac{1 + \frac{s}{z_b}}{1 + \frac{s}{p_a T_0}} \cdot \frac{1 + \frac{s}{p_a}}{1 + \frac{s}{p_b}}. \quad (24)$$

A first look at (24) shows that, as expected, the PSNA(0) mainly depends on the OpAmp characteristics. Specifically, approximating PSNA(0) to h_0/T_0 and substituting the values found in (22) and (23) we get

$$\text{PSNA}(0) \approx \frac{h_0}{T_0} = \frac{G_{Mdd}}{G_{MD}} \cdot \left(1 + \frac{R_1}{R_3}\right) = \frac{1}{\beta} \cdot \frac{1}{\text{PSRR}(0)} \quad (25)$$

since G_{Mdd}/G_{MD} is proportional to the intrinsic power-supply rejection ratio (PSRR) of the OpAmp [37] and $1 + R_1/R_3$ is the feedback factor of the circuit.

In the frequency domain, the zero of the direct path between the supply line and the output, z_b, makes the main contribution. The second effect is given by the pole–zero doublet which arises from the poles of both the transfer functions $h(s)$ and $T(s)$. This effect is negligible because these two poles can be equal or very close to each other depending on the OpAmp configuration and the compensation technique adopted [37]. Finally, the second main contribution is the pole given by the product of the loop gain and the first pole of the OpAmp, that is the gain–bandwidth product of the amplifier.

V. Analysis of Type D Voltage Reference

As for Type C, the Type D voltage reference in Fig. 4 is based on a differential amplifier. It has a structure similar to Type B, the difference being that the bias currents are set equal by imposing equal voltage drops across both resistors R_3 and R_4 exploiting the virtual ground of the OpAmp [4], [5], [16]. Voltage $V_{\rm REF}$ is expressed in a form similar to (10).

A. Small-Signal Model and Analysis

The circuit can be seen as a feedback circuit composed of two main blocks; the amplifier and a feedback network referred to

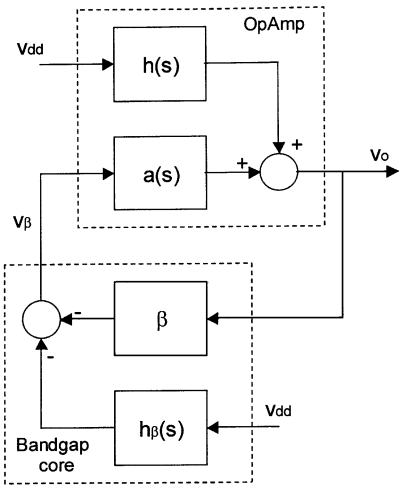

Fig. 11. Block schematic of the Type D bandgap voltage reference.

as the *bandgap core*. From the PSNA point of view, an equivalent schematic block is shown in Fig. 11. Note that v_β is a pure differential signal.

These two blocks can be analyzed separately provided that each one does not load the other or, which is the same, provided that the input resistance offered by both is high.[3]

The OpAmp can be modeled again as in Fig. 9 where $I_D(s)$ and $I_{dd}(s)$ maintain the same expressions as in Section IV-A. Assuming that the bandgap core does not load the OpAmp, for $a(s)$ and $h(s)$ we can write the following:

$$a(s) = \frac{G_{MD} \cdot R_{\text{out}}}{1 + \frac{s}{p_a}} \tag{26a}$$

$$h(s) = G_{Mdd} \cdot R_{\text{out}} \cdot \frac{1 + \frac{s}{z_b}}{1 + \frac{s}{p_b}}. \tag{26b}$$

The feedback gain β is evaluated by analyzing the model in Fig. 12 and, after approximation yields

$$\beta = \left.\frac{v_\beta}{v_s}\right|_{v_{dd}=0} = g_{m1,2} R_{3,4} \frac{R_2/R_1}{2+k} \tag{27}$$

where k is defined in (12). Note that for simplicity we have assumed that the feedback gain is independent of frequency. Simulations in Section VI will confirm this assumption.

The gain $h_\beta(s) = v_\beta / v_{dd}|_{v_s=0}$, strongly affects the PSNA. An approximate symbolic analysis performed on the circuit in Fig. 12 leads to a transfer function with a dc gain

$$h_{\beta 0} = \frac{R_{3,4}}{r_{c1,2}} \frac{R_2/R_1}{2+k} \tag{28a}$$

and a right-half plane (RHP) zero

$$z_\beta = \frac{R_2/R_1}{r_{c1,2}\left[C_{cs2}\left(\frac{R_2}{R_1}+2+k\right) - C_{cs1}(2+k)\right]}. \tag{28b}$$

[3]This can be assumed as being true for the OpAmp. The bandgap core (shown in Fig. 12) can be demonstrated to have an input resistance $R_{\text{in}} \approx \beta_F R_1$ which is large enough not to load the amplifier especially if it is provided with an output stage.

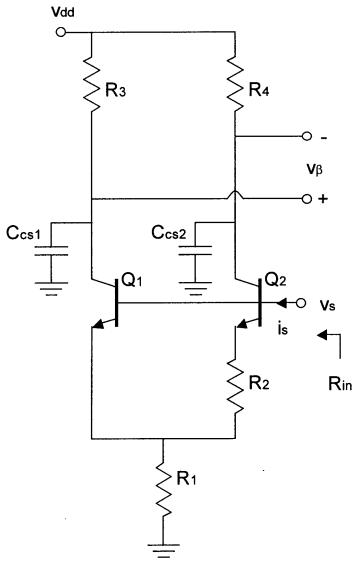

Fig. 12. Small-signal model of the Type D voltage reference bandgap core.

Having already characterized all the blocks in Fig. 11, the PSNA(s) is given by

$$\begin{aligned}\text{PSNA}(s) &= \frac{-h_\beta(s)a(s) + h(s)}{1 + \beta a(s)} \approx -\frac{h_\beta(s)}{\beta} + \frac{h(s)}{\beta a(s)} \\ &= \frac{1}{\beta}\left[\frac{1}{\text{PSRR}(s)} - h_\beta(s)\right]\end{aligned} \tag{29}$$

which means that disturbances coming from the amplifier are greatly attenuated by the loop gain, $\beta a(s)$, while those coming from the bandgap core are transferred to the output divided by the feedback gain, β.

Let us analyze the PSNA substituting $a(s)$, $h(s)$ and $h_\beta(s)$ in (29), that is

$$\begin{aligned}\text{PSNA}(s) &= \frac{-h_{\beta 0}\left(1 - \frac{s}{z_\beta}\right) \cdot \frac{a_0}{1+\frac{s}{p_a}} + h_0 \frac{1+\frac{s}{z_b}}{1+\frac{s}{p_b}}}{1 + \frac{\beta a_0}{1+\frac{s}{p_a}}} \\ &\approx -\frac{h_{\beta 0}a_0 - h_0}{\beta a_0} \cdot \frac{1 - s\,\frac{h_{\beta 0}a_0/z_\beta + h_0/z_b}{h_{\beta 0}a_0 - h_0}}{1 + \frac{s}{p_a \beta a_0}}\end{aligned} \tag{30}$$

where approximation holds considering $p_b = p_a$ (i.e., both the amplifier differential gain and the power supply gain have the same pole[4]). The PSNA(0) can be evaluated by using (29) and, considering (27) and (28a), we get

$$\text{PSNA}(0) \approx -\frac{1}{g_{m1,2} r_{c1,2}} + \frac{1}{\beta}\frac{1}{\text{PSRR}(0)}. \tag{31}$$

Moreover, an RHP zero, which is mainly determined by a linear combination of z_β and z_b, emerges from the feedback, while the gain bandwidth product of the amplifier gives the pole.

VI. Simulation Results

All four bandgaps were designed in a standard 0.8-μm BiCMOS technology. Bipolar n-p-n transistors have a forward current gain, β_F, of 95 and a transition frequency, f_T, of about

[4]This does not pose a strong limitation as it is common for several OpAmp configurations [37].

TABLE I
TYPE A VOLTAGE REFERENCE DESIGN PARAMETERS

Component	*Value*
I_B, I_{C1}	100 μA
I_{C2}	20 μA
A_{E2}/A_{E1}	8
R_1	5.38 kΩ
R_2	5.4 kΩ
R_3	27 kΩ
C_C	10 pF
$r_{\pi 3}$	25.81 kΩ
g_{m3}	3.72 mA/V
g_{m4}	4.31 mA/V
r_{c4}	291.3 kΩ

8 GHz. MOSFET threshold voltages are about 0.75 V for both the complementary transistors, while gain factors, k_n and k_p, are about 100 μA/V^2 and 36 μA/V^2 for NMOS and PMOS, respectively. The four circuits have a 3-V power supply and their power dissipation was maintained in the same order of magnitude thus allowing effective comparison between all the voltage references.

All the simulations were performed with the SPECTRE simulator and technology models supplied by EUROPRACTICE in the Cadence environment.

A. Type A Simulations

The Type A voltage reference was implemented following the schematic in Fig. 1. Design parameters are shown in Table I. The circuit exhibits an output voltage of 1.32 V at room temperature (300 K) with a temperature coefficient (TC) of 20.2 ppm/°C.

Two simulations were performed. The first one by modeling the current generator, I_B, with a 1-MΩ resistor in parallel with a 30-fF capacitor (case A) and the second one by modeling the current generator I_B with a 20-MΩ resistor in parallel with a 60-fF capacitor (case B). In case A, by using (8) with the simulation parameters in Table I, we obtained for the mathematical model a dc gain of −64.9 dB with a zero of 4.34 MHz and a pole of 28.97 MHz. In case B, we got a dc gain of −86.5 dB with a zero of 202.3 kHz and a pole of 29.0 MHz.

Fig. 13 reports the simulated and the expected PSNA behavior for both cases. Specifically, for case A, curves *a* and *b* are the simulated and the expected PSNA, respectively, and so are curves *c* and *d* for case B. It is apparent that the simple first order system described by (8) gives a good approximation of both the circuits in a very simple and useful way.

In both cases, the difference between simulated and expected curves is mainly due to the fact that (8) overestimates the dc PSNA. Specifically, the dc PSNA difference is 2.1 dB and 2.3 dB for case A and B, respectively. A comparison between curves *a* and *b*, normalized with respect their dc value, shows that their difference is below 6 dB. The same difference between curves *c* and *d* is below 4.9 dB.

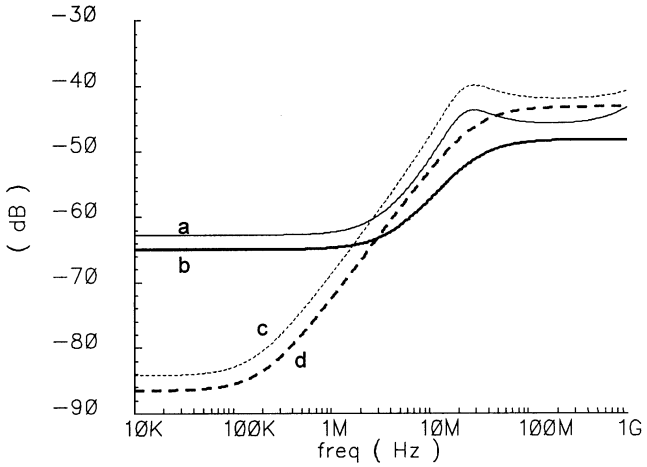

Fig. 13. Simulations of the Type A voltage reference. Case A: Curve *a* simulated PSNA, Curve *b* model. Case B: Curve *c* simulated PSNA, Curve *d* model.

TABLE II
TYPE B VOLTAGE REFERENCE DESIGN PARAMETERS

Component	*Value*
I_{C1}, I_{C2}	100 μA
A_{E2}/A_{E1}	8
R_1	1.93 kΩ
R_2	545 Ω
$(W/L)_{3,4}$	100/4
$g_{m1,2}$	3.80 mA/V
C_{cs1}	29.5 fF
r_{c2}	290.6 kΩ
$C_{\mu 2}$	125.6 fF
C_{cs2}	218.5 fF
$g_{m3,4}$	379.9 μA/V
r_{d3}	669.3 kΩ
$C_{gs3,4}$	558.0 fF
C_{db3}	34.63 fF
C_{db4}	38.02 fF
k	2.08

B. Type B Simulations

The Type B voltage reference was implemented following the schematic in Fig. 2. Since we adopted a BiCMOS technology, the current mirror was made up of a PMOS couple as in Fig. 7. Design parameters are shown in Table II. The circuit exhibits an output voltage of 1.2 V at room temperature (300 K) with a TC of 20.3 ppm/°C.

A first simulation was performed without any compensation capacitor and by modeling the circuit with (14). For the model we obtained a dc gain of −40.6 dB with two zeroes, at 1.12 and 144.6 MHz, and two poles, at 35.38, and 392.3 MHz, respectively. The simulation result is given in curve *a* of Fig. 14 while in curve *b* the model is depicted. The figure shows that the

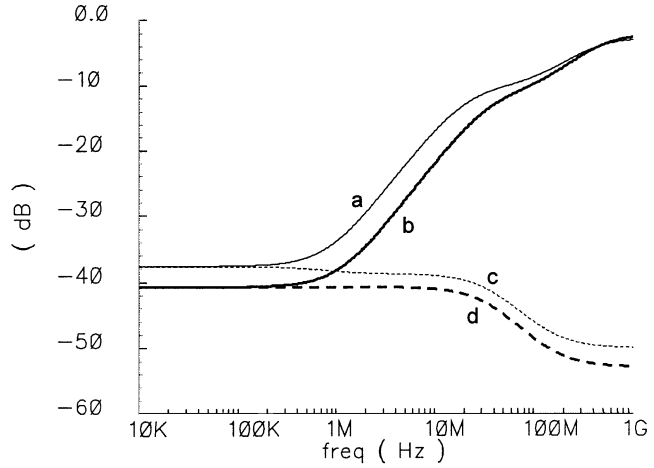

Fig. 14. Simulations of the Type B voltage reference. Without compensation capacitor: Curve *a* simulated PSNA, Curve *b* model. With compensation capacitor: Curve *c*simulated PSNA, Curve *d* model.

model is in a good agreement with the simulated result. Also in this case the main error is due to the difference in the dc PSNA, which is about 3 dB, while the difference between curves *a* and *b*, normalized with respect to their dc value, is below 3.6 dB.

As described in Section II, the "optimum" compensation capacitor value was found using (18), thus yielding a capacitance of 49.4 pF. Equation (19) was adopted to model the circuit. For the model, the dc gain resulted in −40.6 dB, while the pole was at 35.4 MHz and the zero at 144.6 MHz. A second simulation was performed by comparing the "optimally" compensated circuit with the model. The result is shown in Fig. 14 where, curve *c* represents the simulation result and curve *d* represents the model's behavior. As expected, not only is a flat-band response achieved but the model also shows good matching with the real circuit. Specifically, the dc error does not change with respect to the previous simulation, while the difference between the normalized values of curves *c* and *d* is below 1 dB.

C. Type C Simulations

The Type C voltage reference was implemented following the schematic in Fig. 3 and was designed by using the equations in Section IV.

The first simulation was performed by assuming an ideal OpAmp that, without any load, had an intrinsic gain, a_0 $(=G_{MD}R_{\text{out}})$, of 60 dB, an output impedance, R_{out}, of 1 kΩ and a single pole behavior with a transition frequency $(=G_{MD}R_{\text{out}}p_a/2\pi)$ of 10 MHz. Under the same load condition, it was expected to exhibit a power supply gain, h_0 $(=G_{Mdd}R_{\text{out}})$, of −5 dB, a pole, p_b, at 10 kHz and a zero, z_b, at 50 kHz. The amplifier was modeled as in Fig. 9.

The designed voltage reference, whose design parameters are shown in Table III, exhibited an output voltage of 1.19 V at room temperature (300 K) with a TC, of 19.4 ppm/°C.

The bandgap was modeled by (24). Values of T_0 and h_0, to determine dc PSNA and the pole, T_0p_a, were computed by (22) and (23). Note that the determination of *PSNA(0)* could also have been done by means of (25).

The comparison between the simulation result and the mathematical model is shown in Fig. 15, in curves *a* and *b*, respectively. Good agreement is readily apparent. Specifically, a dc error of 1.2 dB is shown while the difference between the normalized values of curves *a* and *b* is maintained below 0.7 dB.

TABLE III
TYPE C VOLTAGE REFERENCE DESIGN PARAMETERS

Component	*Value*
I_{C1}	20 μA
I_{C2}	100 μA
A_{E2}/A_{E1}	1
R_1	21.5 kΩ
R_2	4.3 kΩ
R_3	2.3 kΩ

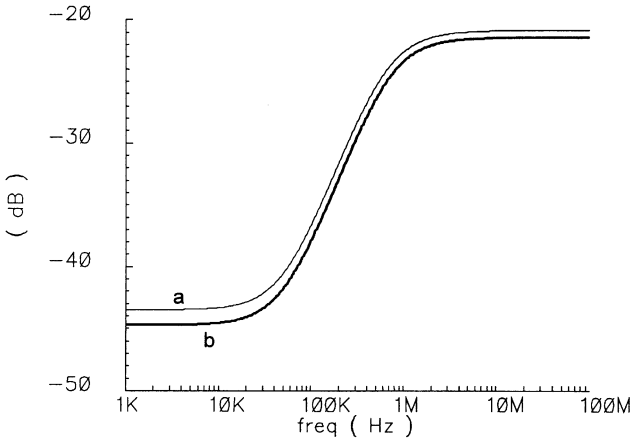

Fig. 15. Simulations of the Type C voltage reference with ideal OpAmp. Curve *a* simulated PSNA, curve *b* model.

A second simulation was carried out by considering the same voltage reference with an OpAmp designed at transistor level. The amplifier is depicted in Fig. 16 and is based on a folded cascode structure. Note that an output stage (i.e., the simple source follower M_{13}–M_{15}) is required to maintain an acceptable dc loop-gain, T_0. Amplifier design parameters are shown in Table IV. In this case, the voltage reference exhibited an output voltage of 1.2 V at room temperature (300 K) with a TC of 23.5 ppm/°C.

Without any load, the amplifier exhibited a dc gain, a_0, of 78 dB and would require a compensation capacitor connected between the gate of M_{15} and ground. However, as shown by (22), the feedback factor β, equal to $R_3/(R_1+R_3)$, lowers the value of T_0 by about 20 dB with respect to a_0, thus compensating the circuit in a natural fashion.

The open-loop gain, $T(s)$, depicted in curve *d* of Fig. 17, exhibits a dc gain of about 58 dB, a unity-gain frequency of 2.02 MHz and a phase margin of 86°.

The magnitude of the transfer function between the output and the supply line, $h(s)$, is depicted in curve *c* of Fig. 17. Note that $h(s)$ exhibits a pole–zero doublet and that its pole is equivalent to the dominant pole of $T(s)$.

Curves *a* and *b* of Fig. 17, represent the simulated PSNA of the voltage reference and the expected PSNA, respectively.

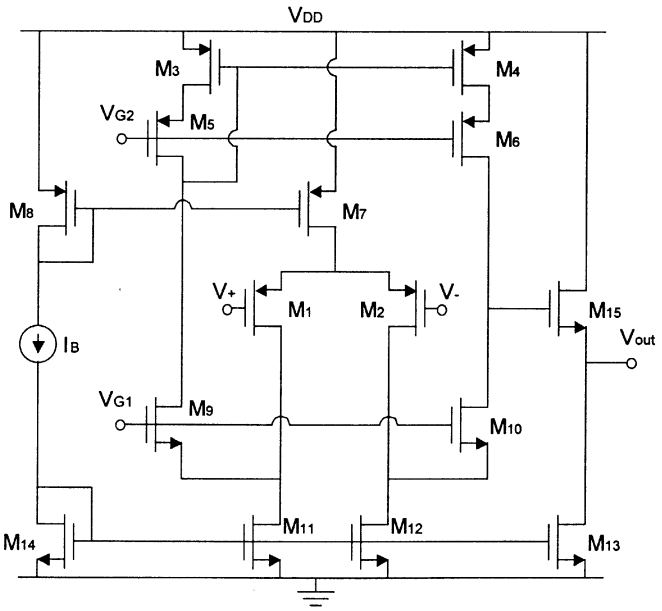

Fig. 16. Schematic of the operational amplifier adopted in the Type C voltage reference.

TABLE IV
OPERATION AMPLIFIERS DESIGN PARAMETERS

Amplifier in Type C		*Amplifier in Type D*	
Component	*Value*	*Component*	*Value*
$M_1 \div M_8$	100/2	$M_1 \div M_9$	50/2
$M_9 \div M_{14}$	50/2	$M_{10} \div M_{14}$	100/2
M_{15}	400/2	M_{15}	200/2
I_B	20 μA	I_B	20 μA
V_{G1}	1.2 V	V_{G1}	1.7 V
V_{G2}	1.8 V	V_{G2}	1.2 V

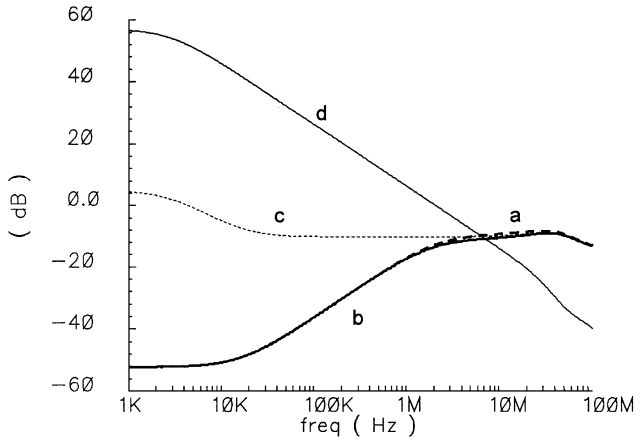

Fig. 17. Simulations of the Type C voltage reference with OpAmp designed at transistor level. Curve *a* Simulated PSNA, curve *b* model, curve *c* $h(s)$, curve *d* $T(s)$.

TABLE V
TYPE D VOLTAGE REFERENCE DESIGN PARAMETERS

Component	*Value*
I_{C1}, I_{C2}	100 μA
A_{E2}/A_{E1}	8
R_1	2 kΩ
R_2	555 Ω
$R_{3,4}$	5 kΩ
$g_{m1,2}$	3.76 mA/V
$r_{c1,2}$	354.2 kΩ
C_{cs1}	24.48 fF
C_{cs2}	196 fF
k	2.09

Specifically, curve *a* was obtained by simulating the PSNA of the circuit in Fig. 3 with the OpAmp in Fig. 16 and curve *b* was obtained by dividing function $h(s)$ by $1+T(s)$ where $h(s)$ and $T(s)$ are depicted in curves *c* and *d*, respectively. The comparison between the two curves shows the excellent agreement between the transistor level circuit and the mathematical model. Note that below the OpAmp unity gain frequency, the PSNA is well approximated by $h(s)/T(s)$ and that over this frequency, that is, when $|T(j\omega)| < 1$, the PSNA can be assumed as being equal to $h(s)$.

D. Type D Simulations

The Type D voltage reference was implemented following the schematic in Fig. 4. Also in this case, a first simulation was carried out using the ideal OpAmp adopted in Section VI-C. Circuit parameters are reported in Table V. The circuit exhibits an output voltage of 1.2 V at room temperature (300 K) with a TC of 18 ppm/°C.

Parameters of the bandgap core were evaluated by using (27) and (28) and resulted in $\beta = 1.27$, $h_{\beta 0} = 956 \cdot 10^{-6}$, and $z_\beta = 2\pi \cdot 165$ krad/s.

The model used to emulate the PSNA behavior of the circuit is given by (30). Specifically, by substituting the above bandgap core parameters and the others reported in Table V in (30) we get for the dc PSNA a value of −79.2 dB. The RHP zero is located at 23.1 kHz, while the pole, $p_a \beta a_0$, is at 12.7 MHz.

Fig. 18 reports the PSNA simulation in curve *a* and the PSNA model in curve *b*. A large error is observed for the dc PSNA. This is due to the fact that when $h_{\beta 0} a_0$ is very close to h_0, as in this case, their difference in (30) may differ from the actual value and lead to an unpredictable PSNA(0). However, since the term $h_{\beta 0} a_0 - h_0$ affects the zero of the PSNA, too, the two curves well match at higher frequencies. When $h_{\beta 0} a_0$ is dominant with respect to h_0 (or vice-versa) the model matches at lower frequencies, too.

A second simulation was carried out by considering a voltage reference with an OpAmp designed at transistor level. Specifically, the amplifier is depicted in Fig. 19 and its design parameters are shown in Table IV. Here, the source follower M_9–M_{15} was inserted to minimize the loading effect of the bandgap core. In addition, a compensation capacitor was required to provide an acceptable phase margin. The voltage reference exhibits an

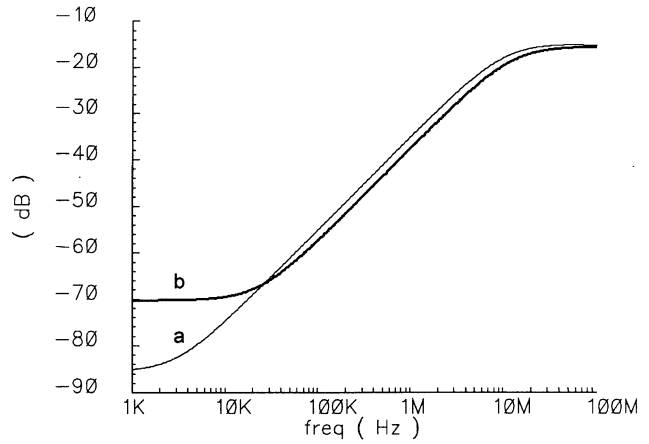

Fig. 18. Simulations of the Type D voltage reference with ideal OpAmp. Curve *a* simulated PSNA, curve *b* model.

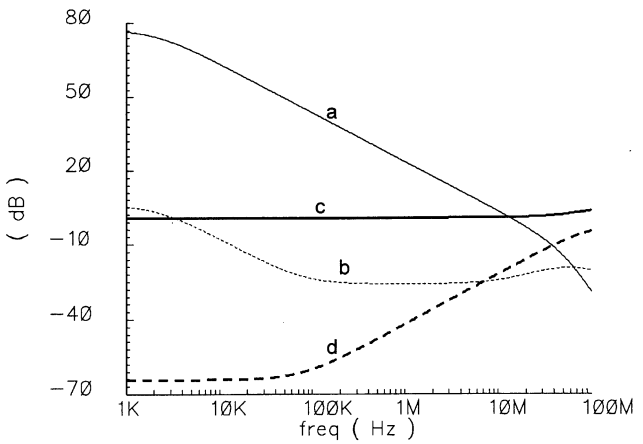

Fig. 20. Block simulations for the Type D voltage reference with real OpAmp. Curve*a* $a(s)$, curve *b* $h(s)$, curve *c* $\beta(s)$, curve *d* $h_\beta(s)$.

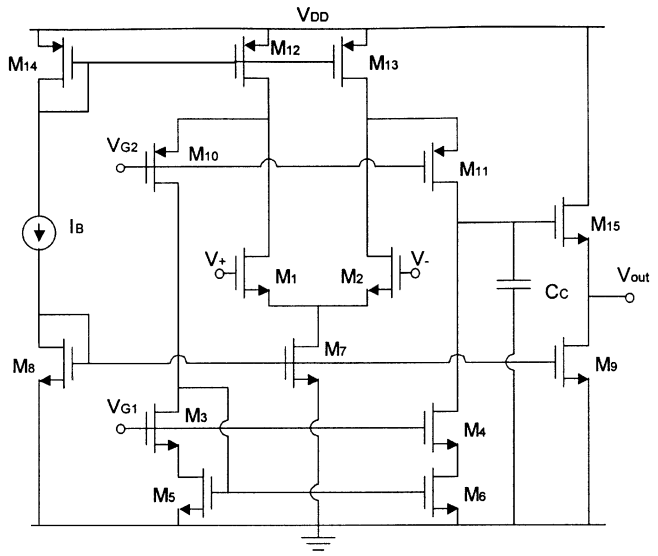

Fig. 19. Schematic of the operational amplifier adopted in the Type D voltage reference.

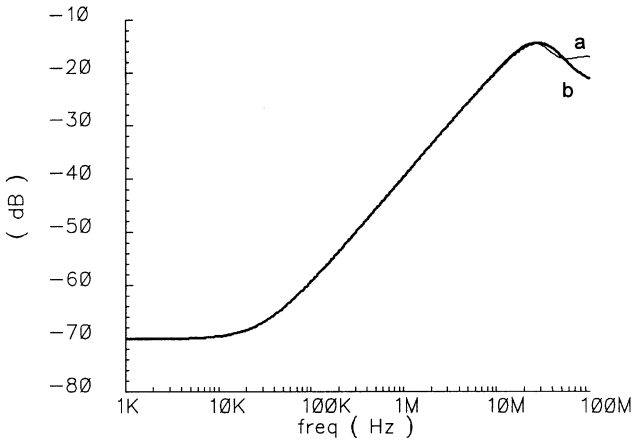

Fig. 21. Simulations of the Type D voltage reference with real OpAmp. Curve *a* simulated PSNA, curve *b* model.

output voltage of 1.21 V at room temperature (300 K) with a TC of 18 ppm/°C.

The magnitude of the amplifier gain is depicted in curve *a* of Fig. 20 and was evaluated by simulating the gain of the circuit in Fig. 19 by applying a differential signal at its input terminals. The amplifier exhibits a dc gain of 77 dB, a unity-gain frequency of 14.4 MHz, and a phase margin of 65°.

The magnitude of the transfer function between the output and the supply line, $h(s)$, is depicted in curve *b* of Fig. 20 and was evaluated by again simulating the amplifier in Fig. 19. Note that also in this case, $h(s)$ exhibits a pole–zero doublet and its pole is equivalent to the dominant pole of $a(s)$. This validates the assumption of modeling $h(s)$ with (26b).

Curves *c* and *d* of Fig. 20, represent core bandgap behavior. Specifically, curve *c* depicts the magnitude of the transfer function v_β/v_s referred to the circuit in Fig. 12 including the capacitive effects given by transistors Q_1 and Q_2. Note that the frequency response is almost flat up to about one decade over the unity-gain bandwidth of the amplifier. This validates the assumption of modeling β by means of a constant value over the frequency range of interest as according to (27). Curve *d* depicts the magnitude of the transfer function v_β/v_{dd}, that is $h_\beta(s)$, referred to the circuit in Fig. 12 comprehensive of the capacitive effects given by transistors Q_1 and Q_2. As in (28b), $h_\beta(s)$ has a single RHP zero.

Fig. 21 compares the PSNA of the actual Type D voltage reference with the model described by (29) when the OpAmp in Fig. 19 is adopted. Specifically, curve *a* depicts the magnitude of the PSNA evaluated by simulating the circuit in Fig. 4. Curve *b* represents the magnitude of the model expressed by (29) where terms $a(s)$, $h(s)$, β and $h_\beta(s)$ were substituted by curves *a–d* in Fig. 20. Clearly, there is excellent agreement between the mathematical model and the transistor level circuit.

VII. Final Remarks and Conclusion

In this paper, the PSNA of four kinds of bandgap voltage references that represent the basis for more modern structures has been analyzed in the frequency domain. This performance becomes of fundamental importance in high-frequency applications where spurious signals coming from the supply line cannot be adequately rejected. To this end some useful models that describe the frequency behavior of the PSNA have been described and, where possible, compensation techniques that improve this

characteristic investigated as well. The four circuits have been exhaustively analyzed and the models developed compared with actual implementations through simulations, showing excellent agreement.

On the basis of the above discussion, the designer can now choose the best bandgap topology for a given application from a number of alternatives.

A first distinction can be made between the first two bandgap voltage references (Types A and B) and the others that use an operational amplifier (Types C and D). Types A and the "optimally compensated" Type B, exhibit good behavior over a wide range of frequencies (up to 1 GHz in our examples). Specifically, both can easily maintain their PSNA below 40–45 dB at high frequencies. Moreover, Type A shows excellent performance at very low frequencies.

In contrast, the PSNA of Types C and D, depends on the OpAmp characteristics and, in the specific, on the PSRR of the OpAmp. At low frequencies, a good PSNA can easily be achieved by increasing the loop gain, especially in Type C given that in Type D the bandgap core plays an important role and its disturbances cannot be attenuated by the loop gain. Nevertheless, both of them present strong limitations at higher frequencies because the loop gain is drastically reduced. In these cases, techniques for reducing the OpAmp PSRR should be adopted as reported in [38].

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