A 10-GB/s SONET-Compliant CMOS Transceiver With Low Crosstalk and Intrinsic Jitter

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***Abstract*—A 4:1 SERDES IC suitable for SONET OC-192 and 10-Gb/s Ethernet is presented. The receiver, which consists of a limiting amplifier, a clock and data recovery unit, and a demultiplexer, locks automatically to all data rates in the range 9.95–10.7 Gb/s. At a bit error rate of less than 10^{-12}, it has a sensitivity of 20 mV. The transmitter comprises a clock multiplying unit and a multiplexer. The jitter of the transmitted data signal is 0.2 ps rms. This is facilitated by a novel notched inductor layout and a special power supply concept, which reduces cross-coupling between the transmitter and receiver. Integrated in a 0.13-μm CMOS technology, the total power consumption from both 1.2- and 2.5-V supplies is less than 1 W.**

***Index Terms*—Clock and data recovery, CMOS integrated circuits, crosstalk, integrated inductors, jitter, OC-192, phase-locked loops, SONET, transceivers, voltage-controlled oscillators.**

I. INTRODUCTION

DEMAND for bandwidth is ever increasing and so is the pressure on cost for communication equipment. This explains the attractiveness of implementing a 10-Gb/s transceiver in a CMOS technology, as opposed to using expensive SiGe or even GaAs processes where 10-Gb/s designs were first known [1]. Additional benefits of CMOS are the higher integration density and the possibility to have large logic blocks on the same chip. Many challenges are posed by the SONET OC-192 requirements on a CMOS design, which has to overcome such drawbacks as slow device speed (low f_t) and large intrinsic device noise. Further, to meet the jitter requirements, good immunity to power supply noise in general and, more specifically, low crosstalk between receiver and transmitter are a prerequisite. These considerations and the need to avoid external components have led to the presented design.

II. 10-Gb/s TRANSCEIVER ARCHITECTURE AND CIRCUIT BLOCKS

The transceiver is composed of the major building blocks shown in Fig. 1. The input signal of the receiver enters the limiting amplifier (LIA) whose output is then fed into the clock and data recovery (CDR). The data output of the CDR is afterwards demultiplexed from 10 Gb/s to four 2.5-Gb/s data streams by two stages (DMUX). The four signals are provided as the buffered chip outputs RXD0–RXD3. The recovered 10-GHz clock is divided likewise by four and provided as a buffered chip output signal RXClk. An external 622-MHz clock (Refclk) is used by the CDR as reference for initial calibration. For the transmitter, the four 2.5-Gb/s data streams TXD0–TXD3 are multiplexed by two multiplexer stages (MUX) into a 10-Gb/s data stream, which is then retimed and buffered to provide the low jitter output signal, DO (Fig. 1). The required 10-GHz clock is generated by a clock multiplying unit (CMU).

A. 10-GHz LC Voltage-Controlled Oscillator

Two *LC* voltage-controlled oscillators (VCOs) are implemented, which share a common building block (see Fig. 2) and operate at 10 GHz. The quadrature VCO in the CDR consists of two cross-coupled VCO building blocks while the CMU VCO uses only one. The tank of the VCO is realized using an on-chip inductor, pn-junction varactors, and an array of switched metal–insulator–metal capacitors (mim-caps). The varactors and inductor are designed to achieve the stringent jitter requirements of the *LC* oscillator. The pn-junction varactors are implemented as stripes of p+ diffusion in the n-well as this provides a high quality factor even at frequencies above 10 GHz ($Q > 15$). For the inductor, a novel horseshoe shape with notches increases the quality factor at 10 GHz. The quality factor is deteriorated by two effects: the skin effect, which forces most of the current to the surface of the conductor, and the proximity effect, which is the increase of current density on the inside caused by the lower magnetic field there. To oppose these effects, the proposed structure has notches on the inside edge, as shown in Fig. 2. These notches force the current toward the outside, leading to a more uniform current distribution across the conductor. Yet the width of the conductor is only locally reduced so that the dc resistance is only slightly increased. As the average radius of the current path is larger, the inductance is increased as well. Measurements confirmed an increase in inductance by 6% and in the quality factor by 30% to a value of 26 at 10 GHz. The architecture of the oscillator combines a coarse/fine tuning scheme, to achieve low phase noise together with a wide tuning range, as depicted in Fig. 2. In the coarse tuning section, a mim-cap array provides a tuning range of 1.2 GHz. The pn-varactors with a tuning range of

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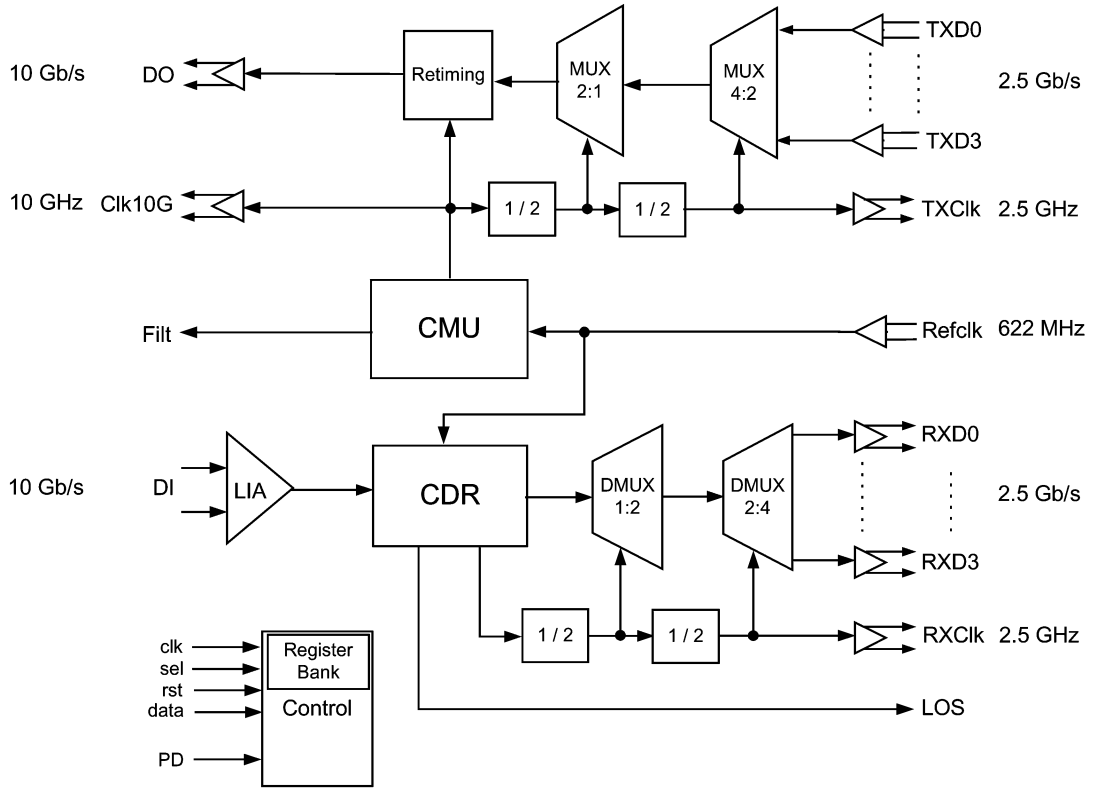


Fig. 1. Transceiver architecture.

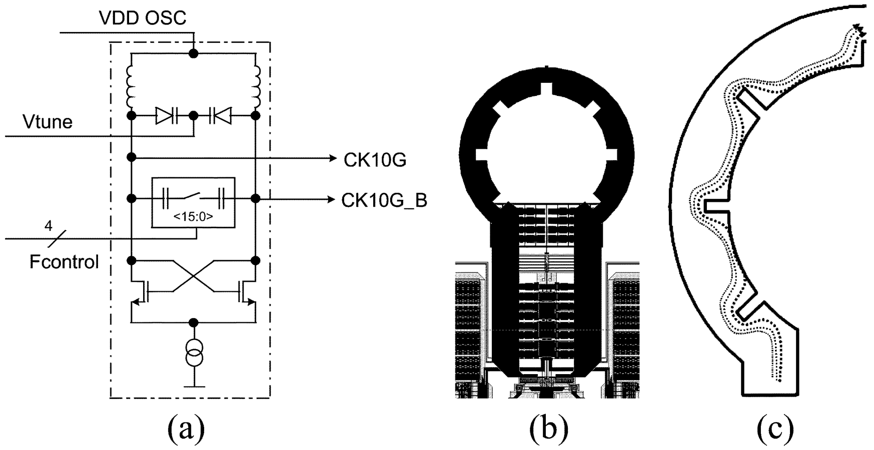


Fig. 2. A 10-GHz *LC* VCO. (a) Schematic. (b) Layout. (c) Current path.

300 MHz are used for continuous tuning during normal operation of the phase-locked loop (PLL). As the capacitance of the pn-varactors is small, the total tank capacitance is very linear. Hence, phase noise is low, as only a small amount of noise is upconverted. A cross-coupled NMOS differential pair provides the negative transconductance. The 10-GHz *LC* VCO achieves a phase noise of -118 dBc at 1-MHz offset, drawing 6.5 mA from a 1.2-V supply. A figure of merit [3] of 190 dB results.

B. High-Speed Current Mode Logic

All high-speed logic functions are based on current mode logic (CML). Active shunt peaking with NMOS loads [4] results in 70% higher bandwidth. As an example, a latch and a buffer are shown in Fig. 3. The dc gains of the CML stages are insensitive to process, temperature, and bias current variations since they are primarily determined by the ratio of load and input transistor dimensions: $A_{\mathrm{dc}} = gm2/gm1 = \sqrt{(W2/W1)}$. Two antiparallel diode-connected NMOS transistors limit the output voltage swing, thus the input pair of the following stage is not overdriven and at the same time the NMOS loads are never fully turned off.

C. Power Supply Concept

With the applied power supply concept, the supplies of the high-speed CML cells are linearly regulated on a per block basis, which allows maximum signal swing without exceeding

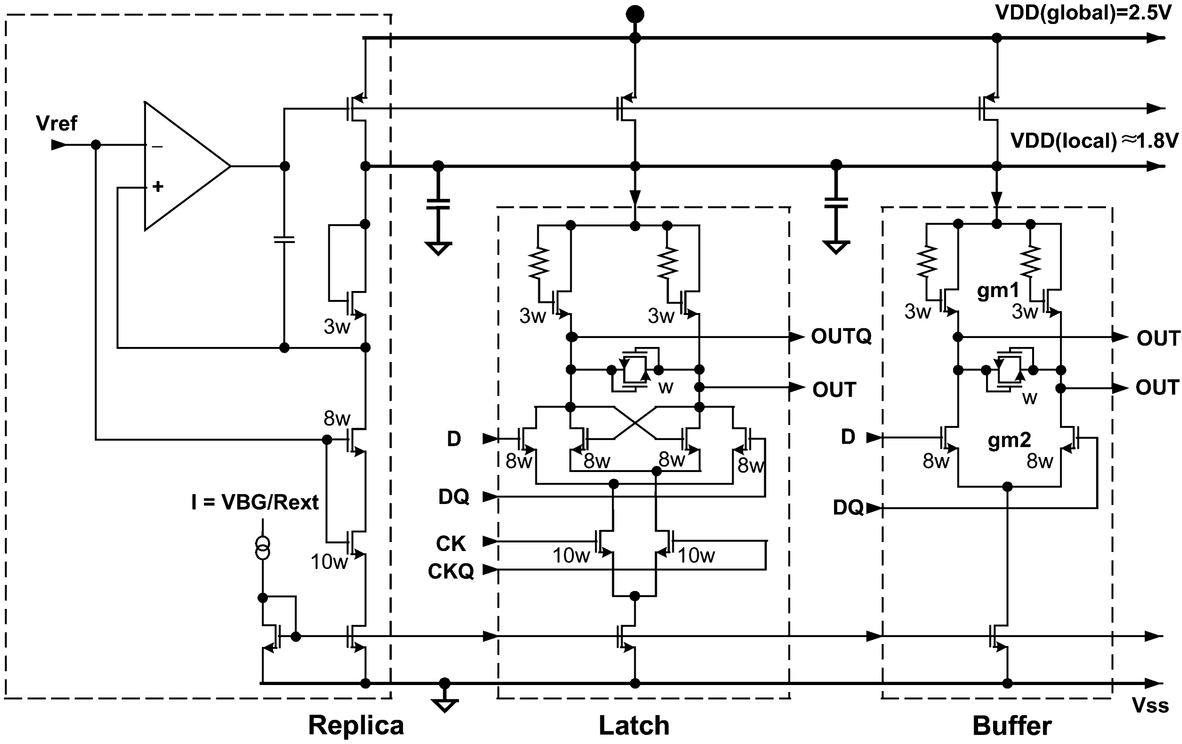


Fig. 3. Power supply concept and high-speed CML logic.

device breakdown voltages. High-frequency crosstalk between Rx and Tx is minimized by local capacitive coupling of the regulated supplies to a common ground plane and by providing a very low impedance path with 29 bondwires to the external ground. The ground plane is realized using metal layer 1 across the entire chip and additionally metal layers 2–6 where space is available. The supply regulators provide isolation of the local supplies from the global one. Further, they have the advantage that all *LC* loops formed by bondwire inductances together with external capacitances and on-chip decoupling capacitance are well damped, as the linear regulators introduces a large impedance into the loops. In addition, no external decoupling capacitances are needed that could prove to be inductive at high frequencies.

III. RECEIVER

A. Limiting Amplifier

In the receive path, the 10-Gb/s input data is first amplified by the LIA, which provides 30 dB of gain at a bandwidth of 7.5 GHz. Its topology (see Fig. 4) is similar to that presented in [4]. However, five gain stages with active shunt peaking and a common-gate input stage [8] are used. The input stage provides 500-mVpp differential input range. The shunt peaking realized with NMOS loads is not used to the full extent as it would cause horizontal closure of the eye pattern due to increased group delay distortion. The signal in the amplifier stages is limited by antiparallel NMOS diodes, which have resistors in front of the gates to shield the output nodes from the gate capacitance. For offset compensation, a balanced integrator circuit amplifies the offset of the output and feeds an error signal into the node between the common gates input stage and the first gain stage of the amplifier. The bandwidth of the offset cancellation loop is set to 50 kHz to keep baseline wander low. To achieve acceptable return loss, the input impedance of the input stage has to be calibrated to match the 100-Ω line impedance (see Fig. 5). The calibration is accomplished by forcing a well-defined current I_{ts} into a replica of the common input stage. The voltage drop, which results at the input, is regulated to a fraction of the bandgap voltage $(v_{\text{ref}} = mv_{\text{bg}})$ by adjusting the bias currents of the common-gate input stage. Since I_{tst} is derived from the bandgap voltage with an external resistor, the synthesized impedance is a function of the resistor R_{ext} and the fraction m only. Both the replica and the regulator opamp are chopper stabilized, thus only mismatch in the current mirrors used for biasing leads to manufacturing tolerances, which can easily be kept below 3%.

B. Clock and Data Recovery

The full-rate architecture of the CDR (Fig. 6) employs a two-loop approach: a fast phase-tracking loop and a slow frequency-tracking loop, both operating continuously. To achieve a smooth transition from frequency to phase tracking, the frequency detector is implemented as a quadrature correlator [6]. Depending on the phase relation between the data transition and the quadrature clock provided by the quadrature VCO, the frequency detector (FD) in conjunction with a charge pump generates an error voltage V_{tune} that adjusts the VCO frequency to the input data rate. After frequency acquisition, the FD output is zero and thus the charge pump is tristated. The phase-tracking loop (Fig. 7) is implemented with a bang-bang phase detector (PD) [5]. Depending on the phase relation between the VCO clock CKI and the incoming data, the PD produces a binary signal V_{PD}, indicating whether the clock is leading or lagging the data.

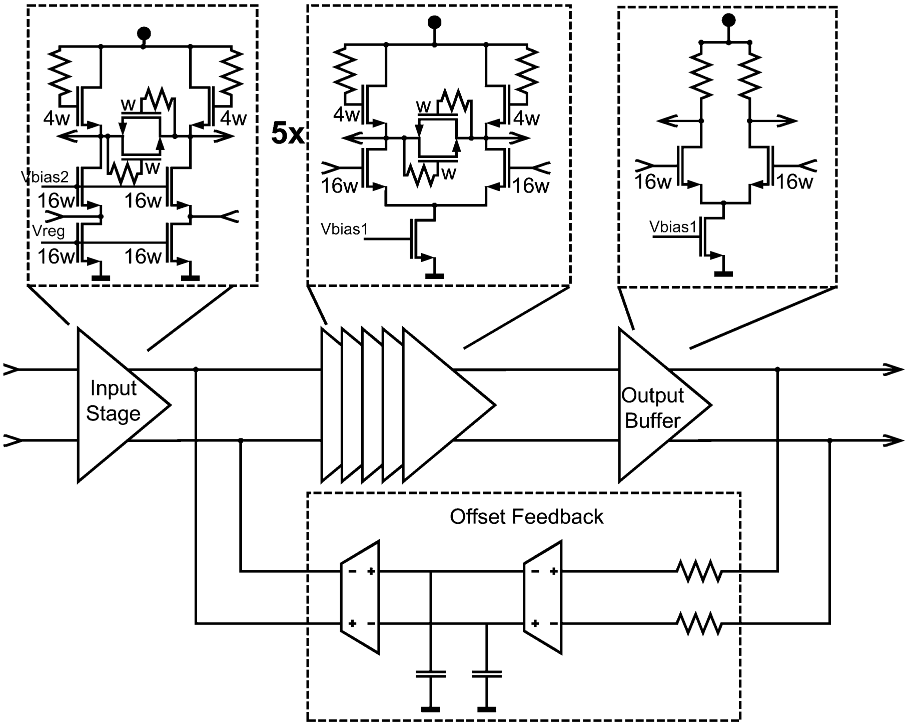


Fig. 4. Limiting amplifier (LIA).

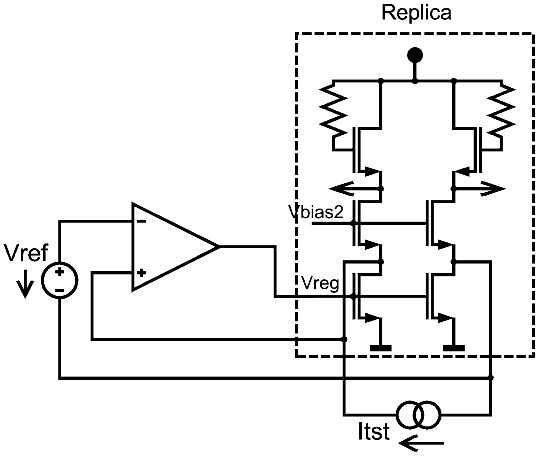


Fig. 5. LIA: tuning circuit for input impedance matching.

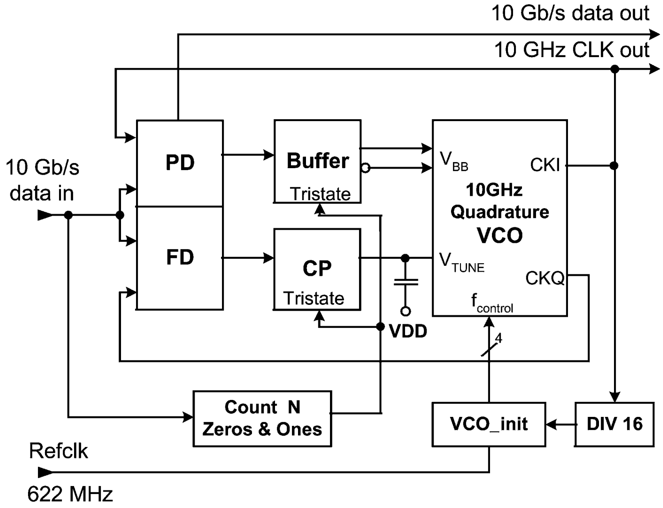


Fig. 6. CDR.

Under lock conditions, the rising edges of the clock are aligned with the data transitions while the falling edges of the clock sample the data in the middle of the symbol interval. A buffer then converts the binary PD output V_{PD} to a fully differential tuning voltage of $\pm V_{\mathrm{BB}}$, thus switching the VCO around the center frequency, which is determined by the FD loop. To avoid phase drift and jitter due to long runs of consecutive 0's and 1's, an additional counter is implemented, indicating if more than N consecutive 0's or 1's at the input are detected [7]. In this case, the counter output CZO sets the buffer output voltage V_{BB} to zero and switches the bang-bang loop to tri-state. The quadrature *LC* VCO, which is controlled by both the FD and PD loops, consists of two cross-coupled VCO building blocks (Fig. 8). The cross-coupling is implemented with differential pairs, whereby the coupling coefficient is determined by device sizes only. Moreover, it is sufficiently larger than the magnetic coupling between both inductors to maintain quadrature phase relation. The pn-varactors are part of the frequency tuning loop, while four antiparallel pn-varactors are added for the bang-bang phase loop. Due to the antiparallel connection of these additional varactors, their nonlinearity is canceled to first order.

IV. TRANSMITTER

During startup, the digital control circuit (VCO-init) disables the charge pump, with the CPreset signal, and calibrates the VCO to 16 times the reference clock (see Fig. 9). This digital calibration achieves an accuracy of 1%, hence automatic adaption for most 10-Gb/s applications is provided. Given the demanding nature of the SONET/SDH jitter specifications, a mostly differential design is used in the CMU: both the VCO

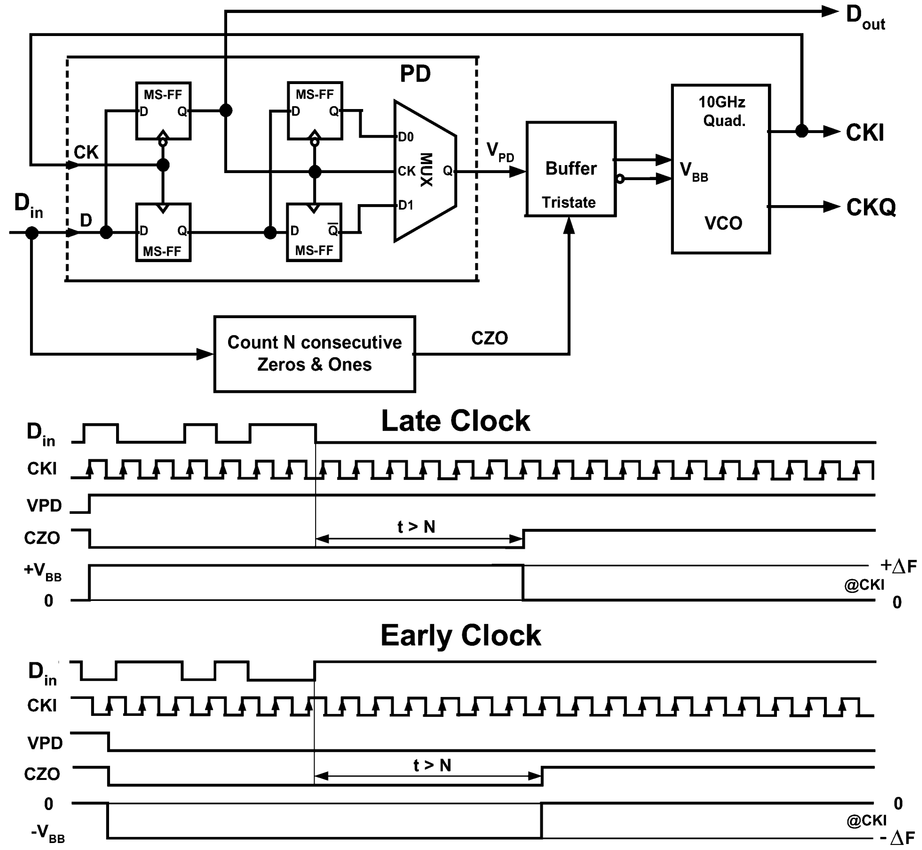


Fig. 7. Phase tracking loop (bang-bang).

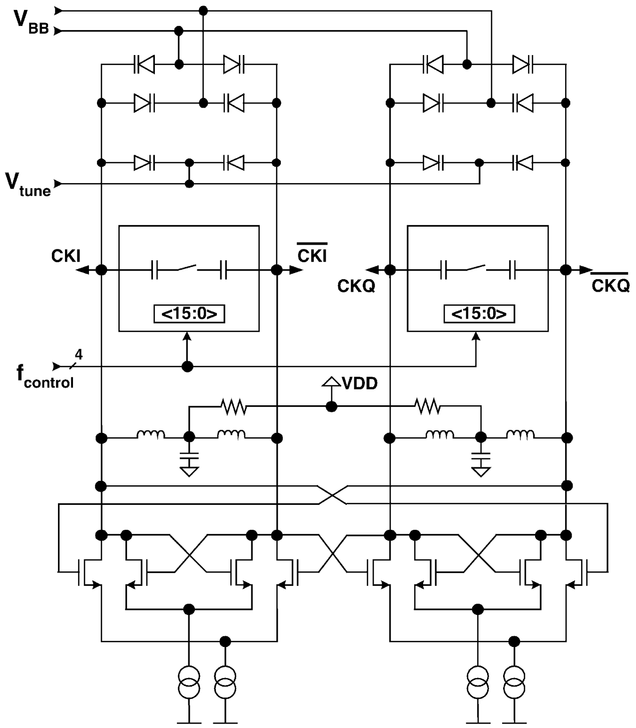


Fig. 8. Quadrature *LC* VCO.

and CML blocks are fully differential. However, the loop filter is connected to the VCO in a pseudodifferential manner, as one side of the filter output is connected to the tuning input and the other side to the center tap of the inductor, as shown in Fig. 9. Hence, a single-ended topology for the charge pump is sufficient. The linear phase–frequency detector is a conventional three-state style structure based on D-flip-flops. The nonlinear gain characteristic of the VCO is compensated by adjusting the charge pump current to keep PLL loop bandwidth and stability constant. The increase of tuning voltage (speeding up the VCO) is associated with a reduction of VCO gain. This reduction is compensated by increasing the charge pump current proportional to the scale factor (SF). Fig. 10(a) shows SF and the VCO gain before and after linearization, and Fig. 10(b) shows the linearization circuitry. The CMU bandwidth is set by the on-chip loop filter to 8 MHz [see Fig. 11(a)]. An external filter can be connected in parallel to the internal loop filter to satisfy the SONET requirement for jitter transfer peaking of less than 0.1 dB. The peaking of the jitter transfer function is then in accordance to SONET requirements [see Fig. 11(b) and 12], yet the bandwidth of approximately 1 MHz does not meet the SONET requirement of less than 120 kHz.

V. MEASUREMENT RESULTS

All measurements were taken at the OC-192 data rate (9.953 Gb/s). To evaluate the sensitivity to crosstalk, measurements were also taken with 20 ppm reference clock offset between Rx and Tx, as this is a very critical case for practical applications. A summary of the measurements is shown in Table I.

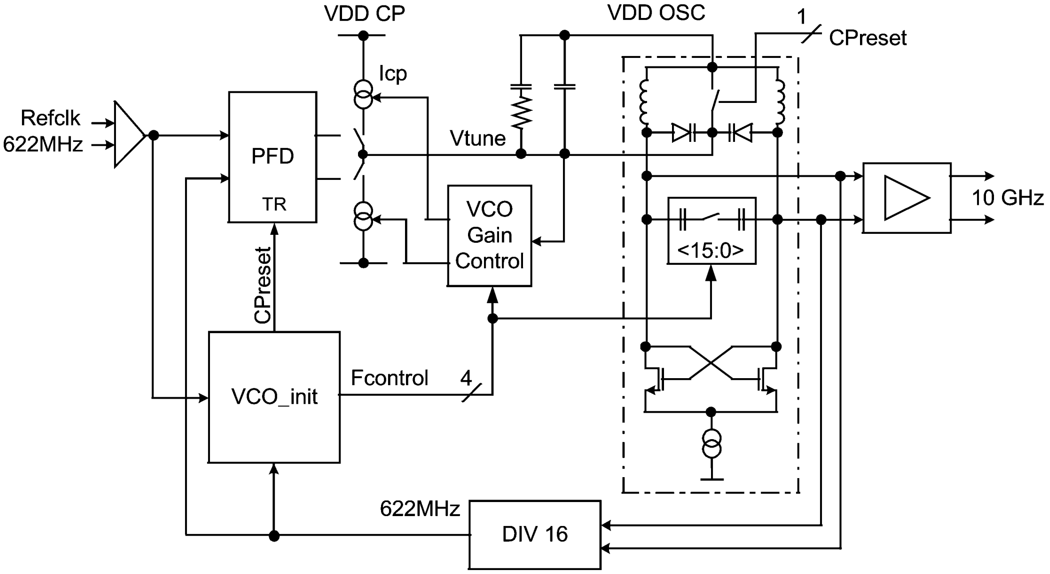
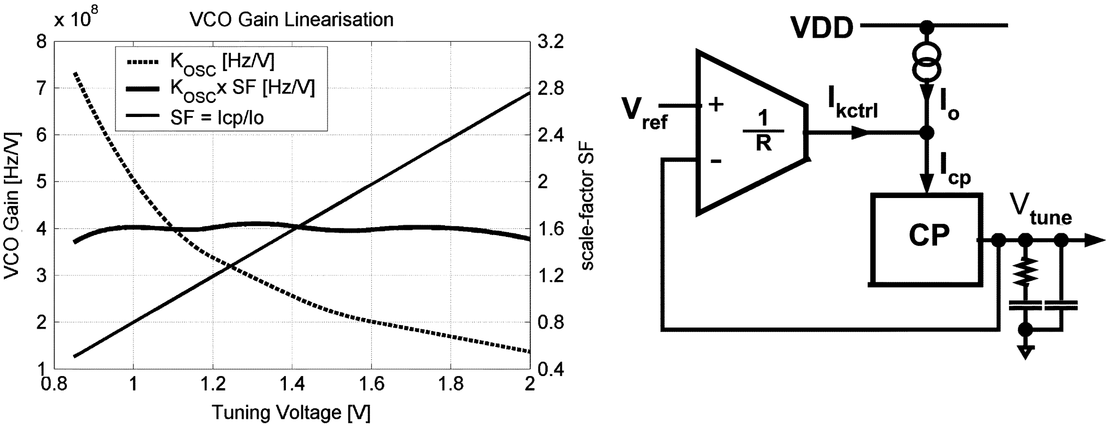


Fig. 9. Clock multiplying unit (CMU).



(a) (b)

Fig. 10. VCO gain linearization. (a) VCO gain. (b) Gain control.

A. Transmitter Measurements

The extremely small clock jitter at the output of the CMU has been measured with a jitter analyzer (Anritsu MP1777A) and verified with phase noise measurements (Agilent HP4352B). The jitter analyzer measurements revealed a jitter of 200 fs rms and 2.0 $\mathrm{ps}_{\mathrm{pp}}$, which is five times below the maximum allowed SONET/SDH specification of 1 ps rms. The measurement was performed at a bit error rate (BER) of less than 10^{-12} and bandwidth of 50 kHz to 80 MHz. Fig. 13 presents the overlaid phase noise measurements of the free-running *LC* VCO, the 622-MHz reference clock at the input, and the 10-GHz clock at the output of the CMU. It is evident that the CMU output exhibits a phase noise characteristic identical to the reference clock, yet the phase noise magnitude is scaled up by approximately 24 dB, which reflects the CMU multiplication factor of 16. Hence, converting phase noise into jitter reveals that the main contributor of the 10-GHz clock jitter is actually the reference clock itself. Integrating the phase noise from 50 kHz to 80 MHz yields a jitter of approximately 200 fs rms, which verifies the jitter analyzer measurement. Crosstalk measurements with 20 ppm transmitter and receiver reference-clock offset reveals a low additional jitter of 100 fs pp on the 10-GHz transmit clock, which confirms the presented power supply

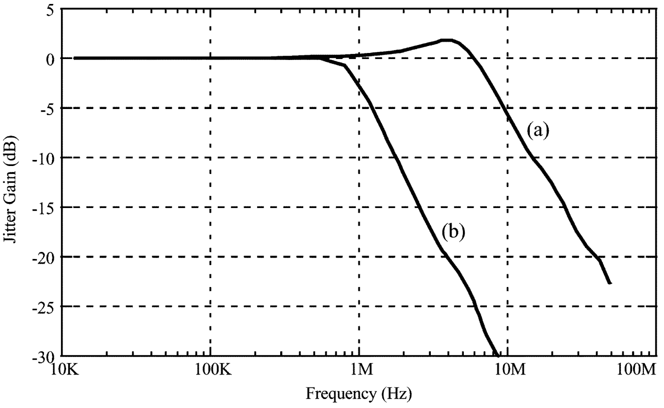


Fig. 11. CMU bandwidth. (a) On-chip loop filter. (b) With external loop filter.

TABLE I
MEASUREMENT SUMMARY

Technology	CMOS 0.13um, 1-poly, 8-metal
Supply voltage	1.2V / 2.5V
Power dissipation (with LIA)	980mW (<1.2W)
Chip size	3mm x 5mm
Bit rates	9.953/10.31/10.664/10.709 Gb/s
Input data sensitivity	15 mVpp single-ended
Recovered clock jitter (locked to 2.5 GHz sinusoid)	0.4 ps_rms within 50 kHz-80MHz
Recovered clock jitter (locked to a 2^31-1 PRBS)	1.1 ps_rms, 8.3 ps_pp full BW
Jitter tolerance	better 0.45 UIpp
Receiver jitter transfer peaking	< 0.1 dB
Transmitter jitter bandwidth	8 MHz (closed loop BW)
Transmitted clock jitter 0 ppm RX/TX	2.0 ps_pp and 200 fs_rms in 50 kHz-80 MHz
Transmitted clock jitter +-20 ppm RX/TX	2.1 ps_pp and 220 fs_rms in 50 kHz-80 MHz
Transmitter jitter transfer peaking	< 0.1 dB (with ext. filter) 1.5 dB (without ext. filter)
Transmitted serial data swing	800 mVdpp
VCO capture range (coarse tuning)	+-600 MHz nom. Freq. 10.31 GHz
VCO locking range (fine tuning)	+-150 MHz nom. Freq. 10.31 GHz

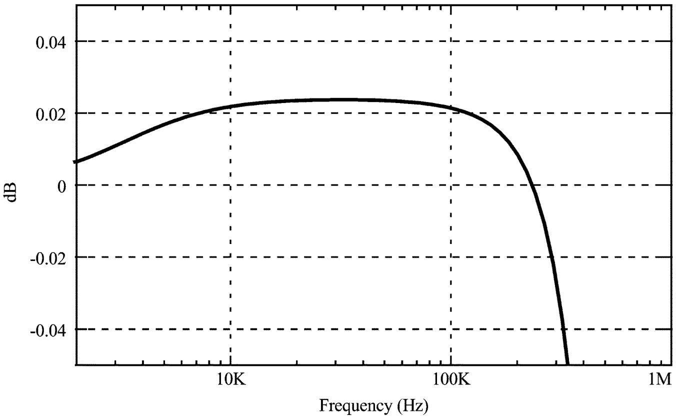


Fig. 12. CMU jitter peaking with external loop filter.

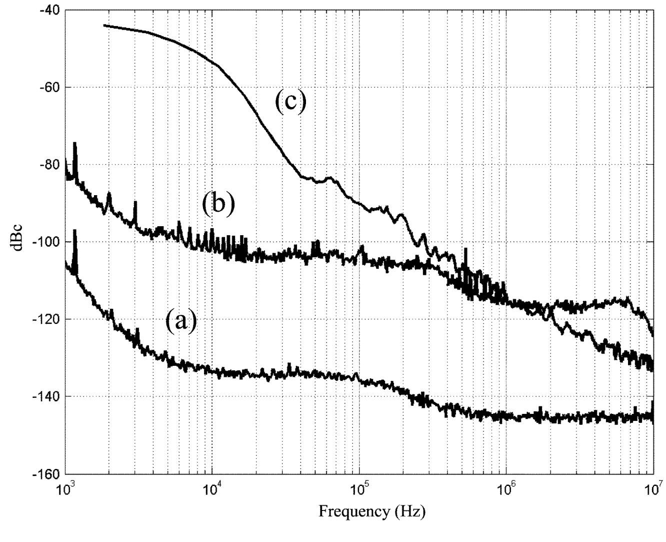


Fig. 13. (a) Phase noise of the reference clock. (b) Phase noise of the CMU. (c) Phase noise of the free-running oscillator.

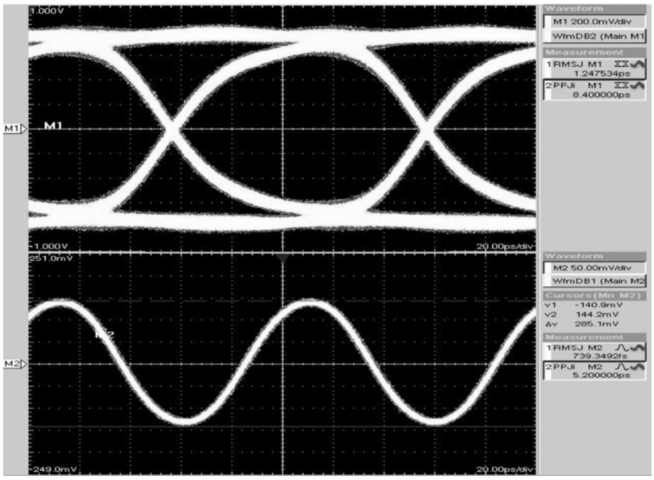


Fig. 14. Transmitter output waveforms. Measurements include data-dependent jitter at high frequencies above 80 MHz and are further exacerbated by approximately 700 fs rms oscilloscope jitter (Tektronix CSA800B).

approach. The eye diagram of the 10-Gb/s data and the 10-GHz clock output measured with a $2^{31}-1$ pseudorandom bit sequence (PRBS) pattern is shown in Fig. 14. An open eye and only negligible intersymbol interference (ISI) can be observed in the data pattern. The differential amplitude of the data signal exceeds 800 $\mathrm{mV_{pp}}$ and the differential amplitude of the clock signal 600 $\mathrm{mV_{pp}}$.

B. Receiver Measurements

The jitter tolerance of the receive path, which comprises the LIA, CDR, and 1:4 DMUX, has been measured at a BER of 10^{-12} with a PRBS pattern applied differentially to the input. For an LIA input signal of 100 mVpp, which corresponds to the nominal value of the CDR input, approximately 0.5 UI is measured. For an input signal of 15 mVpp single-ended, a high-frequency jitter tolerance greater than 0.35 UI is achieved. The measurements show that the jitter tolerance specifications for SONET OC-192 are exceeded with more than 100% margin (see Fig. 15). A PRBS pattern produces 8.3 ps pp jitter and

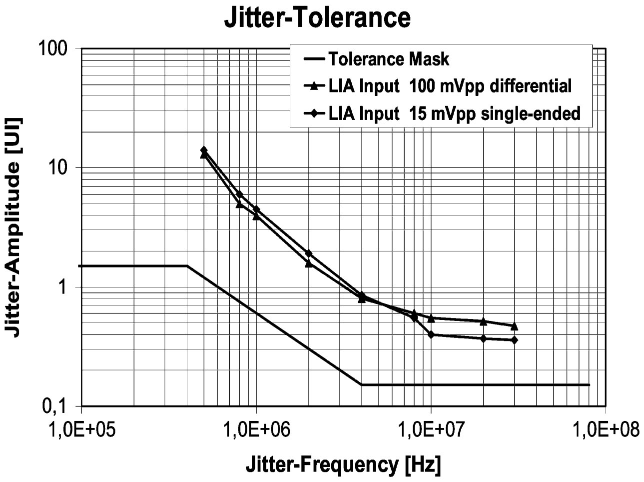


Fig. 15. CDR jitter tolerance measurements.

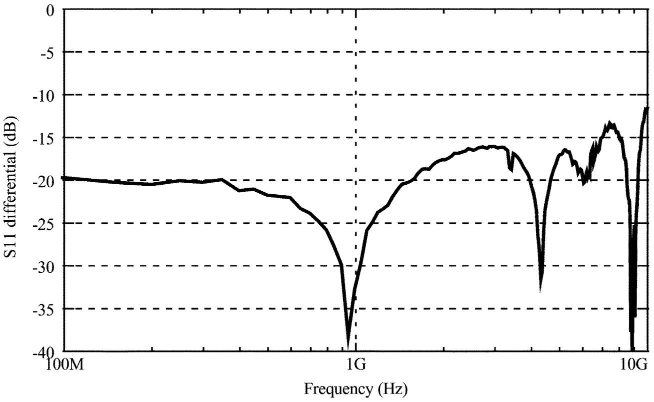


Fig. 16. LIA: input return loss.

1.1 ps rms jitter on the full-rate recovered clock, which includes 700 fs rms jitter of the oscilloscope trigger (Tektronix CSA8000B). Measuring the phase noise with a spectrum analyzer yields −106 dBc at 1-MHz offset. The jitter generation in the SONET band from 50 kHz to 80 MHz is 0.4 ps rms. The return loss measurement of the synthesized input impedance of the LIA is shown in Fig. 16.

VI. CONCLUSION

A fully integrated 10-Gb/s transceiver operating from 9.95 to 10.7 Gb/s is implemented in a 0.13-μm CMOS process. The design is a full rate architecture and features a novel notched inductor layout and a special power supply concept. The receiver input sensitivity is 20 mV at a BER below 10^{-12}. Jitter tolerance and jitter generation specifications for SONET OC-192 are exceeded by margins of 100% and 500%, respectively. Crosstalk measurements reveal a low additional jitter of 100 fs pp on the 10-GHz transmit clock, which confirms the presented power supply approach. A microphotograph of the chip is shown in Fig. 17, and the results of the measurements are summarized in Table I.

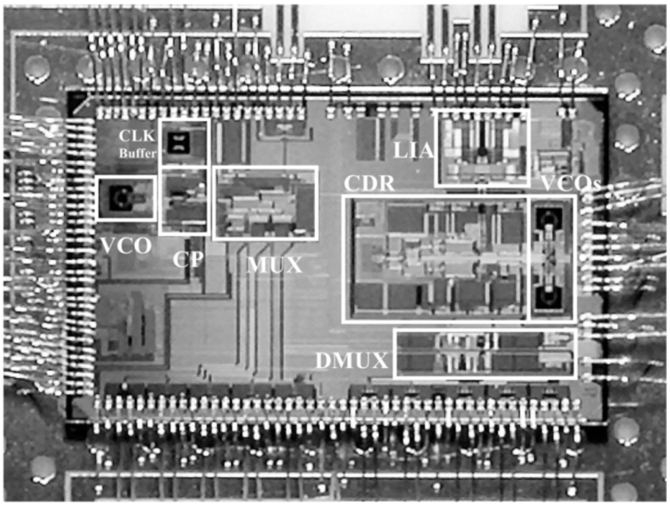


Fig. 17. Chip microphotograph. Chip size is 3 mm × 5 mm.

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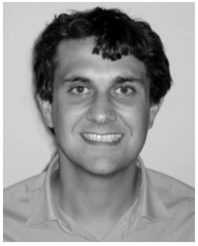
From 1995 to 1998, he was with the Siemens Semiconductor Division, Munich, Germany, working as an Analog Design Engineer on analog front ends and clock multiplying units for security ICs. In 1998, he moved to the Mixed-Signal Department, Infineon Technologies AG, where he designed VGAs, active filters, clock and data recovery, and sigma–delta data converters for T1/E1 and DS3/E3/STS1 transceivers. In 2000, he joined Xignal Technologies AG, Munich, where he develops highly linear 12/14-b continuous time sigma–delta data converters for VDSL and ADSL2 transceivers. Additionally, he is involved in the design of clock and data recovery and clock multiplying units for high-speed multigigabit transceivers for communication products. He currently holds two international patents.



Ernesto Romani (M'00) was born in Giulianova, Italy, in 1972. He received the Laurea degree in electrical engineering from the University of Ancona, Ancona, Italy, in 1997.

From 1999 to 2002, he was with Infineon Technologies AG, Munich, Germany, where he worked on embedded memories and developed analog circuits for DRAMs. In 2002, he joined Xignal Technologies AG, Munich, where he develops mixed-signal and RF circuits for telecommunications.

Frédéric Roger (M'04) was born in Paris, France, on December 17, 1973. He received the Ingénieur degree from the Ecole Supérieure d'Ingénieurs en Electronique et Electrotechnique (ESIEE), Paris, France, in 1996.

He was a Research Engineer at Collège de France (CNRS-IN2P3), Paris, from 1996 to 1999, where he worked on high-speed data acquisition electronics used in particle physics experiments. In 1999, he joined Infineon Technologies, Munich, Germany, to work as a Mixed-Signal Design Engineer and project leader for GSM baseband ICs. Since 2001, he has been with Xignal Technologies AG, Munich, where he is currently a Senior Staff Engineer and Project Manager for 10-Gb/s CMOS transceiver ICs.

Thomas Blon (M'99) was born in 1968 in Buchloe, Germany. He received the M.S. degree in electrical engineering from the Technical University of Munich, Munich, Germany, in 1994.

From 1994 to 1998, he was with the Siemens Semiconductor Division, Munich, working as an Analog Design Engineer on xDSL analog front ends. From 1999 to 2001, he was with the R/W Channel Group of Infineon Technologies Corporation, Santa Cruz, CA, designing high-speed CMOS mixed-signal building blocks for hard disk drive and optical storage applications. In 2002, he joined Xignal Technologies AG, Munich, where he is focusing on the design of highly linear DSL as well as high-speed multigigabit circuits for communication products. He currently holds eight international patents.

Michael Moyal (M'00–SM'03) was born in 1954 in Tel Aviv, Israel. He received the B.S. degree in mathematics and physics from the University of Oregon, Eugene, the M.S.E.E. degree from Oregon State University, Corvallis, in 1982, and the Ph.D. degree from Universität der Bundeswehr Munich, Munich, Germany, in 1998.

From 1982 to 1985 and from 1988 to 1995, he was with the Communication Product Division of Advanced Micro Devices (AMD), Santa Clara, CA, as a Department Manager of SLIC/SLAC analog line cards. From 1985 to 1988, he was with IXYS, San Jose, CA, designing smart DMOS and motion control ICs. From 1995 to 1999, he was with Siemens AG (later Infineon Technologies), Munich, as a Senior Manager responsible for ISDN and xDSL transceivers. He has published six papers in international journals and holds 13 patents. He is a founder of Xignal Technologies AG, Munich. He served on its board and as Chief Technical Officer from 1999 to 2003 and as Chief Scientist from 2003 to the present. His current interests are wide-bandwidth data converters and RF-CMOS and transceivers architectures.

Marcello Vena received the M.S.E.E. degree with honors from the University of Palermo, Palermo, Italy, in 1998.

From 1997 to 1998, he was working as an RF Design Engineer with the Microwave Laboratories, Alenia Spazio, Rome, Italy, developing HMIC circuits for satellite applications. From 1998 to 2000, he worked for Mikron AG, Munich, Germany, as a Digital and Mixed-Signal Designer for industrial and automotive low-power ASICs. In 2000, he joined National Semiconductor, Fürstenfeldbruck, Germany, as a Digital Design Engineer for the Information Appliances Division, where he developed several key modules for the CR16 microcontroller platform. Since 2002, he has been with Xignal Technologies AG, Munich, where he leads the digital design team which focuses on the design of high-performance DSP circuits and advanced control units for the analog circuitry in telecommunication products.

Andrea Melodia was born in Lecce, Italy, in 1975. He received the M.Sc. degree in telecommunications engineering from the University of Bologna, Bologna, Italy, in 2000.

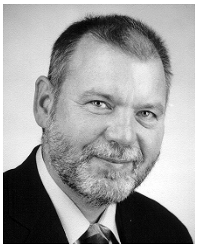
He began his career at Infineon Technologies AG, Munich, Germany, and in 2001, he joined Xignal Technologies AG, Munich, where he is focusing on the design of both analog and digital circuits for communication products.

John Fisher was born in Miami, FL, in 1956. He received the B.S. degree in electrical engineering from Montana State University, Bozeman, in 1980 and the M.B.A. degree from INSEAD, Fontainebleau, France, in 1989.

Since 1981, he has held a number of technical and commercial positions in the semiconductor industry. He is currently Senior Manager of Product Marketing at Vishay Semiconductor GmbH, Heilbronn, Germany.

Grégoire Le Grand de Mercey was born in Paris, France, in 1976. He received the M.S.E. degree in electrical engineering from the Institut Supérieur d'Électronique de Paris, Paris, France, in 2001. He is currently working toward the Ph.D. degree at Bundeswehr University, Munich, Germany.

His research interests are in high-frequency CMOS RF integrated circuits with an emphasis on oscillators. Since 2004, he has been with Infineon Technologies AG, Munich, where his work is focused on CMOS circuit design for wireless applications.



Heribert Geib (M'90) received the degree in electrical engineering and the Diploma in physics from the Johannes Gutenberg University, Mainz, Germany, and the Ph.D. degree in electrical engineering from the University of Darmstadt, Darmstadt, Germany.

He joined Xignal Technologies AG, Munich, Germany, in 2001 after 15 years of experience in several divisions of Infineon and Siemens R&D. His last assignment before joining Xignal was Director of Systems Engineering within the High-Speed Communication IC Division of Infineon, where he focused on 40-Gb/s IC development and various systems for optical transmission. Prior to his high-speed communication activities, he was Product Manager at Infineon's Image and Video Division. He led the development of a single-chip CMOS camera, which was presented at the ISSCC in 1999. He also worked on algorithms for video codecs and their VLSI implementations and was deeply involved in the development of CMOS submicron technologies. He holds 12 patents and has published more than 20 papers in international journals and conference proceedings.