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A Voltage Level Converter Circuit Design with Low Power Consumption

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EXTENDED ABSTRACT

A semiconductor integrated circuit employs multiple supply voltages to reduce the power consumption by an internal circuit. For example, an internal supply voltage used for an internal circuit is generated from an externally supplied a higher supply voltage, and the internal supply voltage is supplied to the internal circuit to reduce the power consumption by the internal circuit. Since an output signal generated by the internal circuit is a lower voltage internal signal, at the front stage of an output circuit, a level conversion circuit converts the level of this signal into a signal for the higher external supply voltage [1]-[8].

In practice, a CMOS logic circuit may be preferred to have mixed gates operating on a lower supply voltage VDDL and gates operating on a higher supply voltage VDDH. However, any gate operating on VDDH and connected after the gate operating on VDDL generates a short-circuit current. Fig. 1 shows a CMOS logic circuit consisting of first and second CMOS inverters which are directly connected to each other. The first CMOS inverter operates on a lower supply voltage VDDL and the second CMOS inverter on a higher supply voltage VDDH. If a node between the first and second inverters is at the lower supply voltage VDDL and if VDDL<VDDH-|Vthp|, the MP2 is incompletely turned off, the short-circuit current flows from a power supply of the higher supply voltage VDDH toward a ground through the second inverter. To prevent the short-circuit current, the level converter must be interposed between a gate operating on the lower supply voltage VDDL and a gate operating on a higher supply voltage VDDH.

Fig. 2 shows a conventional level converter, named the Dual Cascode Voltage Switch (DCVS), interposed between gates operating on different supply voltages in a CMOS logic circuit, to prevent the short-circuit current and reduce power consumption. Although the level converter blocks the short-circuit current, it consumes relatively large dynamic power when it carries out a switching operation. If the CMOS logic circuit must have many level converters, the power consumption thereof will increase to nullify the effort of decreasing power consumption by using the two supply voltages VDDL and VDDH. Furthermore, this conventional level converter has relatively large delay because it is rely on a contention between different transistors on the level conversion path [6].

Hence, we proposed an improved circuit as shown in Fig. 3 to reduce the contention problem so as to achieve high speed and low power consumption. In this circuit, the level conversion circuit converts a signal X on the lower supply voltage side into a signal Y on the higher supply voltage side; the signal X is transmitted to the gates of transistors MN3, MN6 and MP6; and a signal /X for the inverted phase, which is generated by an inverter constituted by transistors MP1 and MN1, is transmitted to the gates of transistors MN2, MN5 and MP5; the respective gates of transistors MP2 and MP3 are cross-connected to the drains of transistors MP3 and MP2, while the sources of both transistors are connected to the higher supply voltage VDDH; and a node B is connected to an output buffer circuit, constituted by transistors MP4 and MN4, which is connected to the higher supply voltage VDDH.

Next, operation of the proposed level converter circuit will be explained. When the voltage level of input signal swings high to low, the output voltage level of the input inverter becomes the lower supply voltage VDDL. Therefore, MN2, MN5 and MP6 are turned on; as a result, node A is then discharged to a reference voltage VSS. Thus, MP3 becomes on, and then, voltage level of node B becomes a higher supply voltage VDDH. In this case, MP2, MN3, MN6 and MP5 are turned off, and thereby, it is possible to prevent a short-circuit current from flowing between the higher power supply voltage VDDH and the reference voltage VSS. On the other hand, when the voltage level of the input signal is switched to logic high, the output voltage level of the input inverter becomes a reference voltage VSS. Therefore, MN3, MN6 and MP5 are turned on; as a result, node B is then discharged to a reference voltage VSS. In this case, MP2 is turned on, and thereby, MP3 becomes off. Moreover, MN2, MN5 and MP6 are also turned off, and thereby, it is possible to prevent a short-circuit current from flowing between the higher power supply voltage VDDH and the reference voltage VSS. It is clear that there are three paths to speedup the output level transition in each input signal condition. These results provide faster output transitions as well as efficient voltage level conversion. As such, it can reduce the contention problem on nodes A and B. As a result, propagation delay time of the circuit itself becomes short. Moreover, no short-circuit current flows; therefore, it is possible to reduce power consumption.

Circuit simulation was carried out using HSPICE and 0.18μm CMOS technology parameters on a SUN ULTRA 10 workstation. HSPICE waveforms of the proposed circuit are shown in Fig.4 for VDDH=1.8V, VDDL=0.8V and an output capacitance of 0.1 pF. The simulation results reveal that the proposed circuit has faster speed and lower power

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consumption comparing with the conventional circuits. Additionally, the proposed circuit can operate level range from 0.8V shift to 1.5V, this feature is useful on the more low voltage supply systems. Accordingly, the proposed level converter circuit can be effectively applicable to an LSI high speed input-output circuit, as an interface between internal and external buses such as a server or exchanger, as an interface circuit between an optical device for optical communication and an LSI, etc.

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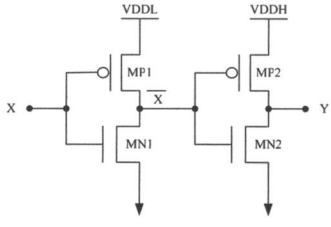

Fig.1 Direct connection of V_{DDL} circuit and the V_{DDH} circuit

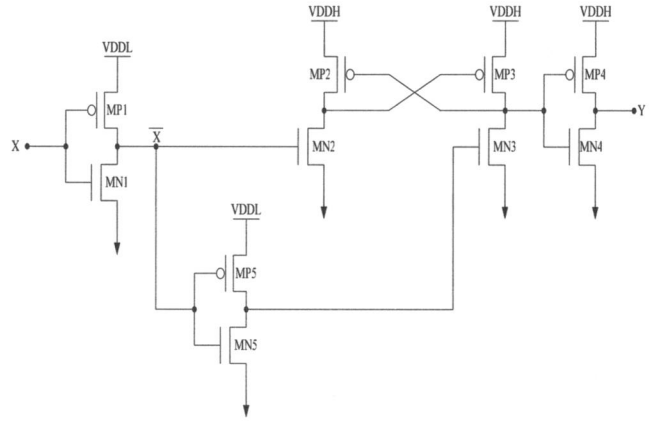

Fig.2 The conventional circuit (DCVS)

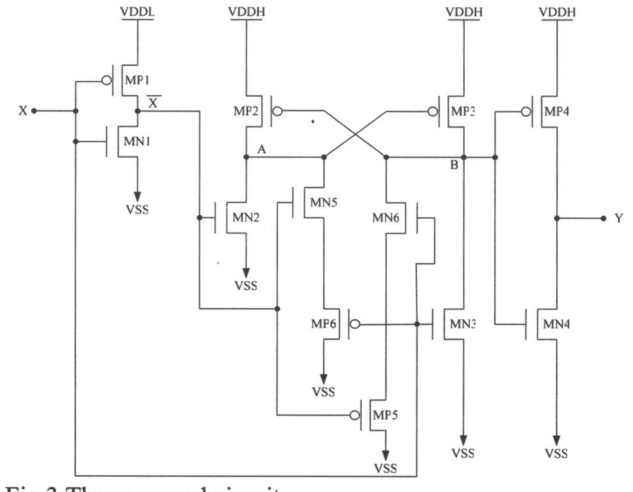

Fig.3 The proposed circuit

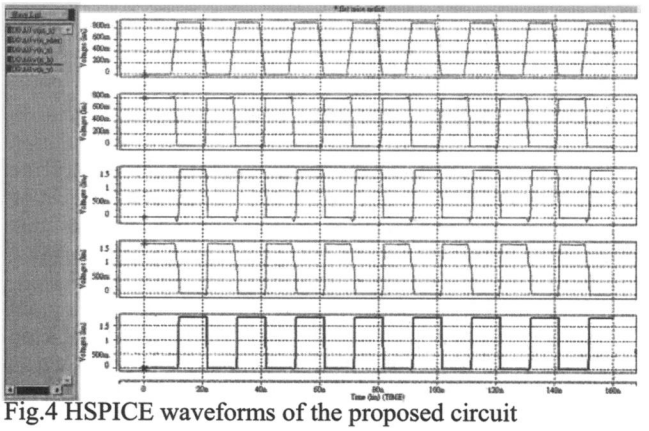

Fig.4 HSPICE waveforms of the proposed circuit