A Compact Switched-Capacitor Regulated Charge Pump Power Supply

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***Abstract*—A CMOS switched-capacitor reference is combined with a switched-capacitor voltage doubling charge pump to produce a compact regulated 3.2-V power supply from an input that ranges from 1.8 to 3.5 V. It can supply up to 6 mA at minimum input. The switched-capacitor topology uses a single PN junction and could allow for inputs and outputs less than 1 V. The concept of constant frequency charge pump regulation is discussed, as is the theory behind stability, load regulation, and efficiency. Measured results from a 0.5-μm CMOS process are given.**

***Index Terms*—Bandgap reference, capacitors, charge pump, circuit analysis, circuit stability, circuit topology, DC-DC power conversion, overcurrent protection, power conversion, power supplies, switched-capacitor circuits, voltage reference.**

I. Introduction

DC-to-DC converters are used to convert a variable low voltage source, such as a battery, into a higher, more usable, constant voltage. A regulated charge pump is a cost effective way to do this. Usually, the charge pumps are designed with separate cells for the bandgap reference, and the regulation circuit (Fig. 1). However, incorporating the reference into the regulation circuitry reduces the supply current and number of components used (Fig. 2). As will be shown, further improvements in component count and current consumption can be made by incorporating a switched-capacitor reference.

Section II develops the theory of charge pump regulation, efficiency, load regulation, and stability. Section III shows how a switched-capacitor reference can be combined with a charge pump to create a very compact power supply. Section IV covers the support circuitry, including in-rush current limiting circuitry, and the bulk bias. Finally, results from a 0.5-μm CMOS device embedded in an ASIC are given in Section V.

II. Charge Pump Theory

A. Constant Frequency Regulation

A simplified version of the charge pump described in this paper is shown in Fig. 3. It is a regulated voltage doubler and the regulation scheme is constant frequency; however, the integral regulation explained in this paper can be adapted to the various charge pump regulation schemes (pulse skipping, pulsewidth modulation (PWM), frequency modulation, etc.) and output ratios (voltage triplers, step down regulators, etc.).

Manuscript received December 5, 2005; revised March 1, 2006.

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Digital Object Identifier 10.1109/JSSC.2006.875303

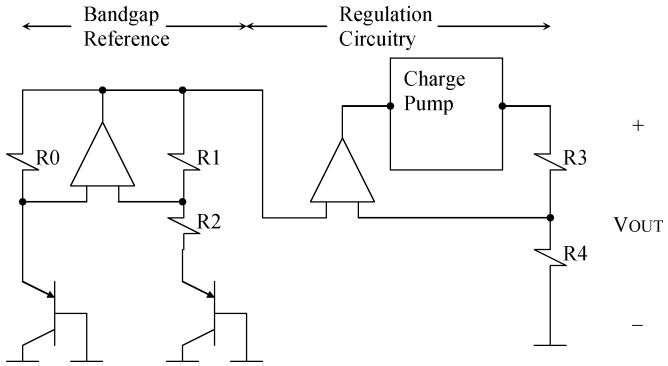

Fig. 1. Typical charge pump regulation scheme using a separate continuous time bandgap reference and regulating operational amplifier.

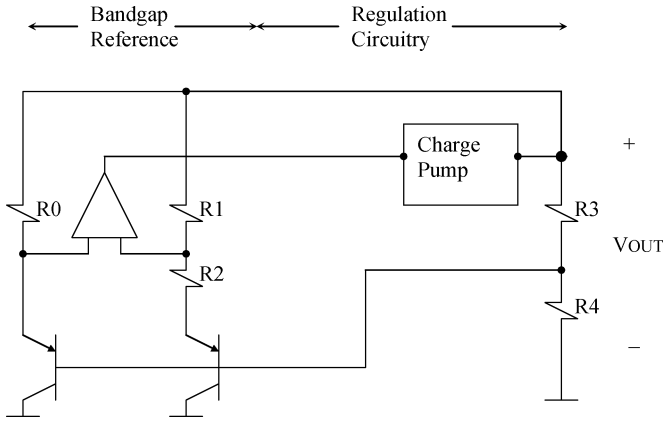

Fig. 2. Charge pump with integral regulation, which eliminates an operation amplifier.

There are two phases of operation: charging $(\phi 1)$ and discharging $(\phi 2)$. During the charge phase the flying capacitor $C_{\rm FLY}$ is charged to the proper voltage by putting it in parallel with the battery and regulating the charging current as shown in Fig. 4(a). During this time C_L supplies charge to the load. Fig. 4(b) shows the discharge phase in which the flying capacitor is put in series with the battery and discharged into the load and into the capacitor C_L. $C_{\rm FLY}$ and C_L are 1 μF and 10 μF external capacitors, respectively.

To control the amount of charge put onto $C_{\rm FLY}$ the output is compared to a reference voltage with the transconductance amplifier G1. If the output is too low, G1 will increase the charging current of $C_{\rm FLY}$. This will result in a higher output voltage when $C_{\rm FLY}$ is discharged. Thus, constant frequency regulation controls the amount of charge put on $C_{\rm FLY}$ by varying the charging current while keeping the charging rate and duration constant. Compare this with PWM which keeps

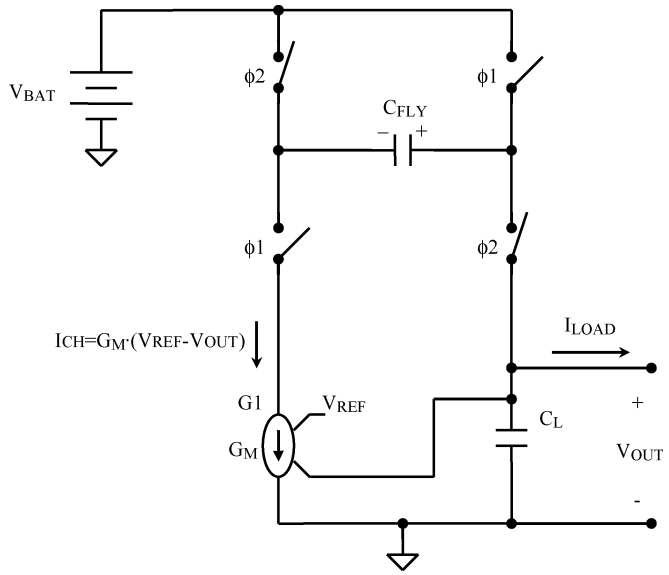

Fig. 3. Simplified model of voltage doubler using constant frequency regulation. If the output is lower than the reference the current $I_{\rm CH}$ will increase resulting in a higher output voltage.

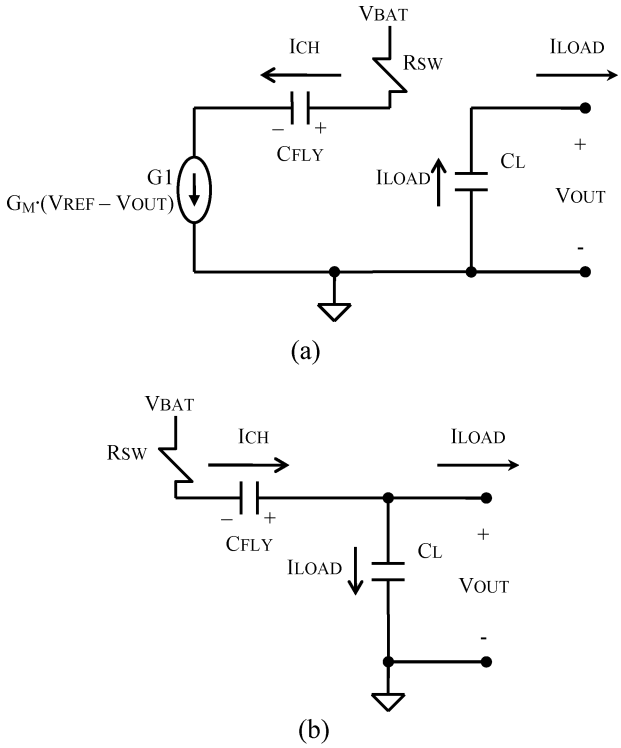

Fig. 4. Voltage doubler charge pump average currents with a constant load: (a) charge phase $\phi 1$; (b) discharge phase $\phi 2$. The charging current is controlled so that $V_{\rm OUT} = V_{\rm REF} - 2 \cdot I_{\rm LOAD}/G_M$.

the charging current constant, but varies the duration. Pulse skipping and frequency modulation vary the rate at which the charge is put on.

The main advantage of constant frequency regulation over the other schemes is that the noise frequency spectrum is well defined so it can be filtered or made synchronous with sensitive cells. A similar regulation scheme using quasi-switches is given by H. Chung in [1].

B. Efficiency

The currents in Fig. 4(a) and (b) are averages for each charge pump half cycle. Over a complete cycle the steady-state average currents of $C_{\rm FLY}$ and C_L must be zero so the average currents in (b) must be equal and opposite of the currents in (a). If they were not, the capacitor voltages would increase or decrease until a steady-state solution was reached. From Fig. 4(b) it can be seen that

$$I_{\rm CH} = 2 \cdot I_{\rm LOAD}. \tag{1}$$

The power efficiency is the ratio of power delivered to the load to the power delivered by the battery. In this ideal case, that ratio is $(V_{\rm OUT} \cdot I_{\rm LOAD})/(V_{\rm BAT} \cdot I_{\rm CH})$. It follows that the efficiency of a regulated voltage doubler is limited by

$$\eta < \frac{V_{\rm OUT}}{2 \cdot V_{\rm BAT}}. \tag{2}$$

In other words, charge pumps are not necessarily efficient even in the ideal case; the efficiency is determined mostly by the ratio of output and input voltages. Equation (2) is a baseline limit that is consistent with what was found by Zhu in [2], and it can be shown to be independent of the duty cycle. Overhead current for the oscillator and other cells further degrade the efficiency. Finally, as shown by Favrat [3], bottom plate parasitic capacitances can be important if the flying capacitor is small, such as in fully integrated systems.

This means that the designed 3.2-V regulated supply created from a battery ranging from 3.5 to 1.8 V has a best-case power efficiency ranging from 46% to 89%.

C. Load Regulation

A plot of the theoretical output voltage versus load current is shown in Fig. 5. Load regulation, also known as output resistance, is a measure of the slope of this curve $(\Delta V_{\rm OUT}/\Delta I_{\rm LOAD})$. The figure shows that good regulation exists for load currents less than a value labeled $I_{\rm LOAD(MAX)}$. The slope (i.e., output resistance) in the regions on either side of $I_{\rm LOAD(MAX)}$ will be derived in this section, as well as general and limiting case expressions for $I_{\rm LOAD(MAX)}$.

First, the output resistance for the region less than $I_{\rm LOAD(MAX)}$ will be derived. From Fig. 4(a) it can be seen that

$$I_{\rm CH} = G_M \cdot (V_{\rm REF} - V_{\rm OUT}). \tag{3}$$

Combining (3) with (1) gives the relationship between output voltage and load current:

$$V_{\rm OUT} = V_{\rm REF} - 2 \cdot I_{\rm LOAD}/G_M \approx V_{\rm REF} \tag{4}$$

and the output resistance is[1]

$$R_{\rm OUT} = \Delta V_{\rm OUT}/\Delta I_{\rm LOAD} = 2/G_M. \tag{5}$$

The output resistance (5) can be made very small, although stability needs to be addressed.

[1]Equation (5) requires the duty cycle to be 50%, and the ripple on C_L to be negligible. A more general equation is $R_{\rm OUT} = 1/(d \cdot G_M) - d/(2 \cdot F_{\rm OSC} \cdot C_L)$, where $F_{\rm OSC}$ is the rate at which the charge is transferred, and d is the percentage of time the circuit is in the charge phase. The negative portion of the impedance is a result of the feedback during the charging phase.

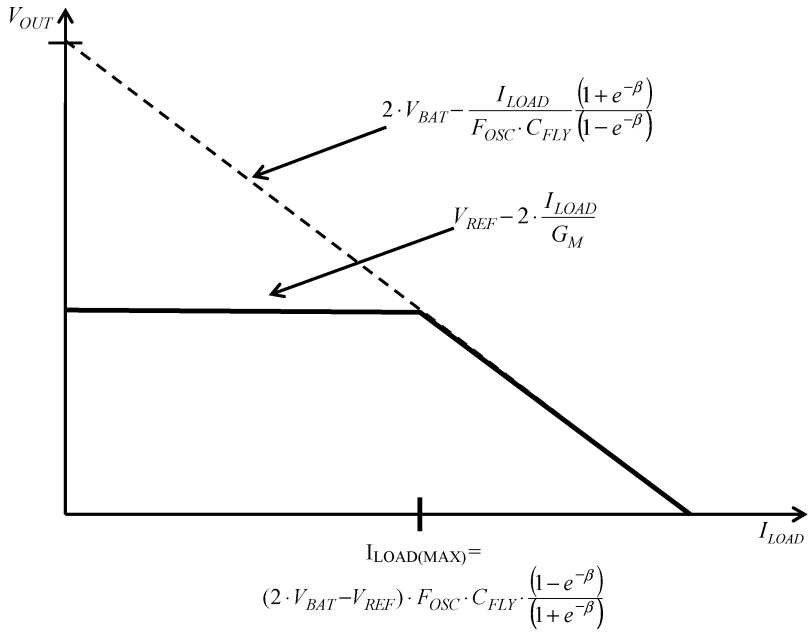

Fig. 5. Theoretical output voltage of regulated charge pump as a function of load current. If load current exceeds $I_{\mathrm{LOAD(MAX)}}$ regulation can not be maintained and voltage must decrease to allow the proper amount of charge to transfer.

If the load is greater than $I_{\mathrm{LOAD(MAX)}}$, regulation is lost, and the output voltage will decrease at a rate much faster than (4) suggests. This is because the transconductance G1 is realized by a transistor operating in the linear region, and there is a maximum amount of charge that can be transferred by C_{FLY} while maintaining the regulated output voltage.

Beyond $I_{\mathrm{LOAD(MAX)}}$ the output voltage is found by finding the maximum amount of charge that can be transferred by C_{FLY} at the oscillator frequency F_{OSC}. This is done by analyzing the voltage across C_{FLY} with the transconductance G1 shorted so that the circuit functions as an unregulated voltage doubler. As can be seen by Fig. 6, the voltage exponentially increases and decreases between V_1 and V_2. The voltage swing is limited by the magnitude of the output voltage and total path resistance R_{SW} (modeled as the battery source resistance, but it also includes the switch resistance and capacitor equivalent series resistance). For simplicity, it is assumed that R_{SW} is the same for both charging and discharging cycles, and that these cycles are of equal duration. Under these conditions, the amount of charge transferred to the load per cycle is

$$\Delta Q = C_{\mathrm{FLY}} \cdot (V_2 - V_1) = I_{\mathrm{LOAD}}/F_{\mathrm{OSC}}. \tag{6}$$

where

$$V_1 = V_2 + (V_{\mathrm{OUT}} - V_{\mathrm{BAT}} - V_2) \cdot (1 - e^{-\beta}) \tag{7}$$
$$V_2 = V_1 + (V_{\mathrm{BAT}} - V_1) \cdot (1 - e^{-\beta}) \tag{8}$$
$$\beta = 1/(2 \cdot F_{\mathrm{OSC}} \cdot R_{\mathrm{SW}} \cdot C_{\mathrm{FLY}}). \tag{9}$$

Combining (6)–(9) results in

$$V_{\mathrm{OUT}} = 2 \cdot V_{\mathrm{BAT}} - \frac{I_{\mathrm{LOAD}}}{F_{\mathrm{OSC}} \cdot C_{\mathrm{FLY}}} \frac{(1+e^{-\beta})}{(1-e^{-\beta})}. \tag{10}$$

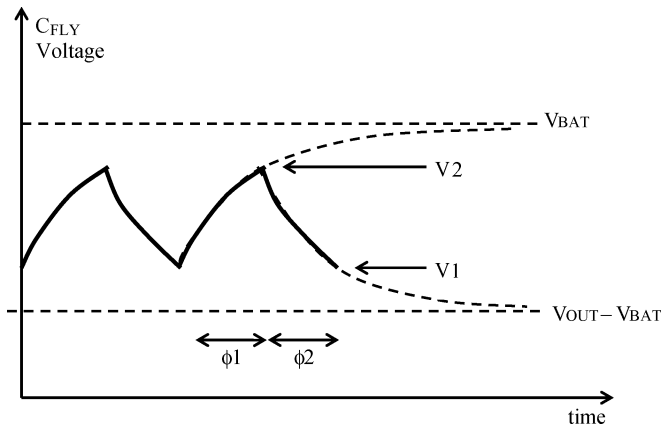

Fig. 6. Flying capacitor voltage when limited by parasitic resistance R_{SW}.

As shown in Fig. 5, the output voltage will be the lesser of (4) or (10). The maximum load current that can be supplied while keeping the output at approximately V_{REF} is found by equating (10) to (4). Its value is

$$I_{\mathrm{LOAD(MAX)}} = (2 \cdot V_{\mathrm{BAT}} - V_{\mathrm{REF}}) \cdot F_{\mathrm{OSC}} \cdot C_{\mathrm{FLY}} \cdot \frac{(1-e^{-\beta})}{(1+e^{-\beta})}. \tag{11}$$

There are two important cases for (11). The first one is $R_{\mathrm{SW}} \ll 1/(2 \cdot F_{\mathrm{OSC}} \cdot C_{\mathrm{FLY}})$. In this case, C_{FLY} is charged fully to V_{BAT} and discharged to $V_{\mathrm{OUT}} - V_{\mathrm{BAT}}$, and the maximum load current that maintains regulation is

$$I_{\mathrm{LOAD(MAX)}} = (2 \cdot V_{\mathrm{BAT}} - V_{\mathrm{REF}}) \cdot F_{\mathrm{OSC}} \cdot C_{\mathrm{FLY}}$$
$$R_{\mathrm{SW}} \ll 1/(2 \cdot F_{\mathrm{OSC}} \cdot C_{\mathrm{FLY}}). \tag{12}$$

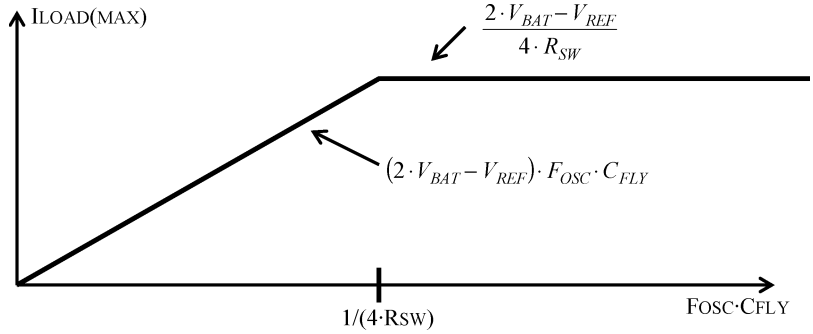

Fig. 7. Maximum load current in which output will maintain regulation as a function of $F_{\rm OSC} \cdot C_{\rm FLY}$. When the time constants are large compared to $F_{\rm OSC}$, the performance cannot be increased with a higher switching rate or larger flying capacitor.

If this is the case, the maximum load current that the circuit can supply can be increased by increasing $C_{\rm FLY}$ or the oscillator frequency $F_{\rm OSC}$; however, as shown by Fig. 7, there is a point of diminishing returns; if $R_{\rm SW} \gg 1/(2 \cdot F_{\rm OSC} \cdot C_{\rm FLY})$ the maximum load current is independent of $F_{\rm OSC}$ and $C_{\rm FLY}$. Under this condition, the maximum load current is[2]

$$I_{\rm LOAD(MAX)} = (2 \cdot V_{\rm BAT} - V_{\rm REF})/(4 \cdot R_{\rm SW}) \qquad R_{\rm SW} \gg 1/(2 \cdot F_{\rm OSC} \cdot C_{\rm FLY}). \tag{13}$$

D. Stability

The circuit in Fig. 3 lends itself to a traditional discrete time analysis rather than the state-space averaging methods used to describe similar charge pump circuits [4]–[6]. Assuming 50% duty cycle, the difference equation solution is

$$V_{\rm OUT}(n) = V_{\rm OUT}(n-1) + \frac{G_M/(2 \cdot F_{\rm OSC})}{(C_{\rm FLY}+C_L)} \times \left(V_{\rm REF} - I_{\rm LOAD} \left(\frac{2}{G_M} - \frac{1}{4 \cdot F_{\rm OSC} \cdot C_L} \right) - V_{\rm OUT}(n-1) \right). \tag{14}$$

$F_{\rm OSC}$ is the clock frequency, and G_M is the feedback transconductance $I_{\rm CH}/(V_{\rm REF} - V_{\rm OUT})$. Using traditional z-domain analysis, the system is stable if

$$\frac{G_M/(2 \cdot F_{\rm OSC})}{(C_{\rm FLY} + C_L)} < 2. \tag{15}$$

Note how (5) and (15) combine and limit the achievable load regulation:

$$R_{\rm OUT} > 1/\left(2 \cdot F_{\rm OSC} \cdot (C_{\rm FLY} + C_L)\right) \tag{16}$$

III. Regulation Using Integral Switched-Capacitor Reference

A. Advantages of Switched-Capacitor References

The continuous time bandgap reference circuit in Fig. 2 could be used with the charge pump in the previous section, but switched-capacitor references [7], [8] have several advantages over continuous-time references. First, the offset of the operational amplifier is cancelled. Second, capacitors match better than resistors. Third, low current (sub-100-nA) references do not require enormous resistors. Finally, charges are summed analogous to the Bamba's current mode reference [9]; therefore, switched-capacitor references do not necessarily require supply voltages greater than the silicon bandgap voltage (approximately 1.25 V).

The disadvantages of switched-capacitor references are that the output is not valid during the time that the operational amplifier offset is being sampled,[3] and that the output cannot be greater than the power supply. The circuit shown in Fig. 8 overcomes these disadvantages while preserving the advantages [10].

B. Reference Operation

Traditional bandgap references add a emitter–base voltage to a proportional-to-absolute-temperature (PTAT) voltage obtained from two PN junctions operated at different current densities. The circuit in Fig. 8 generates the PTAT voltage with a single PN junction by biasing it at different current densities at two points in time similar to that described by Westwick [11] and Gilbert [12]. During phase one, the bipolar is biased at I and during phase two, it is biased at $N \cdot I$. The result (Fig. 9) is a voltage difference of $U_T \cdot \ln(N)$ where U_T is the thermal voltage $k \cdot T/q$. This circuit eliminates the error caused by bipolar mismatch, but the major advantage is the area and power savings. In fact, for low-power devices it may be advantageous to set the duty cycle so that the majority of the time the regulation circuit is in phase one (bipolar biased at I).

The steady-state output voltage is found by doing an analysis of the switched-capacitor network assuming a virtual ground at the inverting node of the opamp:

$$\Delta Q_1 = U_T \cdot ln(N) \cdot C_1 \tag{17}$$

$$\Delta Q_2 = V_{\rm BE} \cdot C_2 \tag{18}$$

$$\Delta Q_3 = V_{\rm OUT} \cdot C_3. \tag{19}$$

If $\Delta Q_3 < \Delta Q_1 + \Delta Q_2$, the voltage at the inverting input of OTA1 will decrease, causing the gate voltage of M2 to ramp at

[2]This is found using the approximation $e^x \approx 1 + x$ for $x \ll 1$.

[3]Johns and Martin claim the circuit in [7] is valid at all times. While this statement is true, the output does have a ripple equal to the offset of the operational amplifier. This ripple does not exist in the presented topology because the charge pump is in the discharge phase while the reference is sampling the amplifier offset.

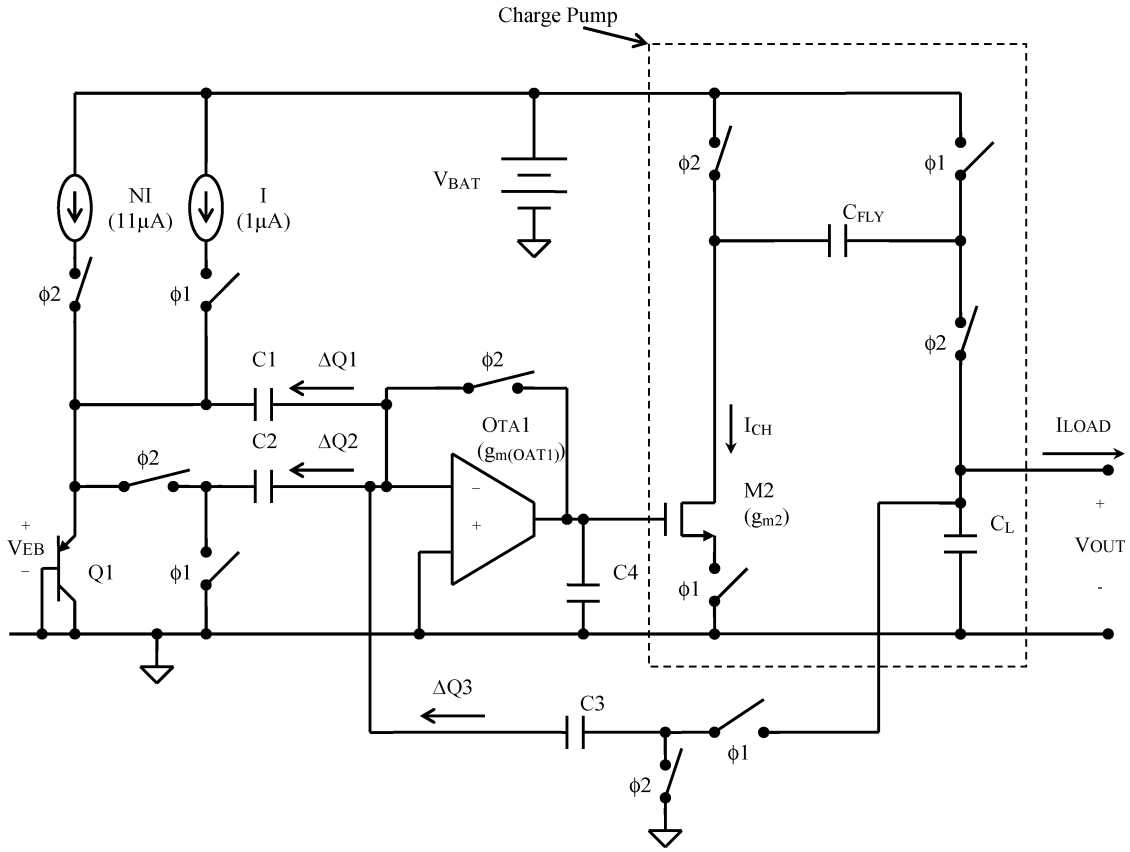

Fig. 8. Switched-capacitor regulation circuitry for a constant frequency charge pump. M2 regulates the amount of charge put on C_{FLY}.

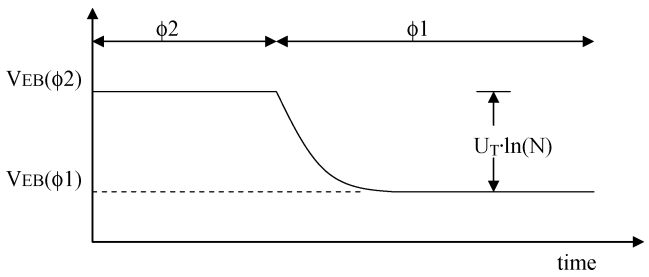

Fig. 9. Emitter–base voltage of Q1 during the two clock phases.

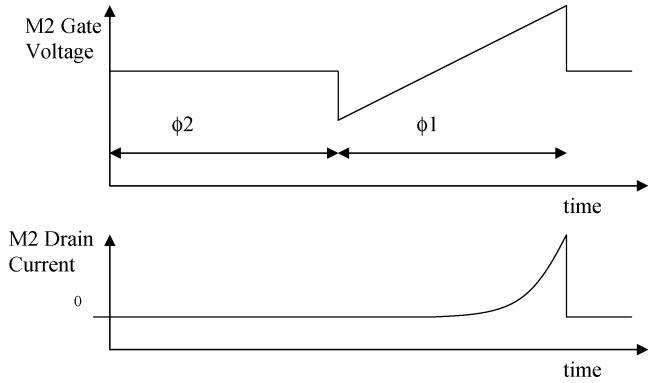

Fig. 10. Gate voltage and drain current of M2 during the discharge/reset $(\phi 2)$ and charge $(\phi 1)$ half-cycles.

a rate proportional to $g_{m(\mathrm{OTA1})} \cdot (\Delta Q_1 + \Delta Q_2 - \Delta Q_3)/C4$, which will turn on M2, charge C_{FLY} with a current I_{CH} proportional to the difference in charge, and increase the output voltage. A hypothetical M2 gate voltage and drain current is shown in Fig. 10. The dip at the beginning of phase one is caused by the gate-to-source capacitance of M2 charging up.

Similarly, if $\Delta Q_3 > \Delta Q_1 + \Delta Q_2$, I_{CH} will be reduced, lowering the output voltage. Accordingly, if the system is stable, the charges must equal each other:

$$\Delta Q_1 + \Delta Q_2 = \Delta Q_3. \tag{20}$$

Combining (17)–(20) gives the steady-state output voltage

$$V_{\mathrm{REF}} = \frac{C_2}{C_3} \cdot \left(V_{\mathrm{BE}} + \frac{C_1}{C_2} \cdot U_T \cdot \ln(N) \right). \tag{21}$$

The loading of C_3 must be taken into consideration if its size is comparable to C_L. The OTA offset is stored onto the capacitors during phase two, and therefore its value is not important if the gain is large enough so that the offset does not change from phase two to phase one.

Notice how the charge pump interacts with switched-capacitor reference, producing an output voltage that is valid at all times. The switched-capacitor reference would not normally be valid during the reset phase $(\phi 2)$, but this time is used to discharge the flying capacitor into the load capacitor. The charge pump behaves as an output stage whose output current is being updated every clock cycle.

C. Feedback Transconductance

The feedback transconductance G_M is the amount of charging current produced by an error in the output voltage; i.e., $G_M = I_{\rm CH}/(V_{\rm REF} - V_{\rm OUT})$. Its value is crucial to the load regulation and the stability of the system. The exact value is very complex because of the ramping nature and initial glitch of the gate voltage of M2, but it is on the order of

$$G_M \sim \frac{C_3}{(C_1 + C_2 + C_3 + C_{\rm PAR})} \cdot \frac{g_{m(\rm OTA1)}/C_4}{(L_{M2}/W_{M2} + L_{M1}/W_{M1}) \cdot F_{\rm OSC}}. \quad (22)$$

$C_{\rm PAR}$ is the parasitic capacitance at the inverting node of OTA1.

D. Control of Temperature Coefficient

Note that in (21), V_{EB} is complementary-to-absolute-temperature (CTAT) and that $U_T \cdot \ln(N)$ is PTAT. Accordingly, ratios of C_1 and C_2 can be chosen to produce an output voltage with a temperature coefficient ranging from pure PTAT to pure CTAT. The former is very useful for temperature sensors, and the latter is often used to bias liquid crystal display drivers.

Of course, the most commonly desired performance is for the output to be independent of temperature—i.e., a bandgap reference response. This requires a ratio of C_1/C_2 in the range of ten. Using multiple PN junctions in series to generate the PTAT reference will reduce this ratio [10], [11].

E. Operational Transconductance Amplifier (OTA)

Because OTA offset is cancelled by the sampling of the switched-capacitor network, a fancy amplifier is not needed to realize OTA1. In fact, a common-source amplifier with a low-voltage regulated cascode [13] to boost output impedance was used (Fig. 11). The 60-μA bias was also a low-voltage regulated cascode, although it is not shown in the figure. The current must be enough to drive the charge pump regulation device (M2, Fig. 8) during the $\phi 1$ half cycle.

Although it was not an issue in the embedded application, the OTA consumes the vast majority of the overhead current in the power supply. To make matters worse, the OTA supply is bootstrapped to the output to provide maximum drive to M2, thus the current draw at the battery is more than 120 μA. A topology that could still drive the gate of M2 with less standby current would be an improvement.

F. Practical Implementation of Charge Pump With In-Rush Current Limiting

The circuit in Fig. 12 is the implementation of the charge pump in Fig. 8. The gate of transconductance device M2 is connected to the output of OTA1. As can be seen by (11)–(13), one needs very large switches to keep $R_{\rm SW}$ small so that the charge pump will supply the required current at the minimum battery input (1.8 V in this case). This creates a problem at start up because the switching transistors (M5 and M11 during $\phi 2$ and M2 and M13 during $\phi 1$) will be saturated until $C_{\rm FLY}$ and C_L charge up. Thus, the initial "in-rush" current will be on the order of $K' \cdot W/L \cdot (V_{\rm BAT} - V_T)^2$. A similar problem occurs if the output is shorted. Unchecked, this current is on the order of 600 mA at maximum battery, which can destroy a bond wire or metal traces.

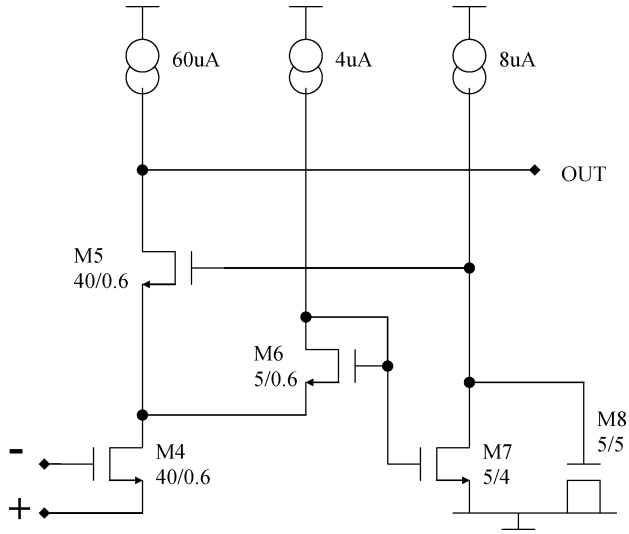

Fig. 11. Detail of common source operational transconductance amplifier with boosted output impedance used in Fig. 8.

The circuit limits this in-rush current differently for $\phi 1$ and $\phi 2$. For $\phi 2$, the gate drive of M11 is controlled robustly by driving it with a diode connected device. When M11 is saturated (the worst case for in-rush current) the pair M9 and M11 act as a simple current mirror, and the current is limited to about $10\ \mu\text{A} \cdot (4000/0.6)/(8/10) = 83$ mA. At low battery (1.8 V), the gate drive of M11 is not limited because the drop across M9 would normally be greater than 1.8 v. The nMOS transistor M12 is not an important contributor to the in-rush current.

Current is limited during $\phi 1$ by the device M1. When the gate drive of M2 is small, M1 is in the linear region and acts as a switch; however, when the gate drive is large, such as during start-up, the drop across the source-drain of M2 will be small and M1 will saturate, allowing the pair M1 and M3 to behave as a current mirror with a current of $10\ \mu\text{A} \cdot (1600/0.6)/(6/10) = 44$ mA.[4] The average current during startup is theoretically $(44\ \text{mA} + 83\ \text{mA})/2 = 63.5$ mA, which compares favorably to the measured 65–74-mA short circuit current.

IV. Support Circuitry

A. Non-Overlapping Clocks

The gate signals $\phi 1$ and $\phi 2$ must not overlap or there will be large current spikes. The standard non-overlapping clock generator in Fig. 13 was used. Note that the large drivers are inside the loop, and not outside where imperfect delay matching may cause clock overlap.

B. Supply for Bulk and Gate Drivers

As shown in Fig. 14, the pMOS device has parasitic substrate PNP devices attached to the source, drain and bulk nodes. If the bulk junction is forward biased, substrate current may cause

[4]Normally, one would make the limiting currents the same for each phase; design constraints prevented this.

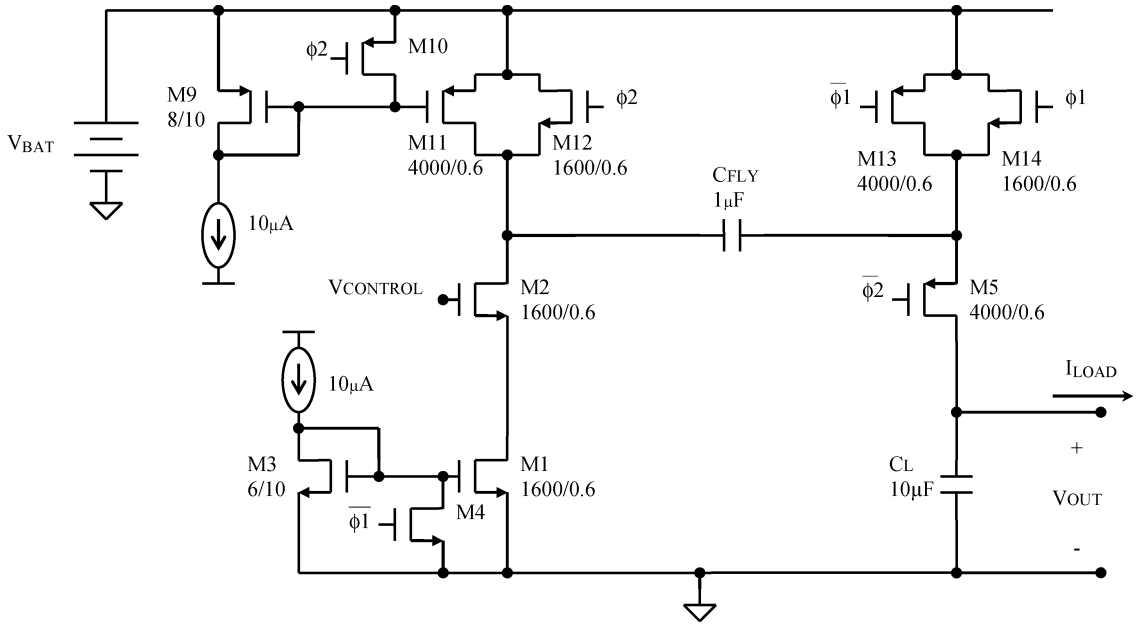

Fig. 12. Schematic of regulated charge pump used in Fig. 8. Current mirrors M9/M11 and M1/M3 limit the in-rush current during $\phi 2$ and $\phi 1$ respectively.

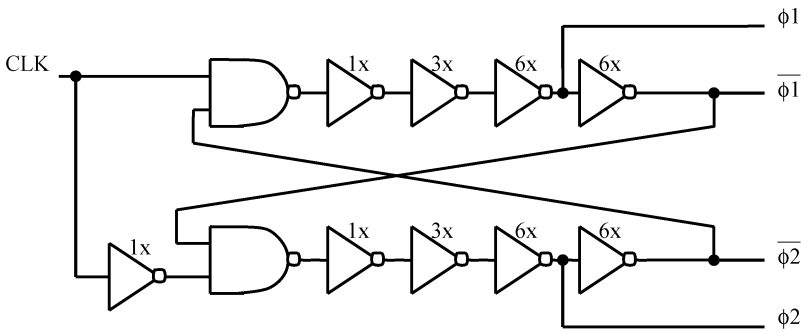

Fig. 13. Circuitry for non-overlapping clock generation. Note that the buffers are inside the loop to guarantee the clocks will not overlap.

latch-up. Traditionally, latch-up is prevented by tying the bulk to the highest supply; however, the battery voltage can range from 1.8 to 3.5 V, and the output voltage ranges from 0 (during startup) to about 3.2 V; therefore, neither the battery nor the output can be guaranteed to the highest voltage at any given time, and special circuitry is needed to prevent latch-up.

The comparator circuit in Fig. 15 is used to sense the higher of the battery $V_{\rm BAT}$ and the output voltage $V_{\rm OUT}$. The higher of the two voltages is switched to the outputs Vhi1 and Vhi2. Vhi1 is used to bias the pMOS bulk nodes in the charge pump and the comparator itself. Vhi2 is used to supply the non-overlapping clock so that the charge pump switches are driven with maximum voltage to minimize their on resistance.

The transistors M12 and M13 provide hysteresis.

The comparator circuit cannot draw any current when the charge pump is powered down so M4–M6 force the outputs to be switched to the battery when in this state. Unfortunately, the charge pump output may be higher than the battery immediately after it is powered down because the charge has not been bled from C_L yet. To get around this problem, when the charge pump is in the power-down state, its output is compared to the battery voltage using the simple nor gate shown in Fig. 16. The gate keeps the comparator powered up until the charge pump output is approximately a threshold voltage below the battery voltage.

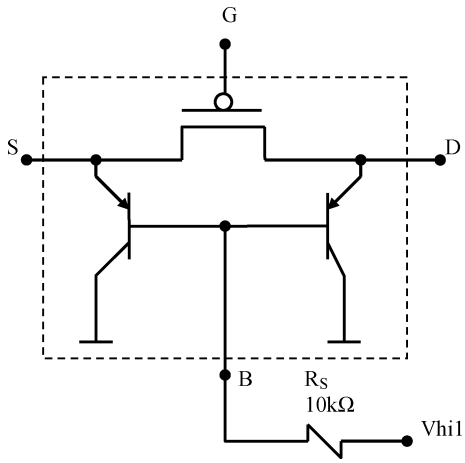

Fig. 14. PMOS equivalent circuit showing parasitic substrate PNPs. Rs is a polysilicon resistor to limit the current if the bulk junction gets forward biased. Vhi1 is the higher of the output or the battery voltage.

In addition to using the comparator to bias the bulk at the highest potential, each of the large devices ($W > 100$) had a

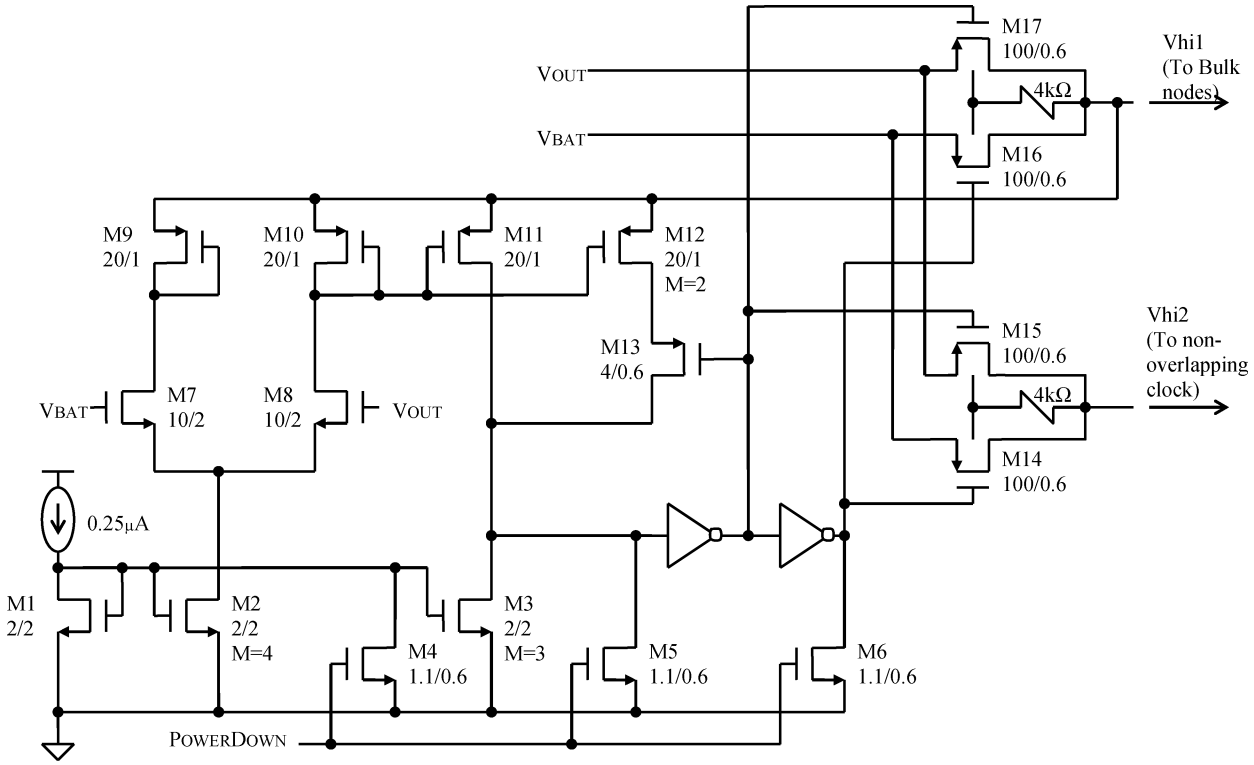

Fig. 15. Comparator circuit to bias logic and bulk voltages at the higher of the output voltage or the battery voltage. The inverters and the bulks of pMOS devices M9–M13 are connected to Vhi1.

resistance in series with its bulk that limited the pnp base current in the event that the bulk node was inadvertently forward biased because of the slow comparator response time in a fast event such as a short.

V. Measured Results

The charge pump described in Fig. 8 was implemented in a 0.5-μm C5 process with double poly capacitors. It is used in a handheld medical meter operating from two AAA batteries. Off current for the charge pump needed to be limited to less than 10 nA. When turned on, the charge pump needed to provide a 3.2-V supply to the whole ASIC, which contained an 8051 microprocessor as well as extensive analog circuitry, and consumed as much as 6 mA.

A. Line Regulation

A typical plot of output voltage versus load current with $V_{\rm BAT} = 1.85$, 2.0, and 2.5 V is shown in Fig. 17. Note that, as the theoretical curve shown in Fig. 5 predicts, there are roughly two regions with $I_{\rm LOAD(MAX)}$ being roughly 6 mA when $V_{\rm BAT} = 1.85$ V. At a battery voltage of 1.85 V, the regulation is good (20 mV/mA) for currents less than 6 mA. For currents greater than 6 mA the flying capacitor cannot transfer sufficient charge without decreasing the output voltage. In this region the regulation is much worse: about 120 mV/mA.

The theory presented in Section II predicts that the slope of the line in the region greater than $I_{\rm LOAD(MAX)}$ will extrapolate back to $2 \cdot V_{\rm BAT} = 3.7$ V at $I_{\rm LOAD} = 0$ mA. The actual intersection is about 3.8 V, which is a reasonable fit with the theory. As predicted by (11), and shown by the two other curves in Fig. 17, the performance improves when the battery voltage is increased.

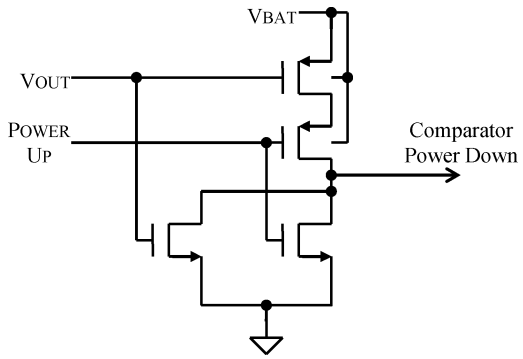

Fig. 16. Nor gate used to ensure that bulk bias comparator is not powered down before $V_{\rm OUT}$ is lower than $V_{\rm BAT}$.

B. Output Tolerance

The unloaded output voltage three-sigma tolerance is about one percent for die on the same wafer. This is much lower than a typical continuous time bandgap reference because opamp offset is not a factor in this design, and capacitor mismatch is less than resistor mismatch. The wafer-to-wafer deviations have two additional error sources: variations in the sheet resistance used to generate the PNP bias, and bipolar saturation current (IS). These additional variations can be expected to add between one and two percentage points to the overall tolerance. Even so, an untrimmed power supply with a tolerance on the order of 3 percent is very good.

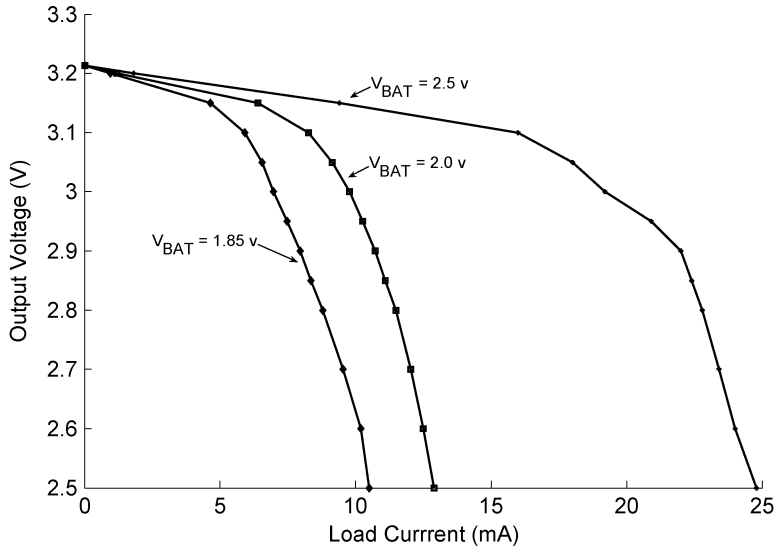

Fig. 17. Measured output voltage as a function of load current with $V_{\rm BAT} = 1.85$, 2.0 and 2.5 V.

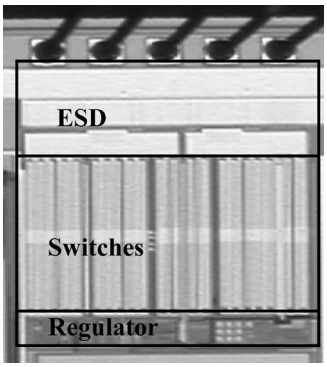

Fig. 18. Micrograph of the regulated charge pump.

TABLE I
MEASURED PERFORMANCE SUMMARY OF THE CHARGE PUMP

Output (unloaded)[a]	3.200 ± 0.036V
Output (6mA Load)[a]	3.144 ± 0.057V
Load Regulation	9.3mV/mA
Input Voltage	1.8 – 3.5V
Line Regulation	11mV/V
Temperature Drift[b]	-4mV
Flying Cap	1μF
Load Cap	10μF
Switching Frequency	90kHz
Size[c]	640x820 μm^2

[a] 3 Sigma numbers, single wafer, V_{BAT} = 1.9v, T=30C, 340 parts measured.
[b] –35°C to 5°C (Peak at 5°C: curvature typical of a traditional bandgap reference.)
[c] The five bond pads and switches constitute 90% of overall area (see Fig. 18).

C. Summary of Measured Results

A summary of the measured performance is given in Table I.

VI. CONCLUSION

A DC-to-DC converter was designed and embedded into an ASIC to create its own 3.2 V, 6 mA supply from a battery input ranging from 1.8 to 3.5 V. The presented circuit is considerably more compact than the traditional circuit shown in Fig. 1 because it incorporates a switched capacitor reference into the regulating loop. Furthermore, the amplifier offset is cancelled by the switched-capacitor network, which allows a simple common source amplifier to replace the two precision amplifiers in Fig. 1.

The switched-capacitor topology generates the reference in the charge domain so it is not limited to supplies greater than one volt. Temperature dependence of the output voltage is controlled by capacitor ratios and can range from CTAT to PTAT. The design limited the short circuit current and the start up "in-rush" current to about 65 mA.

Load regulation is twice the feedback transconductance as long as the flying capacitor can transfer sufficient charge to satisfy the load current. For loads greater than this maximum load current $I_{\rm LOAD(MAX)}$, load regulation is much worse, and under the best conditions the slope will extrapolate to approximately $2 \cdot V_{\rm BAT}$ at $I_{\rm LOAD} = 0$. Maximum load current is determined by the flying capacitor value if the switches are very large so that the *RC* time constants are small compared to $1/F_{\rm OSC}$. If the *RC* time constants are comparable, then maximum load current is almost entirely determined by the combination of the switch and battery source resistances.

The difference equation for the output voltage was presented, allowing the stability criteria to be determined. Stability requirements limit the load regulation for a given oscillator frequency and capacitor values.

The battery current for a regulated voltage doubler will be about twice the load current, and this largely determines the efficiency

ACKNOWLEDGMENT

The author would like to thank Dr. Hoi Lee of the University of Texas at Dallas for pointing out H. Chung's work with quasi-switches. This work was done for AMI Semiconductor.

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