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# A DIGITALLY CONTROLLED ON-CHIP MONOTONIC REFERENCE CURRENT GENERATOR WITH LOW LSB CURRENT FOR FAST AND ACCURATE OPTICAL LEVEL MONITORING

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**KEYWORDS*:* GPON, Current reference DNL, Bandgap voltage**

**ABSTRACT**: This paper describes a digitally controlled on-chip monotonic reference current generator with 8-bit resolution and a LSB (Least Significant Bit) current as low as 100 nA. It was designed as a building block of a generic DC-coupled Burst Mode Laser Diode Driver (BM-LDD) for GPON (Gigabit Passive Optical Network) applications and acts as an on-chip reference current generator with a settling time of 18 ns for fast and accurate optical level monitoring with guaranteed monotony. The proposed architecture of the on-chip reference current generator is based on an 8-bit segmented current-steering Digital-to-Analog Converter (IDAC) and a bandgap voltage reference. The bandgap voltage reference deviates only 0.6% of the nominal value over temperature and power supply variations. A cascade current mirror with a super beta helper circuit is used to guarantee monotony and high accuracy. The linearity errors caused by systematic influences and random variations are reduced by the proposed 2-D double centroid symmetrical architecture. The design was realized in a 0.35 μm SiGe BiCMOS technology with 3.3 V power supply.

## INTRODUCTION

A Burst Mode Laser Diode Driver (BM-LDD) is one of the key building blocks of a GPON (Gigabit Passive Optical Network) ONU (Optical Network Unit) [1]. This requires an on-chip monotonic reference current generator with high resolution of 100 nA. The BM-LDD consists of a 1.25 Gbit/s burst-mode laser driver stage, optical level monitoring, pattern detection, dual-mode (fast/slow) digital APC (Automatic Power Control) algorithm and SPI interface logic [2]. The task of the optical level monitoring circuitry of the BM-LDD is to compare the photodiode current generated by a laser back facet monitor photodiode with a preset reference current [2], [3]. Since the monitoring diode acts as a current source, it is straightforward to use a digitally controlled on-chip current generator as the reference. Due to the high-accuracy requirement of the level monitoring circuitry, and its associated closed-loop digital APC algorithm, monotony is a very important design specification, especially during the calibration of the level monitoring, of the on-chip reference current generator besides design goals concerning die area and speed. The proposed reference current generator has an 8-bit resolution, which is required by the target monitor current range. Since the laser back-facet photodiode currents to be measured are very weak, a low LSB (Least Significant Bit) output current of 100 nA is required for the current reference. Another important design requirement for the reference current generator is a high independence of the monotonic output current from wide ambient temperatures (-40°C to 85°C for outdoor operation), high power supply variations (battery backup requirement) and process parameters.

The novelty of this work is the fact that previous (GPON) laser drivers or commercial components [4] use external components to set the required reference currents for the APC of the laser driver. Former paper [5] shows a concept to develop a current reference generator with a high accuracy but its speed is much slower than our design requirement. Among most of recent reference publications on fast and accurate reference current generator describing previous works, there is no better combination than 100 nA accurate LSB current with 18 ns fast settling time and guaranteed monotony. Using a digitally controlled on-chip monotonic reference current generator together with an intelligent digital APC algorithm [6] eliminates conventional external trimming for current settings as well as reduces the cost of temperature dependent calibrations.

## PROPOSED ARCHITECTURE

The proposed architecture of on-chip reference current generator is shown in Fig. 1, and is based on an 8-bit segmented current-steering Digital-to-Analog Converter (IDAC) and a bandgap voltage reference. An external fixed resistor combined with the bandgap voltage reference provides an accurate reference current for the IDAC. The IDAC has a (3+5) segmented architecture that is an optimum combination of a 3-bit MSBs (Most Significant Bits) unit-element sub-DAC and a 5-bit LSBs binary-weighted sub-DAC for good DNL (Differential Nonlinearity) performance. The output current is accurately regulated by the digital setting codes. The nominal bandgap reference voltage is 1.765 V and by carefully adjusting the resistance of external resistor $R_{ext}$ one can obtain a target reference current equaling:

 

$$I_{\mathrm{Re}f} = V_{Bandgap} / R_{Ext} = 3.2\mu\mathrm{A} \qquad (1)$$

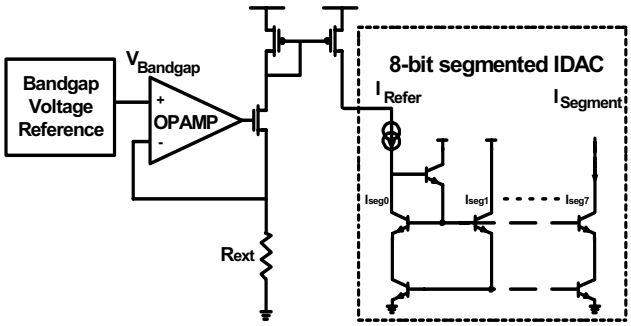


*Fig. 1. Proposed architecture of on-chip reference current generator*

## IDAC ARCHITECTURE

In our application, Differential Nonlinearity (DNL) is much more important than Integral Nonlinearity (INL) because monotonic stepping of the accurate reference current with the digital input code has to be guaranteed to preserve stability of the BM-LDD level monitoring algorithm during calibration.

An IDAC with a unit-element architecture has a guaranteed linear behavior and therefore a small DNL error. A major disadvantage of the unit-element architecture is its complexity, needing many current sources, many current switches and a complex routing. In a binary-weighted IDAC implementation, every switch switches a current to the output that is twice as large as the next LSB. The advantages of this architecture are simplicity and so a smaller silicon area. Unfortunately, a large DNL error and an increased dynamic error are intrinsically linked with this architecture. To get the best of both worlds, the two previous architectures are often combined into what is called a segmented architecture [7], where an N-bit DAC is divided into two sub-DACs: M less significant bits are implemented in a binary-weighted architecture while the (N-M) more significant bits are implemented in a unit-element architecture. The optimum balance among monotony, silicon area and complexity can be found by selecting the value M correctly.

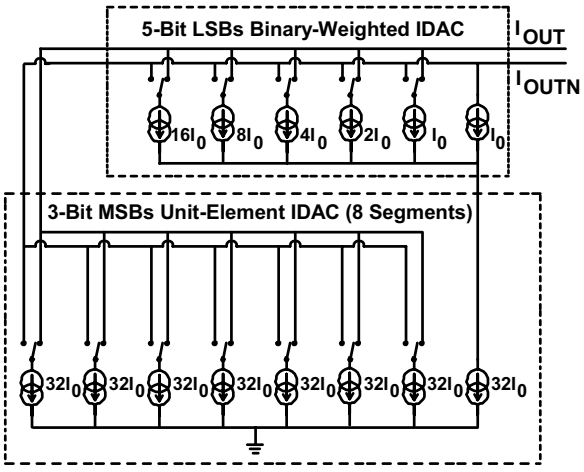


*Fig. 2. Segmented architecture of the 8-bit IDAC*

The architecture of the proposed IDAC is shown in Fig. 2. $I_0$ is the unit current and every segment current is made up of 32 times of $I_0$. This (3+5) segmented structure, instead of (2+6), (4+4) and so on, is selected as an optimum balance between DNL and silicon area based on DNL simulation results. Although several transistors are stacked on top of each other in the segmented IDAC schematic, the limited output voltage range won't bring extra disadvantages because the IDAC output current is fed into a PMOS current mirror in the level monitoring block of the BM-LDD.

Figure 3 shows the simplified block diagram of the 8-bit segmented IDAC. It mainly consists of a 16X16 current sources matrix, a thermometer decoder, and latch arrays. The description on architecture design is mainly focused on the segment current sources matrix. The pattern of the current sources matrix is designed for good matching, and will be described in detail in Section 5.

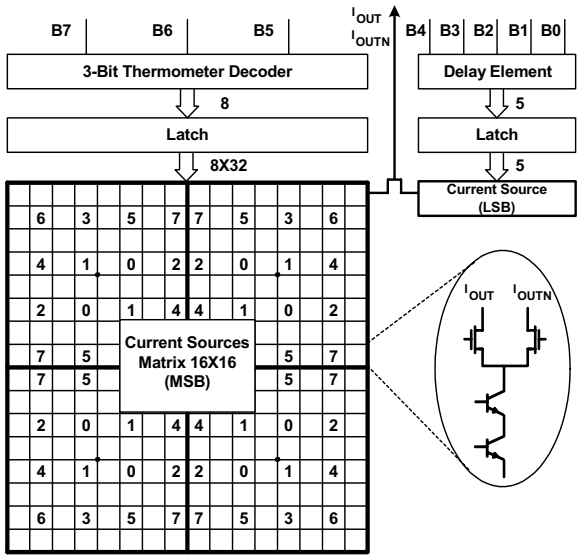


*Fig. 3 Simplified block diagram of the 8-bit segmented IDAC*

## CIRCUIT DESCRIPTION

### Bandgap Voltage Reference

In order to provide a stable reference current for the 8-bit IDAC, the voltage reference should show negligible dependence upon ambient temperature, power supply and process parameters. Therefore, the reference voltage is provided using a bandgap circuit, which is the best method known to create a stable voltage that does not depend on process parameters, temperature and power supply variations.

A bandgap voltage is created by adding together a voltage with a positive temperature coefficient and a voltage with a negative temperature coefficient. The positive temperature coefficient is derived from the difference between the base-emitter voltages of two bipolar transistors operated at different current densities. The negative temperature coefficient is derived from the base-emitter voltage of a bipolar transistor. To reduce the effect of operational amplifier

dc-offset, two base-emitter voltages were stacked, see Fig. 4. The output voltage can be written as:

$$V_{OUT} = 2V_{BE} + 2\left(1+\frac{R_2}{R_3}\right)\frac{kT}{q}\ln(mn) \qquad (2)$$

where $R_2$, $R_3$, m and n are defined in Fig. 4. Aggressive scaling of both m and n was used to decrease the influence of the dc-offset of the operational amplifier even further. In the final design, m was set equal to 4 and n was 36. The topology of the operational amplifier was selected specifically for low input-referred offset. It consists of a resistively loaded bipolar differential input pair, followed by a PMOS differential gain to raise the overall gain of the operational amplifier.

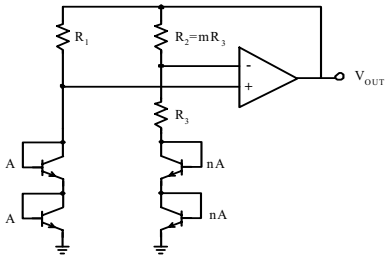


*Fig. 4 Bandgap voltage reference*

## Cascade Current Mirror with Super Beta Helper

It should be mentioned that the SiGe BiCMOS process was chosen to satisfy the primary requirements of a generic DC-coupled 1.25 Gbit/s GPON BM-LDD chip. Though pure CMOS is fast enough for 8bit DAC with 18ns settling time, as mentioned for designing a generic and low cost ONU of GPON systems with outstanding performance by using all gigabit speed laser diode types available on the market, not only settling time but also low LSB current, and high accuracy, as well as guaranteed monotony are all very important design specifications. The combination of these strong requirements made our design non-conventional. Bipolar transistors, available in the BiCMOS process were chosen in order to obtain better matching parameters and due to their more reliable models at very small currents.

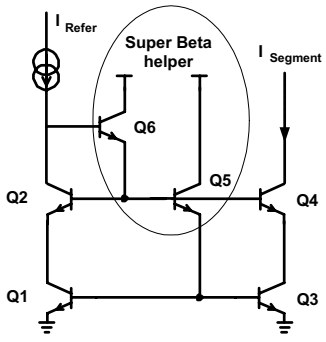


*Fig. 5 Cascade current mirror with super beta helper*

In Fig. 5, transistors Q1, Q2, Q3 and Q4 form a simple NPN cascade current mirror. Comparing with the single transistor current source, the cascade connection can achieve a very high output resistance and a good matching to improve DNL. The physical size of the NPN transistors that act as the IDAC current mirror is decided by the matching requirement that can ensure monotonic behavior (see section 5 in detail). However the physical size of the NPN transistors is also important to obtain a very low LSB current because the transistor current gain beta might degrade when bipolar transistors are operated in a low current.

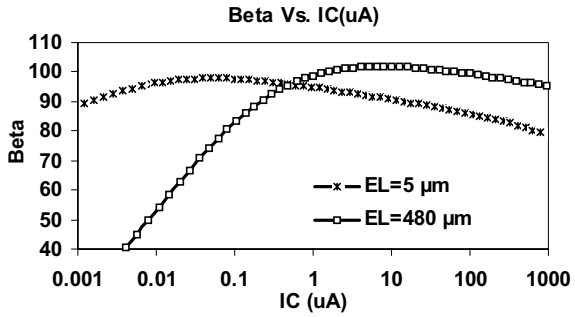


*Fig. 6 Beta Vs. IC of NPN transistor*

Figure 6 shows the typical curve of beta versus collector current IC. The designed segment current for 3-bit MSB unit-element sub-DAC is $32I_0$ (see Fig. 2) = 3.2µA and the designed LSB current for 5-bit LSB binary-weighted sub-DAC is $I_0$ (see Fig. 2) = 100 nA. With an EL (Emitter Length) = 480 µm for the bottom current mirror (Q1 and Q3) of the 3-bit MSBs sub-DAC and an EL = 5 µm for the current mirror of the 5-bit LSBs sub-DAC, the curve in Fig.6 shows that the NPN transistors of the current mirror work in the mid-current region, where the current gain is high and approximately constant, instead of in the low-current region.

Bipolar transistors together with a super beta helper were used for the on-chip reference current generator to guarantee monotony and accuracy especially at small currents. A beta helper circuit is required for base current compensation. The proposed beta helper circuit, called a "super beta" helper circuit, uses two NPN transistors (Q5 and Q6 in Fig. 5), instead of one NPN transistor, to reduce the influence of base current on the output segment current.

$$I_{Segment} = (1-\varepsilon)I_{\mathrm{Re}\,fer} \qquad (3)$$

Note that $\varepsilon$ represents the gain error of the current mirror.

TABLE 1. Comparisons of gain error

| | **Gain error ($\varepsilon$)** | **Gain error for $\beta$=100** |
|---|---|---|
| Simple cascade current mirror | $\frac{4\beta+2}{\beta^2+4\beta+2}$ | 3.865% |
| Cascade current mirror with beta helper | $\frac{2\beta}{\beta^2+3\beta+2}$ | 1.941% |
| Cascade current mirror with super beta helper | $\frac{\beta+2}{\beta^2+2\beta+2}$ | 0.998% |

Formula (3) describes the relation between the input reference current ($I_{Refer}$) and the output segment current ($I_{Segment}$). To simplify the calculation, we assume that all NPN transistors have the same size and beta. Table 1 compares the simple cascade current mirror, the cascade current mirror with beta helper and the cascade current mirror with super beta helper.
Not only is the super beta helper important for the accuracy of the IDAC, it also has a great benefit for the stability of the IDAC output current, allowing the IDAC to provide the level monitoring block with a stable reference current even though the die temperature or power supply voltage changes.

## Latch, Switch and Voltage Buffer

The dynamic performance of a current-steering DAC depends strongly on the properties of the latch and current switch. To minimize the settling time of the DAC, a well-designed latch and two-way switch with a voltage buffer is used. The voltage buffer consists of a simple PMOS differential pair with unity-gain feedback. It sinks the current and serves the same purpose as the buffer in reference [8] although that buffer sources the current. The current is switched between 2 NMOS transistors, as controlled by the latch at the left hand side of Fig. 7. The major function of this latch is reducing the cross-point voltage of the switch transistor differential control signals (Sel and the inverted Sel), in such a way that these transistors are never simultaneously in the off state. By doing so the voltage swing at the collector of the current source is reduced during switching. This swing must be limited because the current source has a considerable capacitance, since the transistors are chosen relatively big to achieve a good matching. We further reduced the settling time by using a unity-gain buffer to make the voltage at $I_{OUTN}$ equal to the voltage at $I_{OUT}$. This makes a considerable difference because $I_{OUT}$ is fed into a current mirror of which the input voltage varies with the current. The unity-gain buffer guarantees that the voltage at $I_{OUTN}$ equals the voltage at $I_{OUT}$ so that parasitic capacitances charge or discharge less when switching.

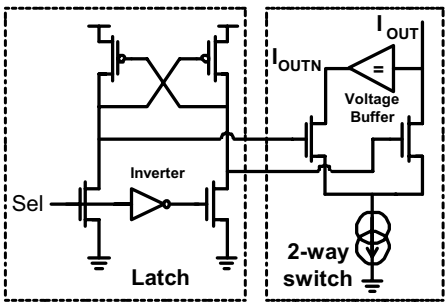


*Fig. 7. Latch and two-way switch with voltage buffer*

## DOUBLE CENTROID SYMMETRICAL LAYOUT

Current-mode DACs inherently suffer from static linearity errors due to systematic influences and random variations. Systematic mismatches originate from process biases, contact resistances, non-uniform current flow, temperature gradients, mechanical stresses and a host of other causes. Random mismatches come from microscopic fluctuations in dimensions, doping, silicon oxide thickness gradients and other parameters that influence component values.

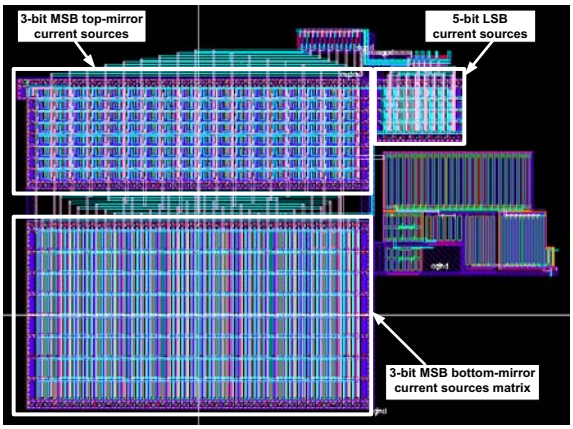


*Fig. 8. Layout of the realized 8-bit segmented IDAC*

The conceptual diagram of the 2-D double centroid symmetrical current sources matrix was presented in Fig. 3 and the layout of the realized 8-bit segmented IDAC is shown in Fig. 8. The 3-bit MSB bottom-mirror current sources matrix contains the bottom group NPN transistors of the cascade current mirror, and the top-mirror current sources matrix contains the top group NPN transistors of the cascade current mirror. The two matrices follow the same layout methodology.
To achieve good matching, a double centroid symmetrical architecture with identical unit transistors is selected. The 16X16 current sources matrix (Fig. 3) is made up of 4 centroid symmetrical quadrants and each of the quadrants is an 8X8 centroid symmetrical matrix too. A double centroid architecture surrounded in a perimeter with dummy cells can minimize graded errors and compensate hierarchical errors. It is also necessary to select the LSB current cell as the unit transistor, because then all tail current sources can be built by assembling identical transistors, minimizing systematic errors. Since each segment current is 32 times as big as the LSB current, one segment current source is made of 32 unit transistors in parallel. This requires 256 unit transistors in total for the 8 segment current sources. Every four unit-transistors are combined by local routing into a block-transistor in which most of inter-routing can be done inside the matrix, saving a considerable silicon area and layout effort.
The latches and the switches are placed in a separate array from the current sources. This is done to avoid coupling between the digital signals and the analog output signal. Another advantage of these separate arrays is that the layout area of a unity cell in the current source array can be minimized. In this way, the distances between the transistors are reduced, resulting in improved matching properties. Furthermore, digital coupling through the substrate has been reduced by the intensive use of substrate contacts and guard rings. To

minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors, sufficiently wide lines have been used. Special care has been taken to realize a symmetrical interconnection array in order not to degrade the matching performance. Throughout the whole design, layout parasitics have been taken into account. They have been manually extracted at each critical node and iterated in the electrical simulations. Good matching figures are obtained with a unit transistor of non-minimum size, for the bottom current mirror EL (Emitter Length) = 15 µm and for the top current mirror EL = 5 µm, compromising DNL, accuracy and area.

## EXPERIMENTAL AND SIMULATION RESULTS

Our proposed on-chip reference current generator has been fabricated in a 0.35 µm SiGe BiCMOS process and successfully tested. Figure 9 shows the die micrograph of the BM-LDD chip. The die sized 4 by 4 mm is housed in a 68-pin VFQFPN package, and each 8-bit IDAC has an active silicon area of 0.16 mm2.

The monotony of on-chip reference current generator was measured via the test pin of the chip at room temperature. The measurement procedure was automated in a LabView platform and via the chip Serial Peripheral Interface (SPI). The output voltage converted from the output current through a load resistor was measured with a high-resolution multi-meter. Figure 10 shows the measured DNL between –0.182 LSB and 0.452 LSB. The DNL is smaller than 0.5 LSB, which proves the required monotony. The peak of errors appears every 16 codes because the mismatch of 16 times of $I_0$, being the MSB of the binary weighted part, dominates the non-linearity. Every 32 codes during the transition from digital input pattern "XX011111" to "XX100000", the biggest peaks occur, because the mismatch of the segment current (32 times of $I_0$) and the mismatch of 16 times of $I_0$ both contribute to the DNL. And Figure 11 shows the measured INL between –0.267 LSB and 0.768 LSB.

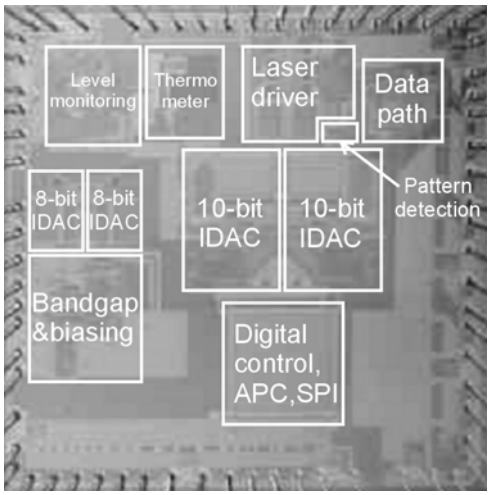


*Fig. 9. Die micrograph of BM-LDD chip*

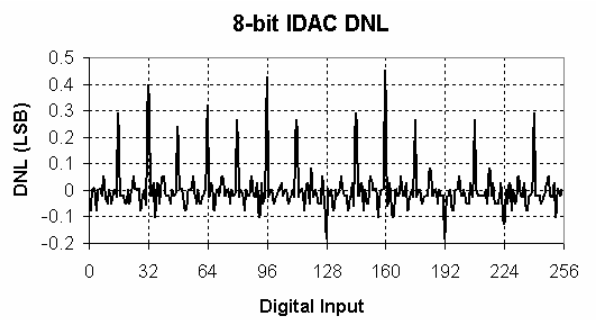


*Fig. 10. Measured DNL of the 8-bit IDAC*

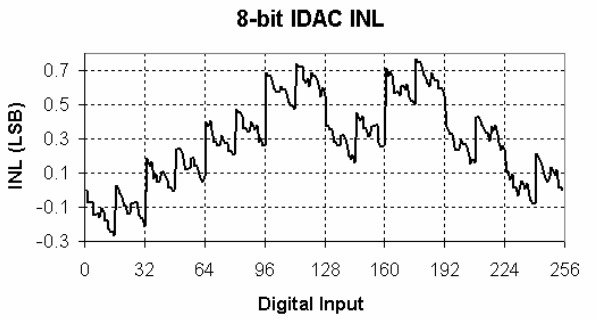


*Fig. 11. Measured INL of the 8-bit IDAC*

TABLE 2. Simulation results about accuracy

| $I_{Refer}$ (µA) | $I_{Segment}$ (µA) | $I_{LSB}$ (nA) | Δ I (nA) |
|---|---|---|---|
| 3.21253 | 3.21154 | 100.2 | 0.992 |

Table 2 gives some simulation results about the accuracy. The LSB current of the on-chip current reference can be as low as 100 nA. The difference between $I_{Refer}$ and $I_{Segment}$ is smaller than 1 nA, which is negligible compared to the 100 nA LSB current.

Simulations of the output current temperature and power supply independence show an output current variation of 0.156% for the cascade current mirror with super beta helper, instead of 3.5% for the cascade current mirror with general beta helper. The results prove the importance of the super beta helper for the temperature and supply independence of the IDAC output current.

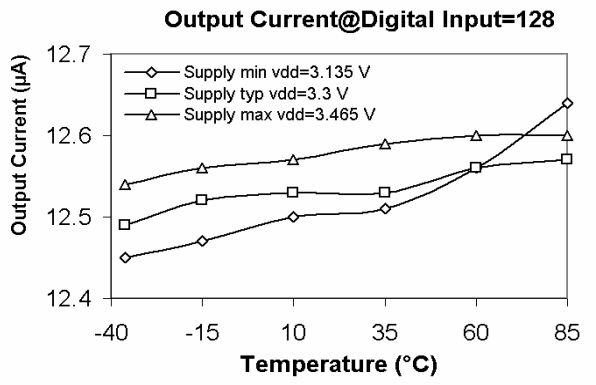


*Fig. 12. Output current vs. ambient temperature and power supply*

Figure 12 shows the measured output current from an experiment changing both the ambient temperature (–40°C ~ +85°C) and the power supply voltage (3.135 V, 3.3 V and 3.465 V). The 8-bit digital input was set to 128, which corresponded to 12.53 μA at 35°C and 3.3 V power supply. The variation of the output current is 0.19 μA over the full temperature and supply range.

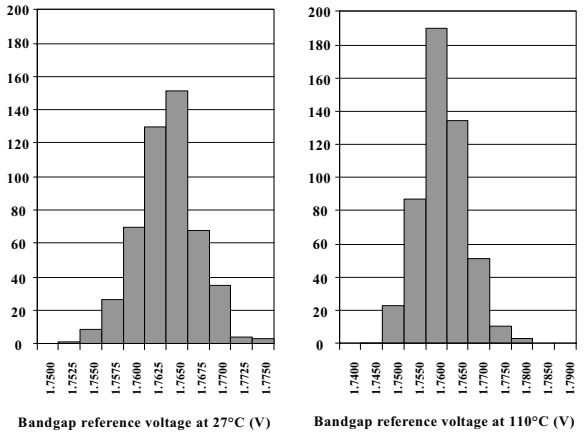


*Fig. 13. Histograms of the bandgap reference voltage*

Figure 13 displays histograms of the output voltage of the bandgap reference, obtained from a Monte Carlo simulation (500 runs). At room temperature the reference voltage is 1.765 V +/- 0.6 %. The worst-case variation occurs at a die temperature of 110°C, the reference voltage is then 1.761 V +/- 0.9 %. This is true for 99.7 % of all produced devices. Figure 14 shows that the measured bandgap reference voltage is very stable over the ambient temperature and power supply variations. It changes only 10.5 mV, which is 0.6 % of the nominal value.

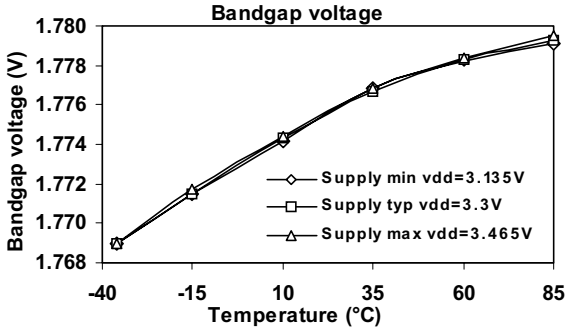


*Fig. 14. Bandgap voltage vs. ambient temperature and power supply*

By performing simulations that sweep all corners of temperature, process and power supply, and taking into account the parasitic capacitances due to interconnections, the settling time of the reference current generator was determined to be 18ns. This was sufficient to reach the requirement of fast level monitoring.

## CONCLUSION

An 8-bit monotonic on-chip reference current generator with a LSB current as low as 100 nA was developed and tested successfully. A bandgap voltage reference was designed to provide a stable on-chip reference voltage. A cascade current mirror with super beta helper circuit was proposed to improve monotony and accuracy despite the low LSB current and despite temperature and power supply variations. The layout parasitic effects were iterated into the design phase, and the routing strategy of the analog block has also been studied to minimize the chip area. Experiments confirm a DNL of ± 0.5 LSB and simulation results show a settling time of 18 ns, which validate the effectiveness of the design strategy from topology selection and circuit design till centroid layout.

## THE AUTHORS

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## REFERENCES

[1] X.Z. Qiu, et al., "Development of GPON Upstream Physical Media Dependent Layer Prototypes", IEEE J. Lightwave Technol., Vol. 22, pp. 2498-2508, Nov. 2004.

[2] J. Bauwelinck, et al., "A high-resolution burst-mode laser transmitter with fast and accurate level monitoring for 1.25 Gb/s upstream GPONs," IEEE J. Solid-State Circuits, vol. 40, pp. 1322-1330, June. 2005.

[3] J. Bauwelinck, et al., "Current Mode Circuits for Fast and Accurate Optical Level Monitoring with Wide Dynamic Range", IEICE Trans. Communications, Vol.E87-B No.9, pp.2641-2647, Oct. 2004.

[4] MAX3656, 155 Mbps to 2.5 Gbps Burst-Mode Laser Driver, Data Sheet, Maxim Integrated Products, Inc., Sunnyvale, CA, 2003.

[5] J.S. Wang et al., "Design and Analysis of High Performance Current Reference Generators for Low-Power CMOS Data Converters," IEEE Trans. Circuits Syst. II, vol. 46, pp. 647-652, May. 1999.

[6] D. Verhulst, et al., "A Fast and Intelligent Automatic Power Control for a GPON Burst-Mode Optical Transmitter", IEEE Photon. Tech. Lett., vol.17, pp. 2439-2441 Nov. 2005.

[7] C.H. Lin et al., "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2", IEEE J. Solid-State Circuits, vol. 33, pp. 1948-1958, Dec. 1998.

[8] J. Bauwelinck, et al., "Low-output-impedance BiCMOS voltage buffer," IEICE Electron. Express, vol. 1, pp.34-38, Apr. 2004.