A Sub-1 V Low-Noise Bandgap Voltage Reference

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***Abstract* – A sub-1 V bandgap voltage reference is presented. The topology allows the reference to operate with a low voltage supply by employing reverse bandgap voltage generation. It also has an attractive low-noise output without the use of a large external filtering capacitor. Theoretical analysis and experimental results show the output noise spectral density is 40 nV/√Hz with a peak-to-peak output noise in the 0.1 to 10 Hz band of 4 µV. The reference has a mean output voltage of 190.9 mV at room temperature. The temperature coefficient of the reference voltage in the –40 to +125 °C range is 11 ppm/°C (mean) with a standard deviation of 5 ppm/°C. The design is compatible with most CMOS and BiCMOS fabrication processes.**

I. Introduction

A voltage reference is a key building block in analog and mixed-signal circuits such as analog-to-digital converters, digital-to-analog converters, DC-DC converters, and LDO regulators. One of the best existing references is the bandgap voltage reference [1]. The reference voltage is created by adding a forward-biased diode voltage (V_{BE1}), which has a negative temperature coefficient (TC), to the scaled difference between two forward-biased diode voltages ($M*[V_{BE1}-V_{BE2}] = M*V_T*ln[(I_{C1}/I_{C2})*(Area_2/Area_1)]$), which has a positive-TC, to yield a 1st-order temperature-independent voltage. The output is approximately equal to the bandgap voltage of silicon extrapolated to zero degrees Kelvin, and it is expressed as

$$V_{REF} = V_{BE1} + M * V_T * \ln\left(\frac{I_{C1}}{I_{C2}} * \frac{Area_2}{Area_1}\right) \approx 1.2V \cdot \quad (1)$$

For obvious reasons, the traditional bandgap voltage reference cannot function well if the supply voltage is less than V_{REF}.

Recently, new voltage references are reported in literature to overcome the low supply voltage problem by using a current-mode reference [2-4]. These references generate a temperature-independent current, which is then mirrored to a resistor to create a sub-1 V output voltage. These circuits are capable of operating with a supply voltage as low as 1 V, and they can be implemented in different processes such as BiCMOS [3] and CMOS [4]. However, most of them suffer from high flat-band and 1/f output noise due to the presence of the MOS current mirror. Another type of low voltage reference, which is based on the weighted difference in gate-source voltages between MOS devices, uses an external filtering capacitor at the output to reduce the noise [5]. Unfortunately, the required capacitance is too large (greater than 100 nF) to be integrated. Furthermore, external components should be avoided since they increase the cost and volume of the system.

In this paper, a new bandgap voltage reference featuring low output noise without the use of a large external filtering capacitor is presented. The circuit architecture is compatible with both CMOS and BiCMOS processes. In Section II, the prior arts of reverse bandgap voltage references are reviewed and analyzed. This is followed by the proposed reference with details of the circuit design and performance analysis that solve the drawbacks with prior arts. Next, experimental results are provided in Section III to validate the design concept and performance. Last of all, the work is summarized in Section IV.

II. Sub-1 V Low-Noise Bandgap Voltage Reference

A. Prior Arts: Reverse Bandgap Voltage References

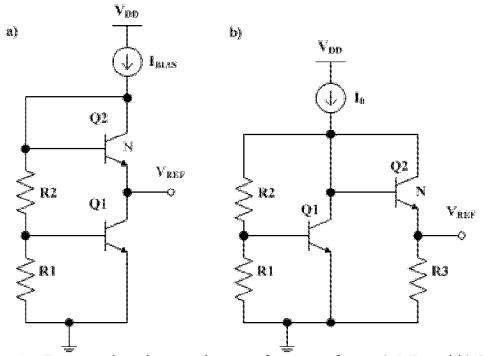

Fig. 1. Reverse bandgap voltage references from a) [6] and b) [8]

The proposed sub-1 V low-noise bandgap voltage reference uses the reverse bandgap voltage principle, which is derived by dividing both sides of (1) by the gain factor M to yield

$$V_{REF} = \frac{V_{BE1}}{M} + V_T * \ln\left(\frac{I_{C1}}{I_{C2}} * \frac{Area_2}{Area_1}\right) \approx 200mV \cdot \quad (2)$$

This principle has been used in the circuit shown in Fig. 1a [6]. In the circuit, the transistor $Q1$ and resistors $R1$, $R2$ form a modified V_{BE}-multiplier with negative-TC. The positive-TC component is created by subtracting V_{BE2} of transistor $Q2$ from the modified V_{BE}-multiplier. Assuming the base current I_{B1} can be neglected, the addition of the negative-TC and positive-TC components yield the following reference voltage:

$$V_{REF} = \left(\frac{R2}{R1}\right) * V_{BE1} + V_T * \ln(N) \approx 200mV \cdot \quad (3)$$

A comparison of (3) to (2) indicates the circuit in Fig. 1a implements the reverse bandgap voltage principle. The main advantage of the circuit is low output noise, which is the noise of $Q1$. The output noise of current-mode references is

dominated by the noise sources of the current mirrors with field-effect transistors. Since *Q1* is a NPN bipolar transistor, its 1/f noise and flat-band noise are always lower than those of a field-effect transistor with the same size and bias current [7]. However, this circuit has a few drawbacks. First, transistor *Q1* operates in the saturation region. The variation in the reference voltage is expected to be large due to the variations in I_{B1}. Second, the circuit topology is process-dependent. It requires the use of NPN transistors, which are not available in most standard CMOS processes. Third, a separate current source with a well-defined TC is required for proper operation.

A simplified version of the reference described in [8] is shown in Fig. 1b. It uses the same operation principle as [6], but this design has no transistors in the saturation region. The circuit is self-biased by using the reference voltage to create a temperature-independent current source. However, the topology is not portable to modern CMOS processes, and it cannot operate below 1.1 V. In addition, the feedback structure is complex and unstable with almost any capacitive load [9].

B. *The Proposed Bandgap Voltage Reference*

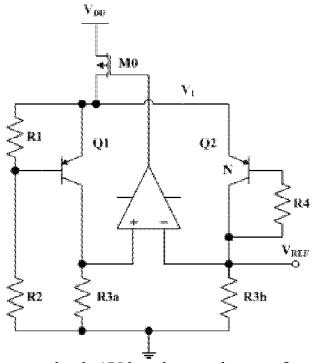

Fig. 2. Proposed sub-1V bandgap voltage reference circuit

The topology of the proposed voltage reference circuit is shown in Fig. 2, with *R3a* = *R3b* = *R3*. The transistor *Q1* and resistors *R1*, *R2* form a modified V_{BE}-multiplier which can be described as

$$V_1 = \left(\frac{R2}{R1}+1\right) * V_{BE1} + I_{B1} * R2 \cdot \tag{4}$$

The reference voltage is defined as

$$V_{REF} = V_1 - V_{BE2} - (I_{B2} * R4) \cdot \tag{5}$$

Substituting (4) into (5) yields

$$V_{REF} = \left(\frac{R2}{R1}\right) * V_{BE1} + (V_{BE1} - V_{BE2}) + (I_{B1} * R2 - I_{B2} * R4) \cdot \tag{6}$$

If resistors *R2* and *R4* are selected such that I_{B1}*$R2$ = I_{B2}*$R4$, the reference voltage fits the form of (3). The inspection of the circuit in Fig. 2 shows the minimum supply voltage is

$$VDD_{MIN} = V_{REF} + (I_{B2} * R4) + V_{BE2} + V_{SATMO} \approx 1V \,. \tag{7}$$

This demonstrates the circuit can operate with a supply voltage as low as 1 V.

The transistors *Q1* and *Q2* operate far from the saturation region, which allows them to have high current gain and low I_B. Moreover, the addition of resistor *R4* provides base current balancing for *Q1* and *Q2*. Besides controlling the effects of the base currents, the circuit uses PNP transistors instead of NPN transistors. Since lateral PNP transistors are available in almost any CMOS process, it makes the circuit portable to different low-cost processes. Last of all, the collector bias currents of *Q1* and *Q2* are well-defined by the feedback loop formed by the op-amp in Fig. 2. It forces the collector voltages of *Q1* and *Q2* to the same potential. Since the resistors *R3a* and *R3b* have the same value, $I_{C1} = I_{C2}$.

C. *Analysis and Optimization of Output Noise*

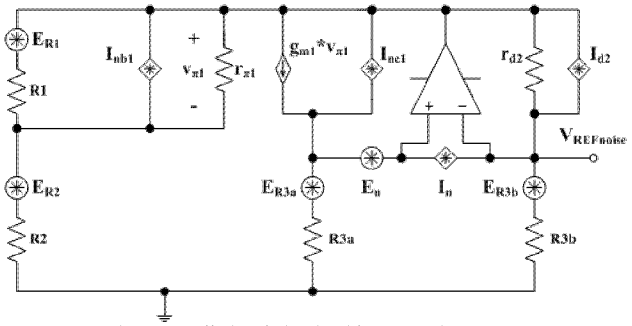

Fig. 3. Small-signal circuit with RMS noise sources

The major noise sources of the proposed circuit can be estimated using the small-signal circuit in Fig. 3. The resistor *R4* in Fig. 2 is usually not a major noise contributor, especially at low frequencies. Hence, it is removed to allow *Q2* to be treated as a diode. The current source *M0* in Fig. 2 is incorporated into the feedback amplifier. The bias currents of *Q1* and *Q2* are defined in the noise analysis as I_{B1}, I_{B2} and I_{C1}, I_{C2} for the base currents and collector currents, respectively. The parasitic base resistance (r_{b1}) of *Q1* is not included since I_{B1} is less than 500 nA for the design ($r_{\pi 1} >> r_{b1}$). The spectral density (*Volts/*$\sqrt{Hz}$) of the un-correlated RMS noise sources in Fig. 3 with *R3a* = *R3b* = *R3* are [1]

$$E_{Rx} = \sqrt{4kT * Rx}; \quad x = 1, 2, 3, \tag{8}$$

$$I_{nb1} = \sqrt{2q * \frac{I_{C1}}{\beta_1} + \frac{K_1}{f} * \left(\frac{I_{C1}}{\beta_1}\right)^a}, \tag{9}$$

$$I_{nc1} = \sqrt{2q * I_{C1}}, \tag{10}$$

$$I_{d2} = \sqrt{2q * I_{C2} * \left(\frac{\beta_2 + 1}{\beta_2}\right) + \frac{K_1}{f} * \left(\frac{I_{C2}}{\beta_2}\right)^a}. \tag{11}$$

Since the noise sources are un-correlated, superposition can be used to calculate the reference output noise contributed by each source. The total mean squared reference output noise ($V_{REFnoise}^2$) is the sum of the squared contributions from each noise source, which is equal to

$$V_{REFnoise}^2 = \left[\frac{1}{G_0}\right]^2 \left| \begin{array}{l} (G_1)^2 * \left\{\left(\frac{R2}{R1}\right)^2 * E_{R1}^2 + E_{R2}^2 + (R2 * I_{nb1})^2\right\} \\ +(G_2)^2 * \left\{E_n^2 + (R3 * I_{nc1})^2\right\} \\ +(G_3)^2 * \left\{(R3 * I_{d2})^2\right\} \\ +(G_2 + G_3)^2 * \left\{(R3 * I_n)^2 + E_{R3}^2\right\} \end{array} \right|. \tag{12}$$

The G factors in (12) are

$$G_0 = G_2 - (G_1 + G_3), \tag{13}$$

$$G_1 = g_{m1} * R3, \tag{14}$$

$$G_2 = 1 + \frac{R2}{R1} + \frac{R2}{r_{\pi 1}}, \tag{15}$$

$$G_3 = g_{m1} * r_{d2} \approx 1. \tag{16}$$

The feedback loop in Fig. 2 forces $I_{C1} = I_{C2}$. The same feedback loop allows resistor *R3b* to be represented as

$$R3b \approx \frac{V_{REF}}{I_{C2}}. \tag{17}$$

Substituting (17) into (14) with $R3a = R3b = R3$ and $I_{C1} = I_{C2}$ yields

$$G_1 = \frac{V_{REF}}{V_T}. \tag{18}$$

In order for the total output noise to be reduced, G_0 in (12) needs to be maximized. This is accomplished by selecting R_1, R_2, and I_{C1} such that $G_2 >> (G_1+G_3)$ or

$$\left(\frac{R2}{R1} + \frac{R2}{r_{\pi 1}}\right) >> \frac{V_{REF}}{V_T}. \tag{19}$$

If (19) is satisfied and $G_2 >> (G_1+G_3)$, (12) is simplified as

$$V_{REFnoise}^2 \approx E_n^2 + (R3 * I_{nc1})^2 + (R3 * I_n)^2 + E_{R3}^2. \tag{20}$$

The dominant noise sources which limit the lowest output noise in (20) are the input-referred voltage and current noise sources of the feedback amplifier, the collector current shot noise of *Q1*, and the thermal noise voltage of resistors *R3a*, *R3b*. Substituting (17) into (8) and (10) shows E_{R3} and $(R3*I_{nc1})$ in (20) can be decreased by increasing I_{C1}. Also, (19) is satisfied if I_{C1} is large (i.e. $r_{\pi 1}$ is small). The noise modeling given above allows designers to focus on minimizing the effects of the major noise sources on the reference output with a given current budget and die size.

D. Circuit Implementation

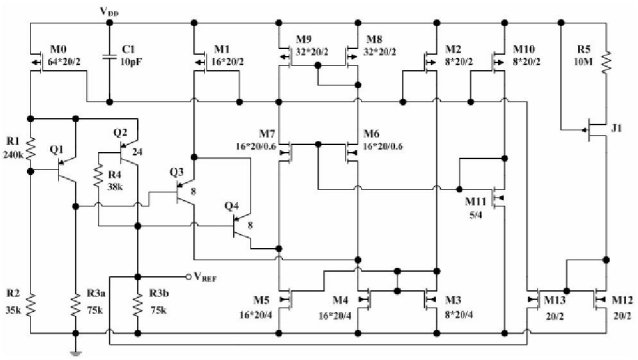

Fig. 4. Schematic of the sub-1V bandgap voltage reference

Fig. 4 illustrates the detailed circuit schematic of the proposed voltage reference circuit. The feedback amplifier consists of the bipolar input pair *Q3*, *Q4* along with a folded-cascode structure formed by *M4* – *M9*. The amplifier is self-biased by mirroring the current from *M0* to *M1*, *M2* – *M5*. Resistor *R5*, junction FET transistor *J1*, and MOS devices *M12*, *M13* form a start-up circuit which is off during normal operation to save power [7]. As soon as the voltage across *R3b* is large enough, *M13* turns off. The bias for the cascode transistors *M6* and *M7* is generated by *M10* and *M11*. Capacitor *C1* in Fig. 4 is used to set the dominant pole in the feedback loop at the output of the amplifier. This makes sure the negative feedback loop is stable. The area ratio between *Q1* and *Q2* was chosen to be $N = 24$. The resistors were selected to have the reference draw ~ 20 µA from the supply at room temperature. This level of current consumption is similar to other low-voltage references reported in literature. It also provides the reference with acceptable output noise performance.

III. Experimental Results

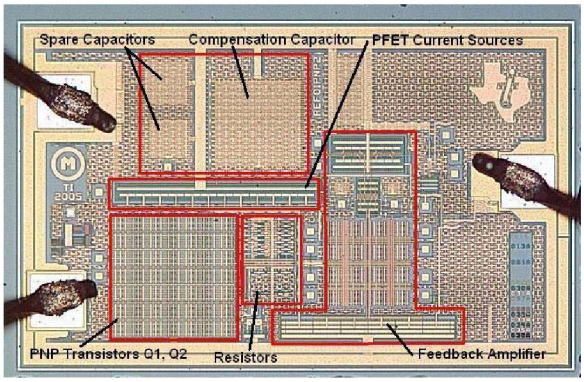

Fig. 5. Chip micrograph of the proposed bandgap voltage reference

The proposed low-noise voltage reference was fabricated using the 50HPA07 0.5-µm BiCMOS process from Texas Instruments [10]. The chip micrograph is shown in Fig. 5. The entire design occupies a die area of 0.4-mm^2.

A total of 32 units were characterized over temperature and supply voltage. The distribution of the untrimmed reference voltage at room temperature with a 1-V supply is shown in Fig. 6. From the data, the reference voltage is 190.91 mV ± 1.083 mV (3σ). Based on this data, the untrimmed error of the reference is less than ± 0.6%.

The distribution of the temperature coefficient (TC) from –40 to +125 °C with a 1-V supply is shown in Fig. 7. The measurements indicate the TC of the reference (box method) is 11.04 ppm/°C with a standard deviation of 5.22 ppm/°C. The mean TC of the reference is less than the values recorded for the circuits in [3] (without curvature correction) and [4-6].

The simulation and measurement results of the output noise spectral density at room temperature with a 1-V supply are displayed in Fig. 8. The measurement results closely match the simulation results. The flat-band noise spectral density is ~ 40 nV/√Hz with a corner frequency of 20 Hz. The measured peak-to-peak output noise ($6*V_{REFnoise}$) is 4 µV from 0.1 to 10 Hz. This is very close to the simulated peak-to-peak noise of ~ 3µV, in which a majority of the low frequency noise is due to the 1/f noise of *M4*, *M5* in Fig. 4. As (20) indicates, the input-referred voltage and current noise sources of the feedback

amplifier are major contributors to the output noise. Nevertheless, the peak-to-peak output noise is low enough for the proposed reference to be used in a 12-bit analog-to-digital converter.

Additional measurements such as supply current and line regulation were collected. These results along with a comparison of performance matrix between similar low voltage references are summarized in Table I.

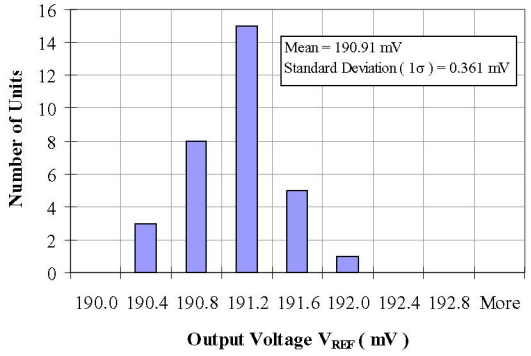

Fig. 6. Untrimmed reference voltage distribution at room temperature

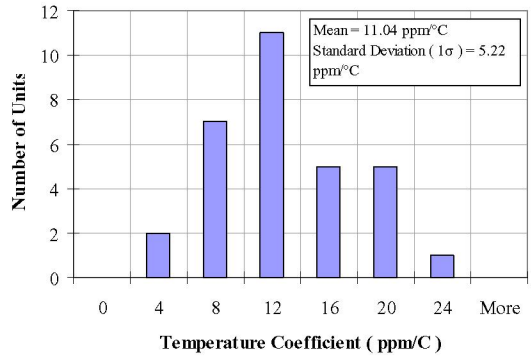

Fig. 7. Untrimmed temperature coefficient distribution

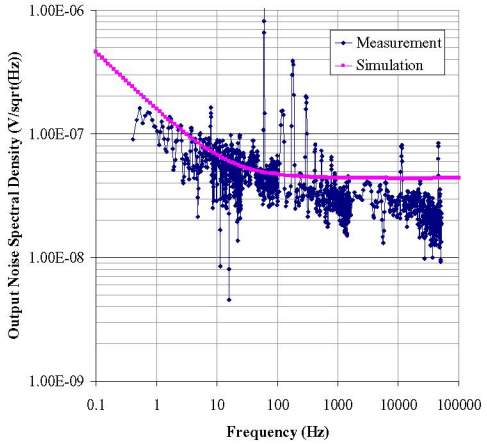

Fig. 8. Simulated & measured results of output noise spectral density

IV. CONCLUSION

A voltage reference is presented in this paper which has a 190.91 mV ± 1.083 mV (3σ) output, a mean TC of 11.04 ppm/°C from -40 to +125 °C with a 1-V supply, and a 20 µA static current. Besides excellent temperature coefficient and untrimmed accuracy, the voltage reference has a very low-noise output without the need for an external filtering capacitor. In addition, a theoretical noise model is given in support of the circuit design and optimization. Last of all, the topology of the circuit is compatible with different processes such as BiCMOS and CMOS with minimal re-design effort.

TABLE I. COMPARISON OF LOW VOLTAGE REFERENCES AT 1-V SUPPLY

	This work	**[3]**	**[4]**	**[5]**	**[6]**
Technology	0.5-µm BiCMOS	0.8-µm BiCMOS	0.6-µm CMOS	0.6-µm CMOS	0.18-µm CMOS
TC (ppm/°C)	11 (-40 to +125 °C)	20[a] (0 to +80 °C)	15 (0 to +100 °C)	36.9 (0 to +100 °C)	63[b] (-20 to +100 °C)
Line Regulation (µV/V)	48 (1.0 to 5.0 V)	114 (0.95 to 2.0 V)	4231[c] (0.98 to 1.5 V)	256.73[d] (1.4 to 3.0 V)	1100 (0.95 to 2.5 V)
Noise Density @ 100Hz (nV/√Hz)	~ 40	N/A	N/A	152 (C_{OUT} = 100 nF)	N/A
V_{REF} (mV) ±3σ Variation (mV)	190.9 1.083	536 N/A	603 N/A	309.31 19.26	169.4 N/A
Minimum Supply (V)	1.0[e]	0.95	0.98	1.4	0.95
Supply Current (µA)	20	92	18	9.7 (max)	2.4

a. Without curvature correction.
b. Converted from 0.76% to 63 ppm/°C with V_{REF} = 169.4 mV.
c. Converted from 2.2 mV over supply range to 4231 µV/V.
d. Converted from 0.083%/V to 256.73 µV/V with V_{REF} = 309.31 mV.
e. Minimum supply voltage at -40 °C.

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