High Speed Serial Link Transmitter for 10Gig Ethernet Applications

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Abstract

This paper presents a Current Mode Logic (CML) transmitter circuit that forms part of a Serializer/ Deserializer IP core used in a high speed I/O links targeted for 10+ Gbps Ethernet applications. The paper discusses the 3 tap FIR filter equalization implemented to minimize the effects of Inter Symbol interference (ISI) and attenuation of high speed signal content in the channel. The paper also discusses on the design optimization implemented using hybrid segmentation of driver segments which results in improved control on the step sizes variations, Differential Non Linearity (DNL) errors at segment boundaries over Process mismatch variations.

Keywords— Equalization, Transmitter, CML, Tap co-efficient, SerDes I/O, ISI ,Gigabits per second(Gbps)

1. Introduction

The continuing growth in processing power of digital computing ASIC's and multi core-processors has fuelled the need for high-speed serial interface links to meet the demands of high performance SoC designs. Unlike the parallel standards, the new serial standards have inbuilt clock information embedded within data patterns. This means that no clock has to be sent along with the data from one end of a link to another. It also means that the clock must be accurately recovered from the received signal, along with the data itself using the clock data recovery logic. It is the plesiosynchronous nature along with the increasing data rates that makes serial link communications so powerful and so challenging to implement.

As standards evolve and data rates continue to climb, serial communications systems with embedded clocks will become even more dominant. These high speed serial links are scalable without limit and are free from the timing and alignment problems that limit the extension of parallel standards to higher bandwidths.

Due to the recent developments in the communication and computation market, the demand for high speed serial data transmission through wired network such as backplane/cable is increasing at a rapid rate in application areas such as servers and data communication routers. To meet this need, industry standards [1] are being developed which define the channel characteristics and I/O electrical specifications of short reach (on-board) and long reach (intercard) High speed serial link Serializer / Deserializer cores that operate at data transmission rates in excess of 10 Gbps. The successful qualification of a high speed serial link IP into a customer ASIC design involves overcoming several challenges to achieve a design with low transmit jitter, high receiver jitter tolerance, optimum power budget and compliance for variety of Industry standards such as Infiniband, SATA, SCSI, Fibre channel specs, 10G Ethernet specs to provide good interoperability.

Section 2 provides an overview of the High Speed Serial link Transmitter core architecture, key sub-blocks comprising the Transmitter. This section describes the Current Mode logic (CML) transmitter circuit designed to support data transmission rate of 10+Gbps, its architecture details, its circuit components and the effect of PVT variations on the transmitter's output linearity. Section 3 describes the transmitter sub-blocks. Section 4 explains transmitter equalization topology used to enable good system performance at 10+ Gigabits of data transmission and section 5 explains the need for precise DNL output step control and the need to make the transmitter's output linearity response more tolerant to PVT variations. Section 6 describes the hybrid (thermometric & binary) segmented architecture approach and compares it with the conventional binary approach of the transmitter implementation and shows the improvement in the Differential non linearity errors of the Transmitter response over process mismatch variations. A summary in section 7 concludes the paper.

1063-9667/10 $26.00 © 2010 IEEE
DOI 10.1109/VLSI.Design.2010.51

2. Background

For many high speed serial standard links, the permissible signal swing at the receiver inputs can be as low as 200 mV peak-peak differential swing (For example, PCI Express permits a minimum differential input swing of 175 mV). At these low swings, even a relatively small amount of noise or stray signal energy can cause significant problems. For example, 50 mV of noise, a level that is often seen on power supplies, represents more than 25% of a 175 mV signal. To compound the problem, at data rates around 10Gbps and above, many parts of the system begin to behave like transmission lines and effect of inter symbol interference (ISI) is much more prominent.

An example of a serial data eye monitored at receiver input is shown above. The channel typically acts like a low pass filter and distorts the incoming serial data signal to varying extent (based on harmonic frequency bin). The Vertical eye opening indicates the amount of Inter symbol Interference (ISI) introduced due to the non ideal channel and interface interconnects (connectors, package etc.,) present in High speed serial link system. Signal integrity concerns frequently dictate that the data signal to be equalized at the transmitter and/or receiver in order to counter the effects of the channel and decode the signal properly.

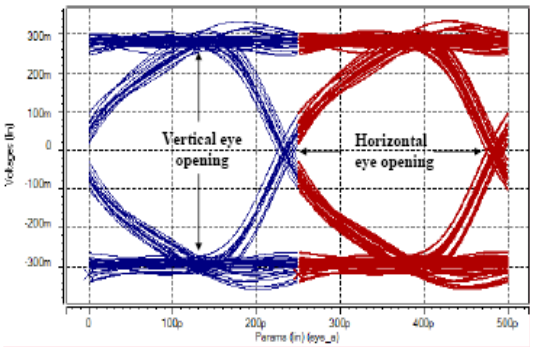

Figure 1: Data Eye Diagram

3. Transmitter Sub-blocks

Transmitter is a key integral block of SERDES core as it serializes the Low frequency parallel bits of input data into a high speed serial stream of output data and drives it across a channel. Transmitter typically comprises of the following key blocks namely Serializer, Predriver, Output driver stages.

The transmitter [2] accepts 8 single ended (CMOS levels) parallel data bits and time division multiplexes (8 to 1) them into a single current mode logic serial stream running at up to 11.1Gbps. The driver/equalizer multiplexes the 8 bits in parallel and creates a differential data stream that is frequency equalized (3-tap Feed forward Equalization) according to the media channel.

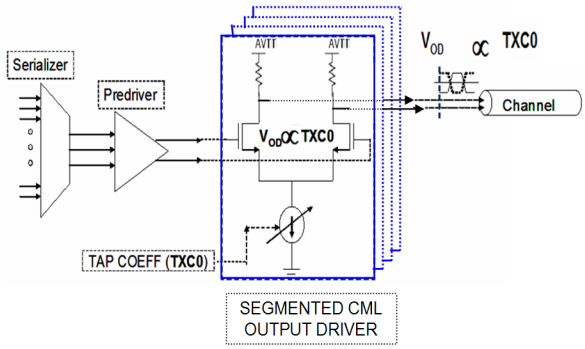

Figure 2: Conventional Transmitter Block Diagram

The conventional diagram block diagram of a high speed serial link SerDes [3] core transmitter diagram is shown in Figure 2. The key circuit blocks comprising the High speed CML mode transmitter are the 8 to 1 Serializer block, Pre-driver stage, Reference current block (IREF) and the output IDAC block which provides the bias current to the Final CML Output Driver stage. The 8:1 section accepts half-rate differential clock, CLKP/N, and does the serialization from 8 parallel bits to a 3-tap FIR where each tap is running up to 11.1 Gbps. The sign and the magnitude of the taps are controllable. The transmitter's output Differential voltage swing VOD varies linearly as a function of its input TAP coefficient settings (TXC0).

$$V_{OD} \ \alpha \ TXC0$$

The transmitter's output differential voltage swing V_{OD} (mV) varies linearly as a function of its final output driver bias current. The bias current is determined by set of input binary TAP coefficient settings (TXC0) which in turn determines the effective peak to peak output voltage swing of the driver as shown in Figure 3.

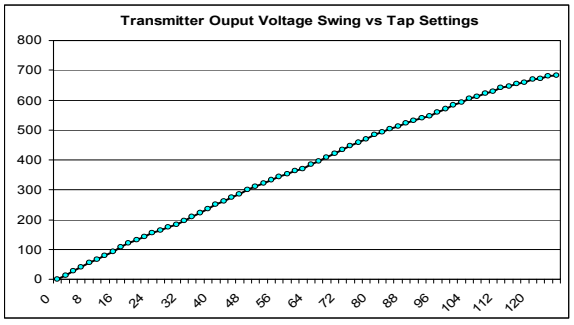

Figure 3: Transmitter Output voltage Vs Input Tap settings

4. Transmitter Equalization

Conventionally, equalization is done at the transmitter to overcome the Inter Symbol Interference (ISI) that results from dispersion and attenuation of high speed signals through the channel. Equalizer at the transmitter has a transfer function that is roughly the inverse of the channel's frequency response as shown in Figure 4. This pre-distorts the data to be transmitted as it suppresses the low frequency contents and boost high frequency components fed into the channel so as to achieve good eye opening at receiver side.

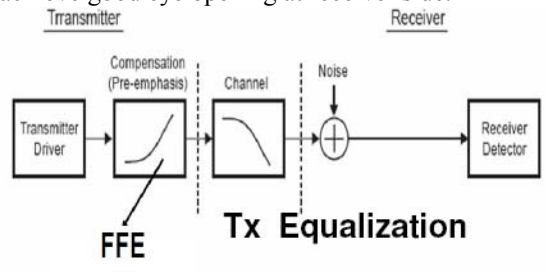

Figure 4: Transmitter Equalization

The serial data signal is delayed by several flip-flops which implement the taps for the filter. Each tap is multiplied by a weighted tap coefficient value, and the results are summed and driven to the serial data output.

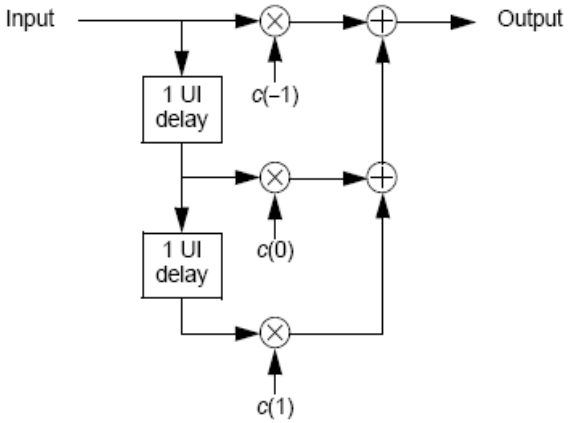

FIGURE 5: 3-TAP TRANSMITTER EQUALIZATION

The resultant output voltage of the equalizer would be summation of main tap, pre and post cursor tap settings with their respective polarity settings taken into account. For example in case where the pre and post cursor polarity bits are set complementary to that of main tap settings, then the output would be

3– Tap Ideal Output =(C(0) - C(-1) - C(+1)) *□V

The graphical representation of summation of main, pre & post cursor taps voltage waveforms to obtain the cumulative output voltage for the above scenario is shown below in figure 6. This equalizer effectively pre-distorts the signal at the transmitter output such that the resulting signal at the receiver input is clean.

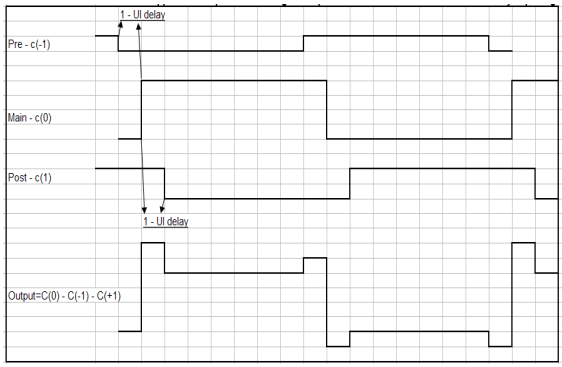

Figure 6a: Pre, Post, Main Tap waveforms

The transmitter output waveforms simulated using cadence spectre simulator for a standard K28.5 bit pattern sequence is shown in figure 6b. As shown in the figure 6b, the high frequency transitions are left untouched, whereas the low frequency transitions are attenuated, realizing a low frequency de-emphasis or a high frequency pre-emphasis.

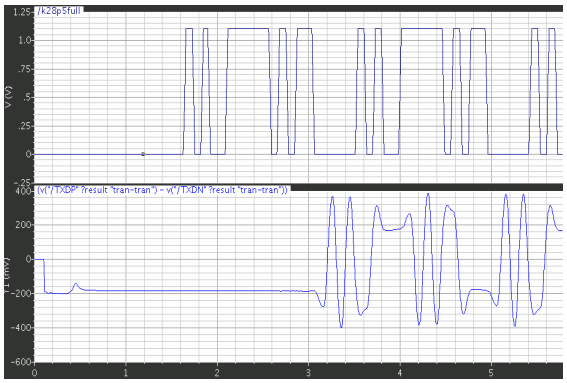

Figure 6b: CML Transmitter output waveforms for K28.5 bit pattern

5. DNL step size variations

The Current Mode Logic (CML) output driver stage comprises a stack of four driver segments and is controlled by a 7-bit binary weighted tap. Each segment is in turn grouped in cluster of 32 unit driver fingers and the switching within the driver segment happens in a binary fashion corresponding to the input tap settings. The output driver is implemented in a segmented fashion as shown in Figure 3. As the binary weighted input tap coefficient settings (7 bits) are swept from minimum to maximum range the corresponding

segments are turned on there by incrementally increasing the output driver swing. However the various industry standards for physical layer has a prescribed electrical specification on the limit of the incremental output voltage/step size limit for the driver outputs in order to obtain a good transmitter linearity response over full range of operation.

The Differential Non linearity specification as prescribed by IEEE 802.3ap standard mandates a uniform voltage step size increments over the full driver output voltage range. The transmitter design has a DNL specification limit of 5mV to 20mV in order to be compliant for IEEE 802.3ap standards. This means that the incremental voltage step size variation including on chip process, voltage, temperature and mismatch variations has to be contained within the limit of 5mV to 20mV.

However the binary segmented approach as shown in Figure 7 exhibits larger DNL variations while switching across the segment boundaries due to inherent binary coding nature as multiple bits are transitioning from ON to OFF at segment boundary.

TABLE 1: SEGMENT SWITCHING TRUTH TABLE

Count	SEGMENT - III	SEGMENT - II	SEGMENT - I
1 -- 32			
64 -- 33			
96 -- 65			
128 -- 97			

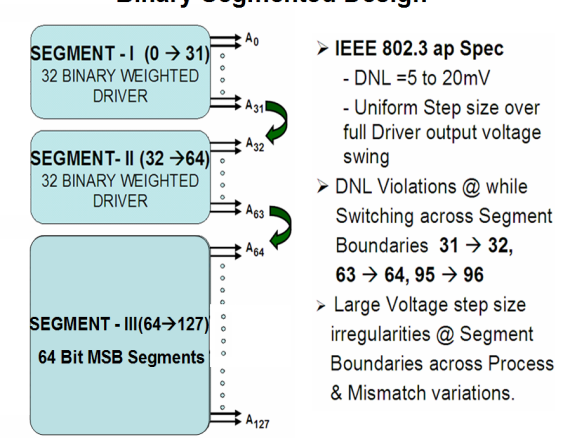

Figure 7: Binary Segmented Transmitter design

The statistical variation of the Differential Non linearity, step size at segment boundary was simulated using cadence circuit simulator, spectre for IBM 65nm, cmos10sf process technology. The results of these statistical simulations showing the Differential Non Linearity distribution for binary segmented transmitter approach is shown Figure 8.

The simulation results clearly show the issue larger step size voltage variations well beyond the IEEE 802.3ap specification limit of 5mV to 20mV range.

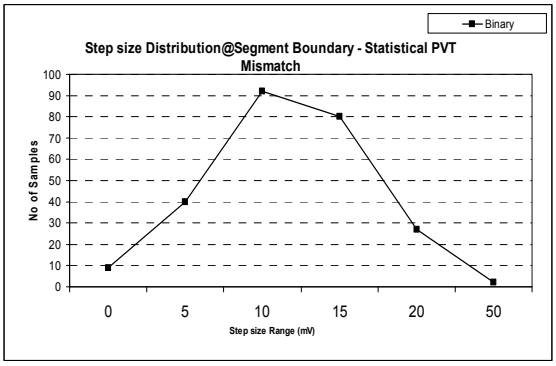

Figure 8: Step size Variations distribution at segment boundary

If there are DNL errors introduced at some point over the main tap segments boundaries of equalizer then the amount of energy contributed by the main tap relative to that of pre/post cursor taps would be lower than that of ideal case. Hence this would translate to larger amount of ISI for tap settings at the segment boundaries. This necessitates a precise control on the output voltage step size(DNL) for main taps C(0) as the tap coefficients are adjusted to maximize eye opening along voltage axis thereby minimizing the Inter symbol Interference(ISI) effects of pre and post cursor bits on the main tap.

3– Tap Ideal Output =(C(0) - C(-1) - C(+1)) *□V

6. Hybrid Segmented Architecture

The proposed solution involves implementation of mixed mode of thermometric switching across segment boundaries and binary switching within the segments. The hybrid segmented architecture approach for the transmitter implementation which involves the use of thermometer decoding at upper/higher order switching across segments and binary switching within the lower order segment improve switching performance at the segment boundaries as shown in Figure 9.

The key advantages of this hybrid approach offers the good linearity response for the transmitter output stage due to thermometric switching across driver segments and at the same time keeps the overall area advantage of binary segmentation within the segments.

TABLE 2: PROPOSED HYBRID SEGMENTATION SWITCHING TRUTH TABLE

COUNT	SEGMENT - IV	SEGMENT - III	SEGMENT - II	SEGMENT - I
1 -- 32	X	X	X	✓
64 -- 33	X	X	✓	✓
96 -- 65	X	✓	✓	✓
128 -- 97	✓	✓	✓	✓

Hybrid Thermometric Segmentation Approach

- Segmentation Approach
  - 7 Bit → 4 Segments with each segment of 32 Units group
  - Binary Switching within Segment (to optimize area & metal tracks)
  - Thermometric switching within segment will need prohibitively large No of Unit elements
  - Thermometric logic to switch across Segments - at segment boundaries
  - To minimize the Large Differential Non linearity/step size voltage irregularities at the segment boundaries due to Binary switching at Segment boundaries

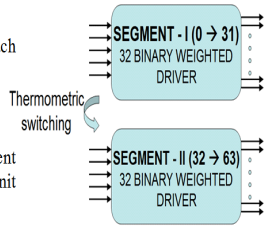

Figure 9: Hybrid Segmented approach

The transmitter main cursor consists of four predriver/driver segments and is controlled by a 7-bit IDAC. The segmentation is done in a group of 32 units and the switching within the segment happens in a binary fashion corresponding to the IDAC input settings. However the switching at the segment boundaries (from one segment to next) is designed in a thermometric fashion. The conventional design had a binary segmentation through out and this resulted in large Differential non linearity/step size irregularities at the segment boundaries. The proposed hybrid segmented architecture approach shown in figure 10 for the transmitter implementation involves the use of thermometer decoding at upper/higher order switching across segments and binary switching within the lower order segments. This hybrid segmented approach improves overall switching performance at the segment boundaries.

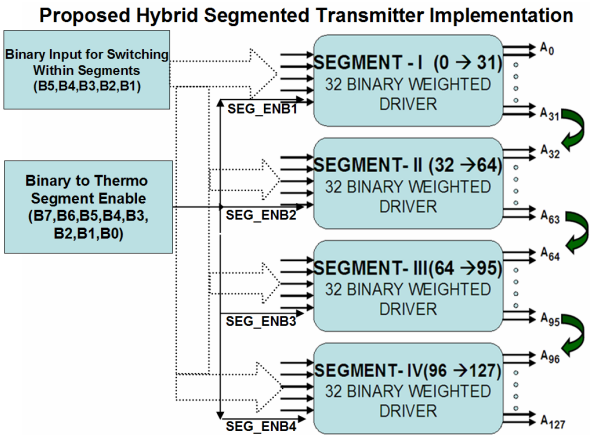

Figure 10: Hybrid Segmented Implementation

The thermometer decoding of the upper segments avoids the static and dynamic problems associated with fully binary-weighted implementations due to the large major carry transitions. It is, however, impractical to implement the entire DAC in straight thermometer format for N input bits, since of high resolution DACs N is large and the unit elements would number several thousand. The segmented architecture is a compromise between the full binary-weighted architecture and the full thermometer architecture. The comparison of Monte Carlo statistical distribution of the step size at the segment boundaries between the proposed thermometric segments and conventional binary segments are shown in figure 11.

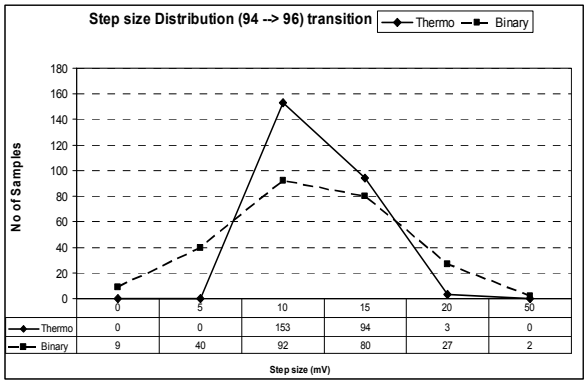

Figure 11: Comparison of voltage step size distribution/DNL errors

The Gaussian distribution of the transmitter differential output voltage ($V_{OD1} - V_{OD2}$) step size as the tap coefficients are incremented at segment boundaries are shown below. This clearly shows that step size voltage distribution is limited over a very narrow range in case of thermometric switching at segment boundaries (within 5mv to 20mv) across process and mismatch variations.

7. Summary

This paper has presented a current mode logic CML transmitter circuit that forms part of a Serializer / Deserializer IP core used in a high speed (11.1 Gbps) I/O link. The paper also presented on a hybrid segmented architecture which is a compromise between the full binary-weighted architecture and the full thermometer architecture.

8. Acknowledgements

The authors wish to thank John F Ewen, Kevin Kramer from IBM Corp. Fishkill, New York for valuable technical guidance, insights and managerial support of this project.

9. References

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