Low-voltage bandgap reference with output-regulated current mirror in 90 nm CMOS


A low-voltage bandgap reference (BGR) circuit is designed and fabricated in a 90 nm CMOS technology. To mitigate error resulting from the mismatch in temperature dependency of the current in the output current mirror device and that of the BGR core, an output-regulated current mirror is incorporated. Experimental results show that the output voltage is 497.2 mV at 25°C with a temperature coefficient of 28.3 ppm/°C between −40°C and 80°C. The circuit occupies 0.0337 mm² and dissipates 276.6 pW with a supply voltage of 1.2 V.

Introduction: There are several ways of providing a reference voltage, which is a fundamental requirement in many VLSI systems. The most popular is a bandgap reference (BGR) circuit, which utilises the temperature characteristic of a bipolar junction transistor (BJT) or diode. However, as CMOS technology enters the deep-submicron (DSM) era, the variability of the current in a PMOS output device depends on the drain bias and temperature. The temperature dependency of the current in a PMOS device becomes more severe and the changes in temperature depend on the output resistance. This effect is more severe with DSM technologies, in which the temperature dependency of the PMOS device is more sensitive to the drain voltage of the device. Therefore, an additional circuit is needed to match the drain voltages of the CMOS output device and the PMOS in the BGR core.

Effects of PMOS drain voltage mismatch: The temperature dependency of the current in a PMOS output device depends on the drain bias voltage. If the temperature dependency of the current in the PMOS output device is 1 nA/°C higher than that of the PMOS in the BGR circuit, then the temperature dependency of the output voltage can increase by several tens of µV/°C, depending on the output resistance. This temperature dependency changes the output voltage by several mV over the operational temperature range. This makes it difficult to obtain a convex curve of output voltage against changes in temperature. This effect is more severe with DSM technologies, in which the temperature dependency of the PMOS device is more sensitive to the drain voltage of that device. Therefore, an additional circuit is needed to match the drain voltages of the CMOS output device and the PMOS in the BGR core.

Circuit design: In the proposed design, shown in Fig. 1, the transistor M1 is connected to a regulating device M0 and an error amplifier U2. Together they form an output-regulated current mirror which set the drain voltage of M2 to that of M0. For the BGR core to operate correctly, the drain voltage of M3 must also match that of M0. This can be achieved by a simple single-stage error amplifier U1. This structure ensures that the output current is correctly matched to the BGR core current, so that I1 = I2 = I3. As long as enough voltage headroom exists for M3 and M8, we are free to determine the output reference voltage VREF by setting the ratio between R1 and R0(R1 = R0), not being affected by the channel length modulation or by the difference in the temperature dependency of M1 and M2. If we include the offset provided by the op-amps, then VREF is determined as follows:

\[
V_{REF} = \frac{R_1}{R_0} \times \frac{R_1}{R_0} \times V_T \times \ln N + V_{BE1} - \left(1 + \frac{R_3}{R_6}\right) \times V_{offset1} + R_1 \times g_{ds3} \times V_{offset2}
\]

where R1 = R2, V_{offset1} is the offset of U1, which is V_{BE1} - V_{BE2}, V_{offset2} is the offset of U2, which is V_B - V_C, g_{ds3} is the transconductance of M1, N is the ratio between the size of the emitters of Q2 and Q1, and V_{BE1} is the base-emitter voltage of Q1.

Experimental results: The proposed BGR was designed and fabricated in a standard 90 nm CMOS technology, and Fig. 2 is a photograph of the die. The circuit operates at a supply voltage of 1.2 V and consumes 276.6 µW at 25°C. The circuit core occupies 0.0337 mm². Fig. 3 shows the measured output voltage of the proposed BGR against temperature. The temperature with zero temperature coefficients is properly positioned around 25°C, at which the output voltage is 497.2 mV. Between −40°C to 80°C, the voltage changes by 1.69 mV corresponding to a temperature coefficient of 28.3 ppm/°C. Fig. 4 shows the measured output voltage against the supply voltage. The chip operates successfully between 1.05 and 1.35 V.

Fig. 1 Proposed bandgap reference circuit

Fig. 2 Die photograph of proposed BGR circuit

Fig. 3 Output voltage dependence on temperature
**Conclusions:** To reduce errors due to the difference in the temperature dependency of the output device and the BGR core device, we propose a low-voltage BGR circuit incorporating an output-regulated current mirror. Experimental results show that an acceptable temperature curve can be achieved despite the variable process parameters of DSM CMOS technology.

**Acknowledgment:** This work was supported in part by the grant from the Industrial Source Technology Development Program (10033657, 10033812) of the Ministry of Knowledge Economy (MKE) of Korea.

References