Digital PVT Calibration of a Frequency-to-Voltage Converter

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***Abstract*—A digital process, voltage, and temperature (PVT) calibration loop for a Frequency-to-Voltage converter (FVC) is presented. The FVC needs a precisely controlled delay element, but delay in CMOS is highly dependent on the PVT condition making it neccessary to calibrate the delay line. The system is designed to calibrate against an external reference frequency which is already present in the intended application. This is advantageous, as it is not neccesary to generate additional bandgap or other reference on chip. Results from transistor level simulations using a 90 nm CMOS process are presented, showing good regulation accross PVT corners and ability to track changes in the PVT condition. The calibration loop is digital and therefore a good fit for CMOS technology.**

I. Introduction

Analog-to-digital converters (ADCs) based on frequency $\Delta\Sigma$ modulators (FDSMs) have shown promise for low-power and low-voltage operation [1]—demonstrating their suitability in wireless sensor network (WSN) applications with modest resolution requirements. In FDSM ADCs, the input signal is frequency modulated (FM) by a voltage controlled oscillator (VCO), followed by a sampling frequency-to-digital converter (FDC). Although the converter has equivalent $\Delta\Sigma$ noise shaping, the noise shaping is limited to the quantization noise of the FDC—any VCO imperfections are added directly to the input signal. The VCO is limiting the performance of the converter with respect to linearity and noise. VCO non-linearity and noise has greatest impact for converters with second order noise shaping because the quantization noise is lower compared to converters with first order noise shaping.

In many applications it is desirable to have a voltage mode input, in the sense that the system output is linear with respect to the input voltage. To achieve this in a FDSM based ADC, a highly linear VCO with wide tuning range is necessary. In deep sub-micron (DSM) CMOS technology, VCOs with inherently high linearity and wide tuning range are not feasible to implement. Techniques such as digital post-processing of the ADC output have been successfully exploited to achieve the desired linearity [2]. A different approach is illustrated in figure 1 [3], [4]. Here the VCO itself is linearized using a closed loop feedback. In this case, the linearity requirement is shifted from the VCO to a FVC. The VCO can then be optimized for low jitter, as in most PLL applications, without too stringent demands for linearity.

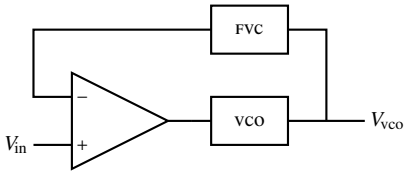

Figure 1. VCO feedback linearizion using a FVC

While most previous approaches have used switched capacitor (SC) based FVCs, we intend to use a pulse width modulation (PWM) based FVC. The implementation of the FVC is discussed further in section II. This FVC requires a time delay circuit with a fixed delay, independent of input signal frequency, and process, voltage, and temperature (PVT). The delay line is presented in section III. The inherent PVT dependence on the delay line is significant, and a calibration system is required to obtain the desired delay. In the intended ADC application, the VCO itself will not need calibration as it is driven in a closed loop feedback. Thus, calibrating the FVC will in turn calibrate the ADC as a whole, assuming the feedback amplifier functions correctly in all process corners.

The main topic of this paper is a system for automatically calibrating the delay circuit from an external reference frequency, to achieve the desired delay across all specified PVT conditions. As the intended application is an ADC, we already have a high quality reference in the sampling clock. This system is discussed further in section IV. In section V we present simulation results from transistor level simulations of the calibration system, which are then discussed. Finally, we conclude and give an outlook to future work.

II. FVC implementation

In this section, we present the design of a low-voltage and low-power FVC, with potential for high linearity. The circuit is depicted in figure 2. Here, q_{pvt}, is a control word for adjusting the delay to compensate for PVT. The circuit generating the PWM signal is shown in figure 2a. Defining the nominal input frequency, F_n, as:

$$F_n = \frac{F_h + F_l}{2} \tag{1}$$

where F_h represents the highest input frequency, and F_l represents the lowest input frequency. Assuming the delay

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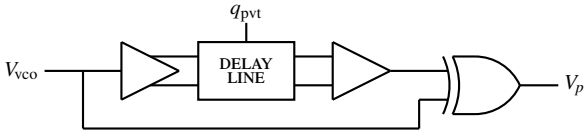
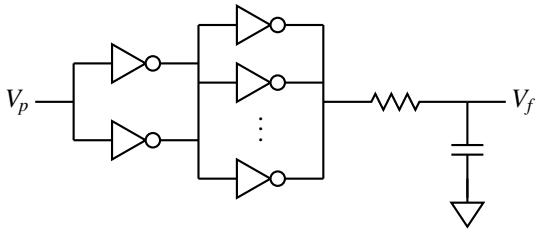


(a) Pulse generator (delay line and XOR function)



(b) Output buffer and low-pass filter

Figure 2. FVC circuit

line will ensure 90° phase shift with respect to the input signal at nominal input frequency,

$$NT_d = \frac{1}{4F_n} \tag{2}$$

where N is the number of stages in the delay line, and T_d is the delay from one delay unit, the average value of the output voltage will be given by

$$V_f = \frac{F_i \cdot V_{dd}}{F_h + F_l} \tag{3}$$

where F_i is the frequency of the input signal.

A passive low-pass filter is used to reconstruct the output voltage, V_f, by band-limiting the pulse signal, V_p, as illustrated in figure 2b. It is important to note that the output swing is less than rail-to-rail if F_l is greater than DC—which is the case for most practical applications. Because of this inherent limitation, C is several times larger than would be required if full rail-to-rail swing was possible. Additionally, care must be taken to stabilize the supply voltage, V_{dd}, as the integrated output signal will have a first order dependence on the supply voltage.

III. Delay line implementation

The delay line is the most critical component for the overall FVC performance. Jitter and distortion in the delay line will add to the output signal. Besides jitter, distortion needs consideration to achieve high linearity. If the delay element has not had time to settle to rail when the next edge is applied, the delay element will start from an undefined state resulting in a shorter delay. By decreasing the rise and fall time of each element, distortion can be reduced to well below the noise floor, at the expense of requiring more stages to achieve the desired delay. Additionally, the delay line must have sufficient tunability to account for all specified PVT corners—the unit delay, T_d, must be precisely controlled according to equation 2 to have a defined output voltage level.

The delay line element used here is shown in figure 4. Starved inverters is not used in this design because of the noise contribution from the starving transistors. Instead variable load capacitance was used to provide tunability. The variable capacitance in figure 4 is implemented using a capacitor array of gate capacitance loads which can be digitally switched on or off by the tuning system discussed in the next section.

IV. PVT calibration loop

The purpose of the PVT calibration loop is to find q_{pvt} so that the delay of the FVC delay line is fixed according to equation 2. The delay as a function of tuning word in the delay line does not need to be monotonic. However, better linearity will allow for a smoother and faster tracking of a dynamic PVT condition.

The PVT calibration circuit is built around a replica of the delay line used in the FVC, similar to the approach in [5]. Careful layout of the delay lines will ensure an identical PVT condition for both circuits, and only mismatch will cause deviation in the delay. The calibration circuit operates by periodically connecting the replica delay line in feedback for one period of the reference clock. A counter is used to count the number of positive edges seen during this period. A magnitude comparator is then used to decide if too many or too few edges were counted.

In normal operation, an up/down counter is used to generate the tuning word, q_{pvt}, for the delay lines. This tuning counter will count up or down depending on whether too many or too few clock edges were counted by the edge counter. In addition to the tuning word counter, a successive approximation register (SAR) algorithm is used when the calibration circuit is reset after power up. The SAR will probe all bits sequentially, starting with the most significant bit. This way, the circuit will have a shorter start up time, as the SAR normally will find the appropriate tuning word faster than the counter. Thus the SAR is used to quickly find the PVT corner, while the counter is subsequently used for tracking changes in the PVT condition. Fast startup is advantageous in the intended WSN ADC application, as the WSN node may periodically power down the ADC to conserve power.

The calibration system is depicted in figure 3. A state controller driven by the reference clock is used to synchronize the phases of the calibration system. The state S_0 is used only after an external reset to start the SAR. After S_0, the state controller logic cycles the four states $S_1, \ldots, S_4$ sequentially and repeats indefinitely. A multiplexer (MUX) is used to select whether the delay line is connected in feedback, or idle. Turning off oscillation when not needed conserves power and breaks the jitter accumulation. This is similar to a recirculating multiplying delay-locked loop (MDLL) [6], [7]. However, the delay line is not running continuously in this case. An enable circuit is used to make sure that the oscillation turns off when the delay line output is in the idle state. This is to avoid too narrow pulses on the edge counter.

The frequency of oscillation of the replica delay line when feedback is enabled, F_r, is given by

$$F_r = \frac{1}{2NT_d} \tag{4}$$

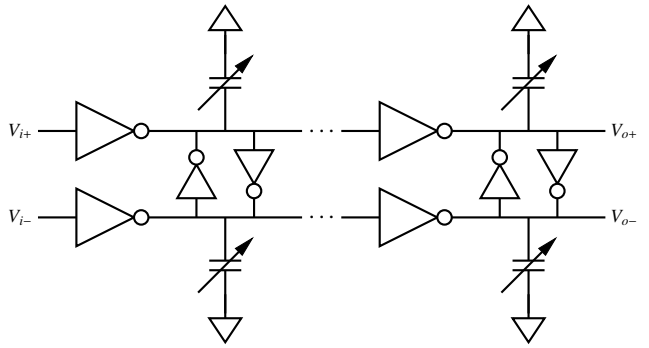


Figure 4. Delay line implementation with PVT tunability

From this, the number of edges, N_e can be derived

$$N_e = F_r T_s \tag{5}$$

Where T_s is one period of the reference clock signal.

As the delay is probed periodically, the system will not track and correct for transients in the PVT condition. Power supply noise is the most likely source of short term changes. The process is fixed after manufacturing, and only circuit aging will affect the process corner. These changes will be on a much longer timescale than the speed of the calibration loop. The temperature will likely change during runtime, but ambient temperature changes are also assumed to be much slower than the speed of the calibration loop. The power supply may experience a droop if powered by a depleatable energy source that gradually wears out. Again this change can be considered slow compared to the calibration loop. As the FVC itself has a first order dependency on V_{dd}, a good regulation of the delay line supply voltage is assumed, although the absolute value is allowed a ±10 % margin of error.

The calibration loop was designed for low complexity, low power, and robustness. The current implementation does no lock detection. In lock, the system will continuously program the delay up and down—one LSB of the tuning word. However, the resulting frequency spur will be attenuated by the reconstruction filter of the FVC. Lock detection would be beneficial for saving power, because the replica delay line would be idle for periods when the PVT condition is static. If process mismatch is significant, an additional tuning is necessary to calibrate the fixed offset due to the process. This could be implemented by removing one or more delay elements from the control of the calibration loop, to allow for offset compensation, depending on how precisely the absolute value of the delay needs to be controlled.

Table I
SIMULATED PVT CORNERS

PVT corner	Process corner	Supply voltage [V]	Temperature [° C]
Fast	FF	1.32	-25
Nominal	TT	1.2	27
Slow	SS	1.08	75

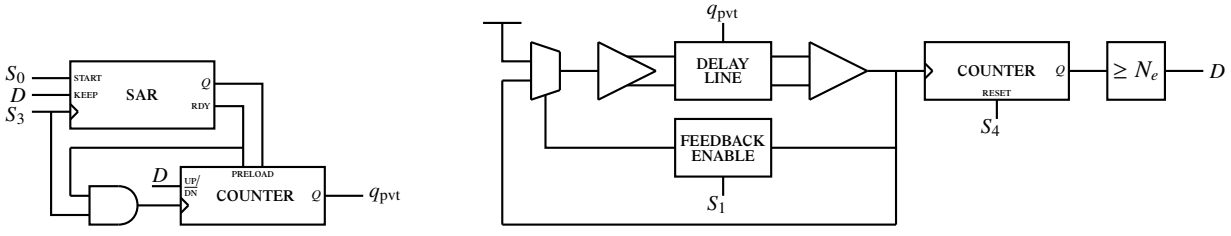
V. SIMULATION RESULTS

In this section, transistor level simulations of the calibration system is presented. The transistor models are foundry models for a commercially available 90 nm low-power CMOS process. The PVT corners giving rise to the fastest and slowest performance were considered, along with the typical condition. The PVT conditions are summarized in table I. In these experiments, we have assumed a VCO frequency range from F_l = 10 MHz to F_h = 30 MHz, thus NT_d is required to be 12.5 ns from equation 2. A delay line with N = 32 elements was used, and 6 bits were used for the tuning control word. The reference frequency was 2 MHz, thus T_s = 500 ns, which gives N_e = 20 from equation 5.

The simulation results are summarized in figures 5 and 6. Figure 5 plots the results from a full system simulation for the three PVT corners listed in table I. This simulation setup was designed to show whether the system was able to calibrate to the desired delay over all specified corners. The second simulation setup was designed to show the calibration loop response in the presence of a dynamic PVT condition. From the discussion in section IV, temperature was chosen as the most relevant for dynamic change during runtime. Figure 6 plots the dynamic response of the system in the presence of a temperature gradient. The temperature was swept from −25° C to 75° C in the time interval from 30 µs to 130 µs.

A. Discussion

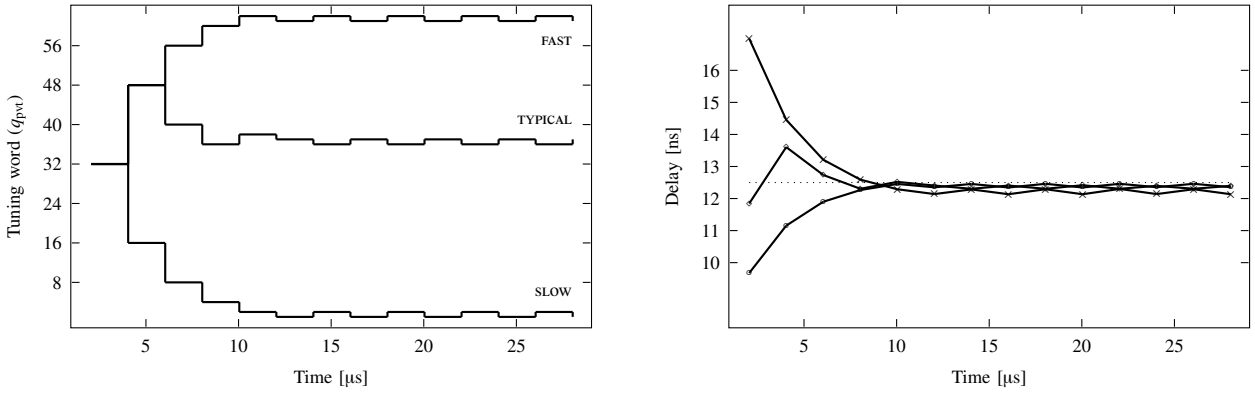
In both experiments the delay line is calibrated quickly because the SAR algorithm is used initially to find the operating point. The effect of continuously running the up/down counter is seen after the SAR algorithm finishes. When in lock, q_{pvt}



(a) Tuning word generator

(b) Replica delay line with feedback and delay measurement

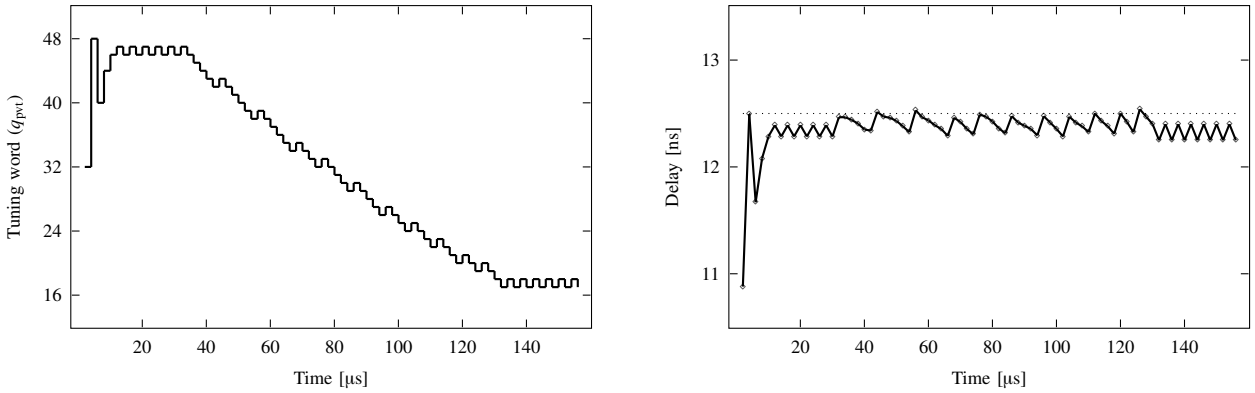
Figure 3. Calibration system outline



(a) Delay line control word, q_{pvt}

(b) Delay (typical: $\diamond$, fast: $\circ$, and slow: $\times$)

Figure 5. Calibration to a static PVT condition in fast, slow, and typical corners



(a) Delay line control word, q_{pvt}

(b) Delay

Figure 6. Calibration with typical process and V_{dd}, temperature is swept from −25° C to 75° C

cycles between two values, because the system will judge the delay as either too high or too low. In the intended application, this is not likely to cause a deterioration of the signal as the frequency spur is located outside the signal band.

While the calibrated delay is close to NT_d, the tuning is clearly limited by coarse resolution. It is important to note that this will not affect the linearity of the FVC, and in turn the ADC. However, it does directly affect the DC output level of the FVC.

VI. Conclusion

In this paper we presented the design and simulation of a PVT calibration system for a FVC. The calibration system is a good fit for DSM CMOS in that it is digital, low complexity, and does not require a bandgap reference. The simulation results presented in the preceding section indicates that the system is capable of calibrating and tracking PVT conditions over all specified corners during runtime.

Future work include a chip prototype of the calibration logic, and integration with the full ADC system.

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