# A Precision CMOS Voltage Reference with Enhanced Stability for the Application to Advanced VLSI's

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## Abstract

A precision CMOS voltage reference circuit is very important for the design of the stable voltage down converter of the high density VLSIs. By using the active mode operation of the component MOS transistors a CMOS bandgap type reference voltage circuit was re-designed for the enhancement of the circuit stability against the internal noises. The voltage supply independence, temperature independence and the stability characteristics of the reference circuit are analyzed by using analytical model. The designed circuit was incorporated into 5V to 3.3V down converter and integrated into a 16M DRAM by using 0.6μm CMOS technology. The measured characteristics of the fabricated voltage down converter shows a voltage dependence of 47.5mV/V and 18ppm/C temperature coefficient at $V_{ext}$=3.2V and 255ppm/C at $V_{ext}$=5.45V, respectively.

## I. Introduction

Recently, there have been many reports on the successful fabrication of ULSI's with deep submicron CMOS technology.[1, 2] While the device sizes keep on scaling down with the technology development, the 5V supply is still widely used in most circuits and systems. The submicron CMOS transistor is known to suffer from reliability degradation under the stress of the 5V supply due to hot carrier effect.[3] To avoid the hot carrier related problems, it is necessary to convert down the external 5V to a reasonably lower internal voltage.[4] This low internal supply voltage reduces the power consumption as well.[3]

Many schemes of the voltage down converter have been developed and incorporated into CMOS VLSI's. The band gap reference types based on parasitic bipolar transistors were studied because of its well developed design technique and good performance.[5] The process compatibility, however, makes the CMOS voltage converter more useful in the advanced VLSI's such as 4M DRAM and 16M DRAM.[6-8] An important issue in the design of voltage down converter for the integration into DRAM circuits is its noise immunity against the internal noises. The operating frequency of the DRAM reaches more than 20MHz and rather high electromagnetic interference noise flows through power lines. Also, when DRAM is operating in its active mode, a high peak current near the data output buffer generates an abrupt disturbance in the load node of the internal voltage supply.[3]

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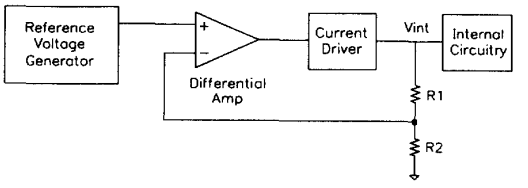


Fig. 1. Block diagram of the voltage down converter.

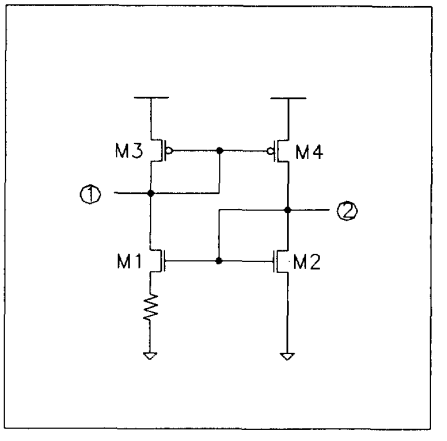


Fig. 2. Circuit of the precision CMOS reference voltage generator.

In this paper, a new design technique of a CMOS voltage down converter circuit for the application to advanced VLSI, especially 16M DRAM, is presented. In this technique, we use every transistor in its saturation mode to enhance the circuit stability against internal noise keeping good temperature insensitivity characteristics.

## II. CMOS Voltage Down Converter Circuit

The voltage down converter of Fig. 1 is composed of 3 different functional blocks, a precision CMOS voltage reference circuit, a CMOS differential amplifier and a CMOS voltage follower.[5] The overall characteristics of the voltage down converter follow those of the voltage reference circuit. Therefore, its insensitivity

to the variation of the external supply voltage and operating temperature are critical to obtain a stable operation of voltage down converter. A simple threshold voltage reference type was used in 16M DRAM in spite of its poor temerature characteristics owing to its circuit simplicity.[9] There was a report of a voltage reference circuit which used the threshold voltage difference between different MOSFETs to achieve the required temperature insensitivity.[10] However, additional process steps to make a difference in the threshold voltage of MOSFETs complicates its uses in the ordinary design of CMOS circuit.

A CMOS circuit with theoretically perfect supply independence was developed by E. Vittoz as a band-gap reference type following the bipolar circuit as shown in Fig.2.[11] In his scheme, MOS transistors are operated in weak inversion mode to obtain a stable PTAT(Proportional To Absolute Temperature) voltage. However, the current level of the MOS transistor in the weak inversion state is too low to get a stable reference voltage in the environment like a high density DRAM where a large internal noise is induced during operation. In addition, the MOS model in the weak inversion mode is not well developed to be used safely in the circuit design. In order to overcome these drawbacks, we use the active mode operation to obtain a stable internal reference voltage for the use in the noisy environment like 16M DRAM.

## III. Sensitivity Analyisis of CMOS Voltage Reference

When every MOS of Fig.2 is biased into its active mode, from the requirement of the equal voltage between gate and source of N-MOS M1 and M2, the operating current and reference voltage are given by

$$I_{op} = \frac{V_{GS2}-V_{GS1}}{R} = \frac{2}{R^2\beta_1}(K-1)^2 \qquad (1)$$

$$V_{ref} = V_T + \frac{2}{R\beta_2}(1-\frac{1}{K}) \qquad (2)$$

where $V_T$ is the threshold voltage of N-MOSFET, K is $\sqrt{\frac{\beta_1}{\beta_2}}$ and T is the absolute temperature. The magnitude of the reference voltage is independent of the external supply voltage. The bias current depends on the square of K and 1/R. Note that it shows stronger dependence on K and 1/R than the reference voltage does. To investigate the supply voltage dependence, we assume that the voltage at node 1 is higher by $\Delta V$ than that of node 2 and the current flowing through M1 is higher by $\Delta I$ than that through M2. Then equation (2) becomes

$$V_{ref} = V_{ref}\ of\ eq.(2) + \frac{K}{R\beta_1}(\lambda_n-\lambda_p)\Delta V \qquad (3)$$

where $\lambda_n$ and $\lambda_p$ are the channel length modulation parameters of the N-MOS and P-MOS, respectively. If $\Delta V$ depends on the external supply voltage linearly, the voltage independence is given as

$$\frac{dV_{ref}}{dV_{dd}} = \frac{K}{R\beta_1}(\lambda_n-\lambda_p) \qquad (4)$$

Therefore, as the channel length gets longer, the voltage dependence decreases. Its temperature independence is

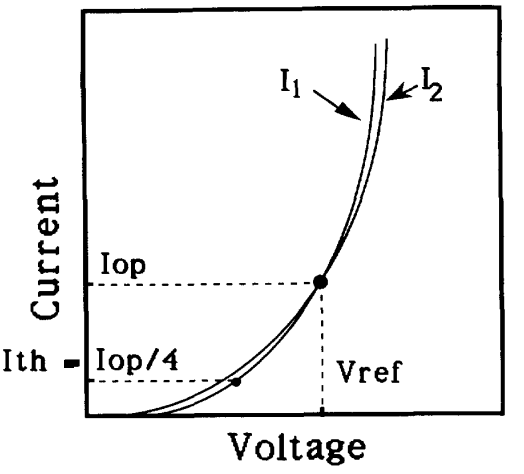


Fig. 3. Schematic diagram illustrating the operating point and the threshold bias current for the stable operation of the voltage reference circuit.

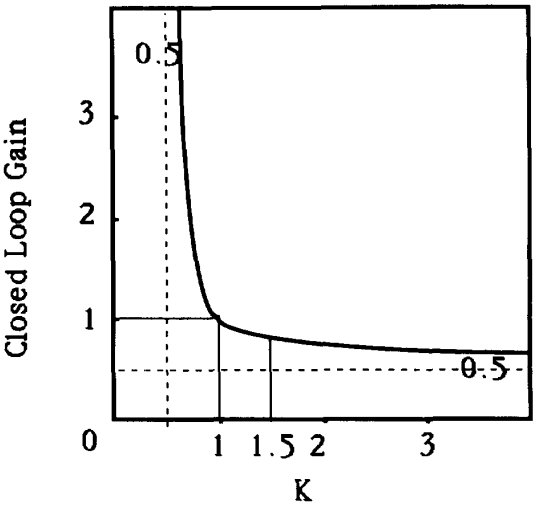


Fig. 4. Closed loop gain $A_v$ vs. K characteristics. The insufficient stability range is $1 < K < 3/2$.

$$\frac{dV_{ref}}{dT} = \frac{dV_T}{dT} + \frac{2}{R\beta_2}(1-\frac{1}{K})(\frac{3}{2T}) \qquad (5)$$

Since $dV_T/dT$ has a negative value of about -2mV/C, $dV_{ref}/dT$ can be reduced to a small value by properly choosing R, $\beta_2$ and K.

## IV. Stability Analysis of CMOS Voltage Refernce

A realistic concern of the circuit is the stability of the operating point of the circuit. It has two stable operating point at I= 0 and I = $I_{op}$ as shown in Fig. 3. A start-up circuit can be used to enforce the circuit into the stable range around the operating point. However, in the case of the narrow stability range, a simple start-up circuit is insufficient to obtain a stable operating point. One has to use a DC bias circuit to obtain a

stable operation of the reference circuit. The boundary between the insufficient and sufficient stability range can be analyzed by investigating the stability of closed loop composed of M1, M2, M3 and M4. The closed loop gain is given as

$$A_v = \frac{1}{2} + \frac{1}{4(K-1/2)} \quad (6)$$

The $A_v$ vs. K characteristics are shown in Fig. 4. The closed loop gain is determined by only the size ratio of transistors M1 and M2, not the size of R. That is, one can determine the stability of the circuit by properly choosing the ratio of transistors M1 and M2. Since $\frac{dA_v}{dK}$ depends on $-1/(K-1/2)^2$, the circuit shows more unstability as the value of K decreases. If we define the boundary between the sufficient and insufficient stability as the K value satisfying the following equation

$$\frac{1}{(A_v-1/2)}\left|\frac{d(A_v-1/2)}{dK}\right| < 1, \quad (7)$$

the circuit has an insufficient stability for the range $1 < K < 3/2$.

The threshold point for the unstability can be obtained from the condition of $A_v = 1$. From eq.(1) and (6), the current at the threshold point $I_{th}$ is given by

$$I_{th} = \frac{1}{4} I_{op}. \quad (8)$$

Therefore, a start-up circuit should flow a larger current than $I_{th}$ to the reference circuit to obtain a stable operation. In order to verify the above analysis, we choose two different circuits for the SPICE simulation. Fig. 5(a) shows the transient voltage characteristics of the circuit with K=1.04 and R=16.5Kohm under the condition of impulse input signal at the $V_{ref}$ node. Fig. 5(b) shows the charcateristics of the circuit with K=2 and R=30K ohm. It can be observed that the circuit stability increases with the increase of K as we expected in the above analysis.

## V. Internal CMOS Voltage Down Converter

Fig. 6 shows the complete internal voltage converter circuit designed by follwing the result of the above analysis. It uses two stage CMOS differential amplifier for the amplification of the reference voltage, in this case 0.98V, to the 3.3V internal voltage level. A transimpedance voltage follower circuit is used to supply a constant voltage to the internal circuitry of 16M DRAM. Fig. 7 is an optical micrograph of the fabricated circuit. A 0.6 μm CMOS process is used and the resulting circuit is successfully integrated with 16M DRAM to reduce the external 5V voltage to 3.3V internal power supply voltage. The regulated voltage vs. the external power supply voltage characteristics are shown in Fig. 8. The temperature insensitivity chracteristics are shown in Fig. 9. As shown in Fig. 8, its voltage independence is as small as 47.5mV/V in the range between 4.3V and 5.7V, which can bring a stable DC and AC operation characteristics to the integrated 16M DRAM. The temperature independence is 18ppm/C at $V_{ext}$ = 3.2V and 255ppm/C at $V_{ext}$ = 5.45V, which are comparable with those of band gap reference in the bipolar transistor circuit.

## VI. Conclusions

In conclusion, we developed a design technique of a stability enhanced precision CMOS voltage reference. Our technique uses the active mode chracateristics of the CMOS transistor to obtain a stable operation even under a large AC noise and ground bouncing of the high performance VLSI circuit. A reference voltage of 0.98V is first made using the developed reference circuit and incorporated into the CMOS voltage down converter to convert it to 3.3V internal supply voltage. The fabricated voltage down converter shows a 47.5mV/V supply voltage immunity characteristics in the range between 4.3V and 5.7V. Its temperature independence is 18ppm/C at the external voltage of 3.2V and 255ppm/C at the external supply voltage of 5.45V. The developed voltage down converter is suc-

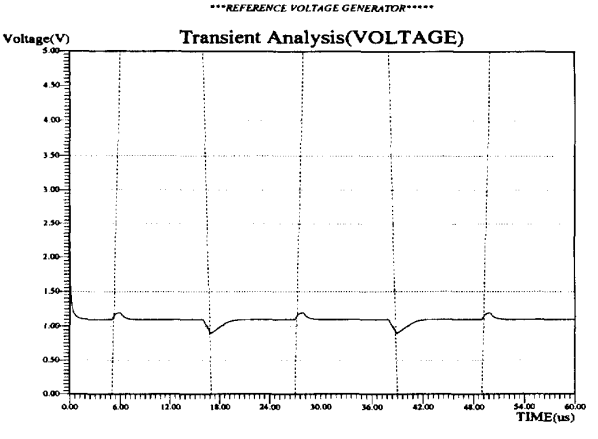


Fig. 5(a). Voltage stability analysis of K=1.04 circuit when the node 2 is capacitively coupled with the 5V noise pulses.

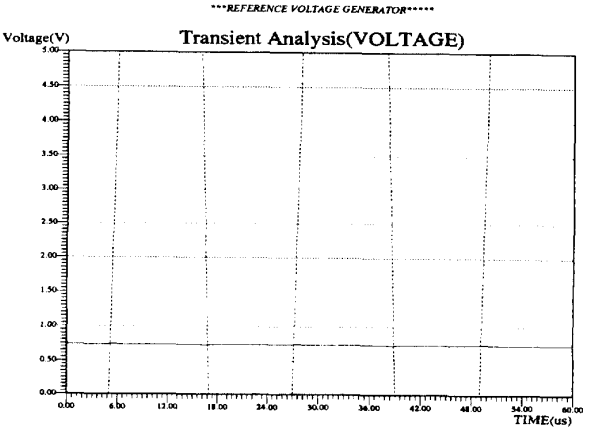


Fig. 5(b). Voltage stability analysis of K=2 circuit under the same condition as (a).

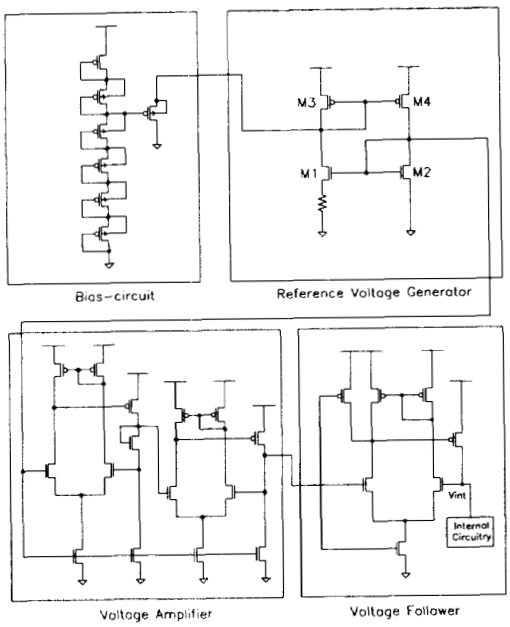


Fig. 6. Complete circuit schematic of the voltage down converter.

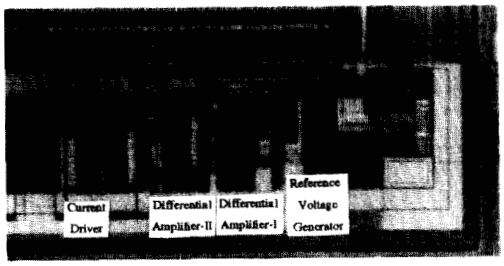


Fig. 7. Optical micrograph of the fabricated chip.

cessfully integrated into 16M DRAM resulting in a stable 16M DRAM characteristics over a full operation range.

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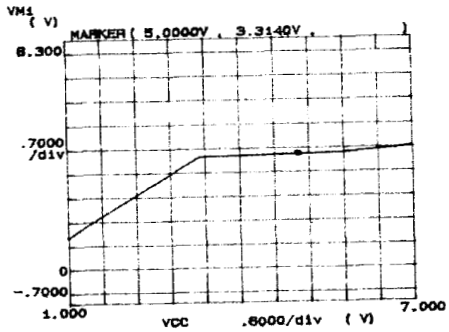


Fig. 8. Measured voltage dependence characteristics of the output of the fabricated voltage down converter.

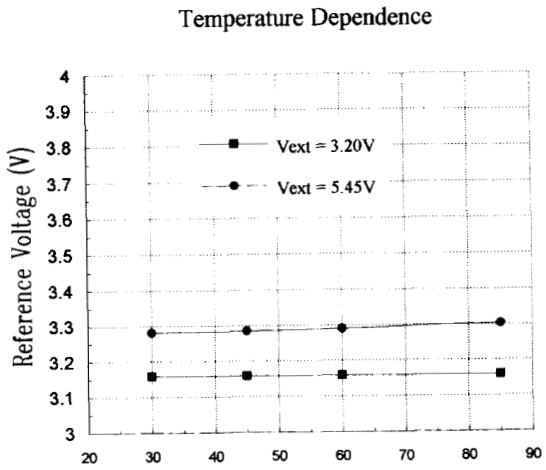


Fig. 9. Measured temperature dependence characteristics of the output of the fabricated voltage down converter.

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