A Low Power Sub-1 V CMOS Voltage Reference

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ABSTRACT

This work describes the circuit which generates a stable voltage of 466.5 mV for 1.8 V power supply in 0.18 µm technology. Circuit uses MOSFETs in linear region and in subthreshold region to generate PTAT and CTAT respectively intended to replace resistor and BJT. The temperature coefficient of circuit is 28.4 ppm/^{0}C in the range of -20 to +120^{0}C. The power supply rejection is measured as -30 dB at 8 KHz. Low power consumption of 3.98 µW is an important attribute of this circuit.

I. INTRODUCTION

Bandgap reference circuit is widely used to provide stable current and voltage references in analog circuits as well as in mixed signal CMOS circuits. A stable reference circuit should be robust against temperature, power supply and process variations.

Sub-1-V reference generation has got importance due to scaling resulting in shrinkage of MOS dimensions and reduction of power supply to minimize power consumption. The BGR generators that can be operated under 1-V supply have been widely used in ADCs, DRAM's, flash memories and various analog devices. Owing to follow Moore's law, it has become necessarily important to decrease the total power in the chip. This puts the constraint on the power dissipation of Reference generators. The design of this bandgap also considers for low power operation. In traditional BGR circuit, bipolar transistors and one or more resistors are used. BJTs that are used in BGR are in parasitic form in CMOS. Resistors occupy large area on the chip and hence increase the cost. On chip tolerance of resistors vary from 20% to 30% [6]. So we have replaced these components with MOS transistors to improve performance of BGR and to save chip area. The combination of different operating regions like subthreshold, linear and saturation of MOS suppresses the temperature dependence of voltage reference.

II. TRADTIONAL BANDGAP REFERENCE

Fig. 1 shows the traditional BGR. It comprises of both PTAT and CTAT sections. Reference voltage is given as

$$V_0 = V_{BE2} + IR_1 \quad (1)$$

$$= V_{BE3} + M\, I_2R_2 \quad (2)$$

where M is the multiplication factor between the W/Ls of M_4 and M_5. V_{BE} gives CTAT with roughly -1.5 mV/°K at room temperature. PTAT voltage is generated across resistor R_1 and also R_2. Thus, Vo (Vref) is approximately 1.25V which is nearly equal to bandgap of silicon (1.12V) at room temperature. We replaced the resistors and BJTs of the following circuit by MOS transistors to achieve efficient performance of reference and save area.

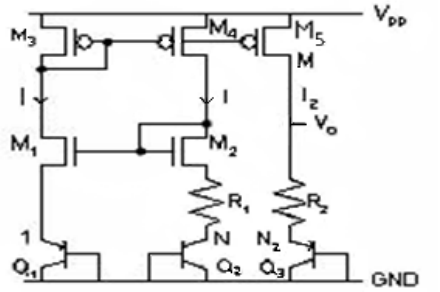

Fig 1 Traditional Bandgap Voltage Reference Circuit

III. STUDY OF MOS IN DIFFERENT REGIONS Of OPERATION:

In subthreshold region, for $V_{gs} < V_{th}$, there flows a finite current but it exhibits exponential dependence on V_{gs} which is given by[3]

$$I_d = \mu \frac{W}{L} V_T^2 \sqrt{\frac{q\varepsilon Nch}{4\Phi b}} \exp\left(\frac{Vgs - Vth - Vc}{nVT}\right) \quad (3)$$

where V_c is the correction term which gives the difference between V_{th} in the strong inversion and subthreshold region.

Φ_b is bulk Fermi level which is dependent on temperature given by [3]

$$\Phi_b = V_T \ln\left(\frac{Nch}{ni}\right) \quad (4)$$

n_i is the intrinsic carrier concentration which is also dependent on temperature given by [3]

$$n_i^2 \alpha T^3 \exp\left(\frac{-Eg}{KT}\right) \quad (5)$$

In triode region, MOSFET behaves like a resistor whose resistance value is controlled by W/L of the transistor and by the input bias applied so long as $V_{DS} << 2(V_{GS} - V_{th})$ [1]. It is given by following expression

$$R_{on} = \frac{1}{\mu Cox\left(\frac{W}{L}\right)(Vgs - Vth)} \quad (6)$$

without considering the early effect.

Threshold voltage decreases by 2mV for every 1^o C rise in temperature which results in increase in the drain current[12]. However, mobility decreases with temperature given by $\mu \alpha T^{-1.5}$ due to lattice

scattering (vibration of lattice) in the silicon crystal over -173 ^{o}C to +127^{o}C and its effect is dominant one, due to which there is decrease in drain current[10,11] .This can be used to anneal the change in current caused in the subthreshold region. Thus due to decrease in drain current with temperature in triode results in increase in their drain potentials.

For verifying the above equations appropriate transistor configuration was simulated in Cadence environment from -20 ^{o}C to +120^{o} C. Figures 2,3 show the Vout (i.e.V_{ds}) of a MOSFET operated in different regions of operations. It can be seen from these figures that MOSFET has PTAT behavior in triode [9] and in subthreshold region it has CTAT behavior [3]. Simulator used is Eldo SPICE with netlist generation in Cadence Virtuoso Schematic.

Following numerical data were obtained:
Change in V_{ds} = - 0.03 mV/C for subthreshold region; that for triode region is +1.66 mV /C.

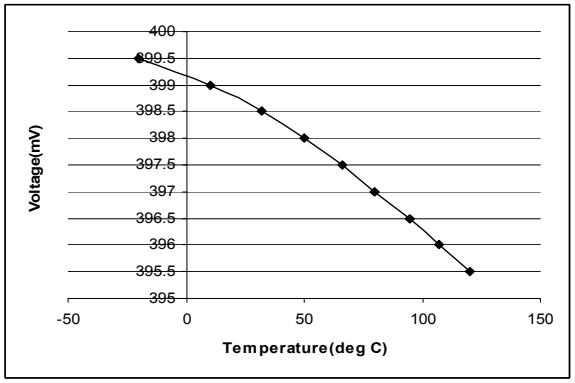

Fig 2 V_{ds} vs temperature for MOS in subthreshold region

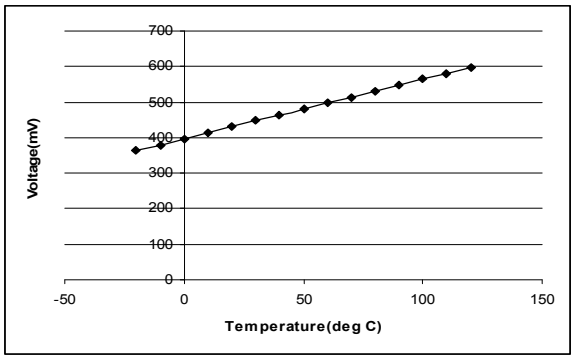

Fig 3 V_{ds} vs. temperature for MOS in linear region

IV. CMOS VOLTAGE REFERENCE

The proposed circuit is shown in Fig.4. Vdd has been chosen to be 1.8 V for the design and the technology is 180 nm. Supply independent biasing has been obtained by choosing W/Ls = 10µ/20µ for four transistors M_1, M_2, M_3 and M_4 (Fig. 4). This scheme is used for high power supply rejection [1]. All four transistors are always in saturation. Current through the circuit is governed by these four transistors.

M_5 and M_6 are operated in triode region; both behave as voltage controlled resistors. Here, two transistors are used which maintain symmetry in the circuit. The gate bias of 1.10 volt for these transistors obtained from the common gate node of M1 and M_2 is sufficient to keep M_5 and M_6 in triode region. The MOS M_7 and M_8 are in subthreshold region where they behave as BJTs of traditional BGR. Widths of these transistors need to be very large to ensure that these are in subthreshold region.

When the supply is turned on, there can be condition in which all the transistors carry a zero current through both the branches indefinitely as this is one of the operating points of loop formed by M_1, M_2, M_3 and M_4.Transistor M_9 act as "start-up" circuit to remove this problem. Whenever current through both the branches is zero that means gate potential of M_1 and M_2 is at ground and that of M_3 and M_4 is at Vdd. This makes M_9 ON and it supplies charges to the gate of M_1 and M_2 from the gate of M_3 and M_4. As soon as the gate node of M_1 and M_2 charges up to the gate voltage of M_3 and M_4, M_9 goes to cut off and thus start up device switches OFF.

$V_{gs7,8}$ of M_7 and M_8 produces CTAT voltage in subthreshold region. $V_{ds5,6}$ produces PTAT voltage of M_5 and M_6 in triode region. We assume that there is no contribution of M_1, M_2, M_3 and M_4 to the variance of V_{ref} with temperature. The final analytical expression of reference over which the addition of both PTAT voltage and CTAT voltage occurs is given by

$$V_{ref} = V_{gs7,8} + V_{ds5,6} \quad (7)$$

$V_{gs7,8}$ is obtained by manipulating equation (3) and $V_{ds5,6}$ by I_dR_{on} , substituting the value of R_{on} from equation (6) resulting into,

$$V_{ref}=nV_T\ln\left(\frac{Id}{\frac{W8}{L8}I_S}\right)+V_{th}+V_c+\frac{Id}{\mu Cox(W6/L6)(Vgs-Vth)} \quad (8)$$

Where $Is = a\mu V_T^2\sqrt{\frac{q\ e\ N_{ch}}{4\Phi_b}}$

where a is empirical constant which is found by simulation.

Electron mobility is given by [11],

$$\mu(T) = m\ T^{-1.5} \quad (9)$$

where m is proportionality constant.

Taking first order approximation for finding threshold voltage,

$$V_{th}(T) = -0.002\ T + V_{th0} + b \quad (10)$$
$$= -0.002\ T + c$$

Here, $c = (V_{tho} + b)$ is constant

where V_{th0} is the threshold voltage at 0^0C temperature, b is the conversion factor from degree Celsius to degree Kelvin.

The derivative of I_S is derived as,

$$\frac{d\ln Is}{dT} = \frac{d[\ln(\mu V_T^2 \sqrt{\frac{q\,e\,N_{ch}}{4\Phi_b}})]}{dT} \quad (11)$$

$$= \frac{(3+\frac{Eg}{kT})}{8T\ln(\frac{Nch}{T\sqrt{PT\exp(-Eg/2KT)}})} \quad (12)$$

where P is proportionality constant of equation (3)
Taking the derivative of V_{ref} with temperature,

$$\frac{dVref}{dT} = \frac{nk}{q}[T\ \frac{-(3+\frac{Eg}{kT})}{8T\ln(\frac{Nch}{T\sqrt{PT\exp(-Eg/2KT)}})} - \ln\frac{W_8}{L_8}$$

$$- \ln I_s + \ln I_d] + \frac{Id}{Cox(\frac{W_6}{L_6})}\ [\frac{-0.002\,T^{3/2}}{m(Vgs+0.002T-V_{th0})^2}$$

$$+ \frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}]-0.002 \quad (13)$$

= 0 for minimum V_{ref} at temperature 27^0C.
Simplifying above equation results into,

$$\frac{nk}{q}[T\ \frac{-(3+\frac{Eg}{kT})}{8T\ln(\frac{Nch}{T\sqrt{PT\exp(-Eg/2KT)}})} - \ln\frac{W_8}{L_8} - \ln I_s$$

$$+ \ln I_d] = \frac{-Id}{Cox(\frac{W_6}{L_6})}\ [\frac{-0.002\,T^{3/2}}{m(Vgs+0.002T-V_{th0})^2}$$

$$+ \frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}] + 0.002/(nk/q) \quad (14)$$

$$\frac{W_8}{L_8} = \exp\{\frac{q\,I_d\,L_6}{W_6 C_{ox} nk}[\frac{-0.002\,T^{3/2}}{m(Vgs+0.002T-V_{th0})^2}$$

$$+\frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}] - \frac{(3+\frac{Eg}{kT})}{8\ln(\frac{Nch}{T\sqrt{PT\exp(-Eg/2KT)}})}$$

$$- \ln I_s + \ln I_d - 0.002/(nk/q)\} \quad (15)$$

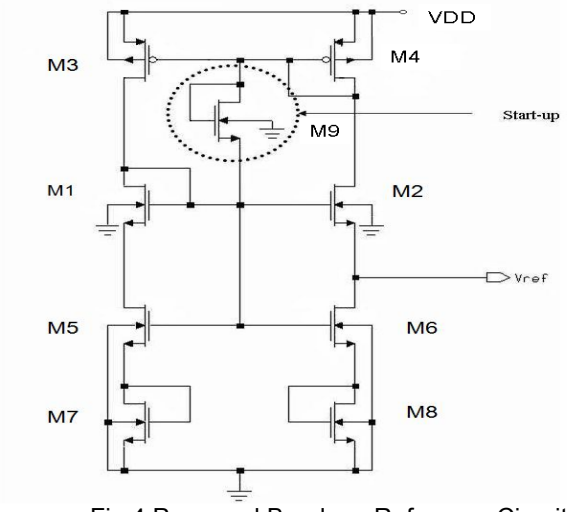

Fig 4 Proposed Bandgap Reference Circuit

From equation (15), we get the dimensions of $M_{7,8}$ with respect to $M_{5,6}$. These values are found and mentioned in experimental results.

V. EXPERIMENTAL RESULTS

Initial current is set by four transistors M_1, M2, M_3 and M_4. This comes out to be 6.1uA.When this loop is connected in circuit, current changes to 1.11 uA. The ratio is given by equation (15) which is found at temperature 27^0C.

A 180nm CMOS technology is used. Process parameters and device parameters are obtained from BSIM3 model of given technology. These are N_{ch} = 3.9 x 10^{17} cm^{-3} ni = 1.77 x 10^{10} cm^{-3}, E_g is 1.1eV, C_{ox} found at t_{ox} = 4.08 nm, n =1, k is Boltzmann constant, c = - 46 mV, By simulation, we got Id = 1.11 uA, V_{th} = 434.98 mV, V_{gs} = 306 mV, a = 409.28, m comes around 272.2, mobility at temperature of 27^0C = 0.0523 m^2/V-s, I_S = 22.22 nA. Putting all the values in equation (15), the values of W_6/L_6 were varied to get optimum value of W_8/L_8. This ratio comes out to be 33.11. If value of length is 20µm, the value of width comes up around 662.2µm. This is followed by a graphical approach in which W/Ls of M_5,M_6 were varied to get the minimum temp. coefficient(figure5). Accordingly, $W/L_{7,8}$ were also varied so as to get minimum temp. coefficient(figure 6).Simulated values show that W_8 is 618 µm.Thus by graphical method a error of 7.1 % in W_8 is corrected.

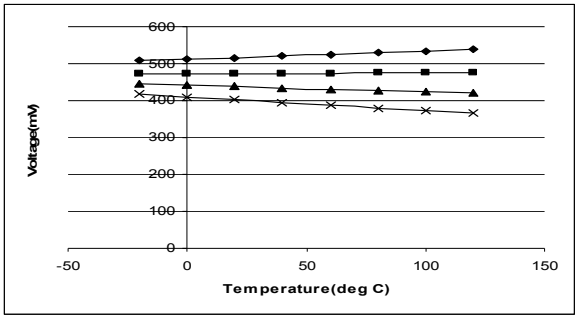

Fig 5 Variation of V_{ref} with temperature for different values of $W/L_{5,6}$

Figure 5 shows the variation of V_{ref} with temperature from -20 to 120 degrees for different values of $W_{5,6}$. In this figure, second curve (from the top) shows least variation with temperature.

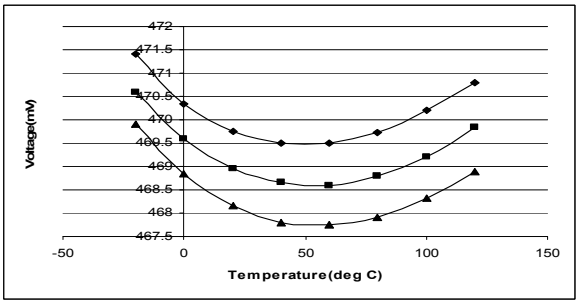

Fig 6 Variation of V_{ref} with temperature for different values of $W_{7,8}$

Widths of M_7 and M_8 are varied from 500u to

700u by keeping other dimensions constant and the results are in depicted in figure 6. Further finer variations led to $W_{5,6}$ = 618µm.Thus final dimensions are $W/L_{1,2,3,4}$ = 10u /20u, $W/L_{5,6}$ = 2.13u /20u, and $W/L_{7,8}$ = 618u /20u .

The output impedance of circuit is 35.61 Mega ohms. The circuit is tested for different resistive and capacitive loads. For resistive load of more than 100 Mega ohms, a small increase in temperature coefficient was found and for capacitive load, PSR actions at 10 KHz for -30 dB. The circuit has been tested for the temperature range as mentioned earlier. The circuit was also tested at four process corners such as FF, SS, FS and SF and checked for the temperature coefficient.

A.TEMPERATURE VARIATION FROM -20 to 120^{0}C

Having decided the W/Ls of all the transistor**,** the final temperature variation resulted parabolic behavior (figure 7) with minimum V_{ref} =466.38 mV at 45^{0}C and maximum of V_{ref} = 468.24 mV at -20^0 C. Small fluctuation of the order of 1.86 mV has been observed in Vref over the total range of temperature. This is equivalent to 28.4 ppm/^{0}C or 0.39% which is a very good figure of merit for bandgap reference circuit.

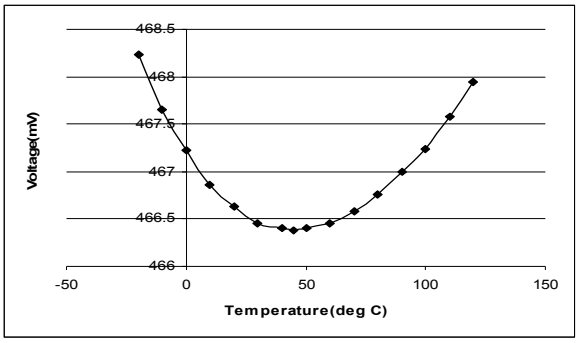

Fig 7 Final variation of Vref with temperature

B. IMPACT OF PROCESS VARIATIONS

Process parameters such as threshold voltage, mobility, etc. are different functions of temperature at different process corners. So, the bandgap reference should show minimum variation at different process corners. At four process corners (FF, SS, FS and SF) numerical values of variations in V_{ref} (in ppm/^{0}C) obtained are 29.28, 30.91, 37.93 and 34.01 respectively. Thus these values show voltage variation at four process corners with respect to temperature well under acceptable standards.

C. STABILITY ANALYSIS OF THE CIRCUIT

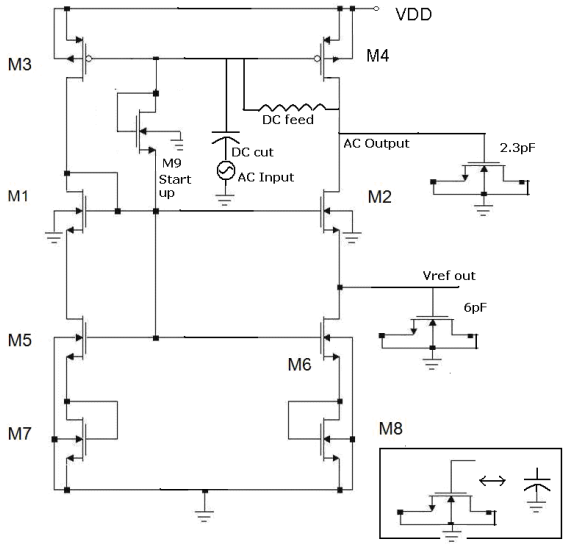

Fig 8 Circuit set up for AC analysis

Bandgap Voltage reference circuit needs to be well stabilized in all the conditions, as this circuit is a very generic voltage/current provider to many loads. The proposed bandgap reference has been verified for its open loop stability in all the conditions, keeping DC operating points same. The methodology for the ac open loop analysis is shown in the Figure 8. Two capacitors of C_1 of 2.3pF, C_2 of 6pF are used as shown in the figure. These are required from the simulations, to increase stability and to smoothen the settling of the circuit. These capacitors can be made of n-MOSFETs.

One of the closed loops in the existing circuits has to be broken at a point and ac analysis is required to be done for the open loop. During this analysis, DC operating conditions should remain the same. To implement this, the feedback path from the gate to drain connections of M4 has been broken and it is replaced by a DC feed inductor. This element keeps both nodes short for DC conditions but removes the connection for AC analysis. AC input is being injected at the gate connection of M4 through a sufficiently large DC Cut capacitor. We should keep in mind that these elements are used only for the ac analysis purpose.

Now the stability of this open loop has been checked at the drain of M4 as the output. Phase margin is observed to be 84 degrees, which is sufficient to keep the circuit stable & oscillation free. The respective simulation results for the ac analysis are shown below.

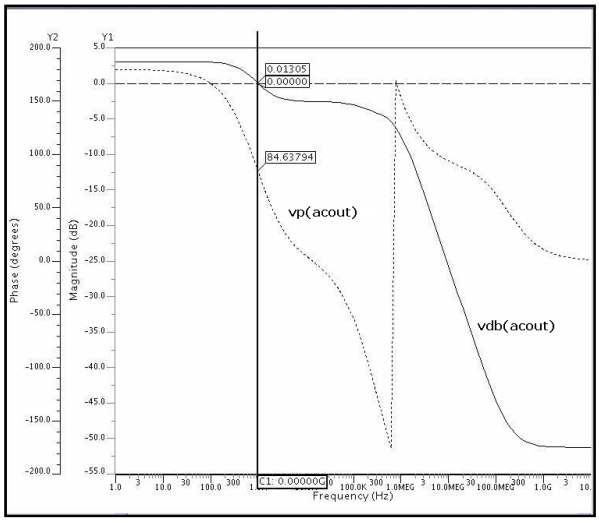

Fig 9 AC analysis simulation results

The transient response of the circuit has also been verified at the typical conditions. Power supply has been ramped down first and then ramped up to the final value for this purpose. The corresponding settling of Vref is shown in the following figure. Vref has been observed to settle down is its final value with out any oscillations as the Vdd ramps up in 10µS.This also justifies the start-up circuit performance.

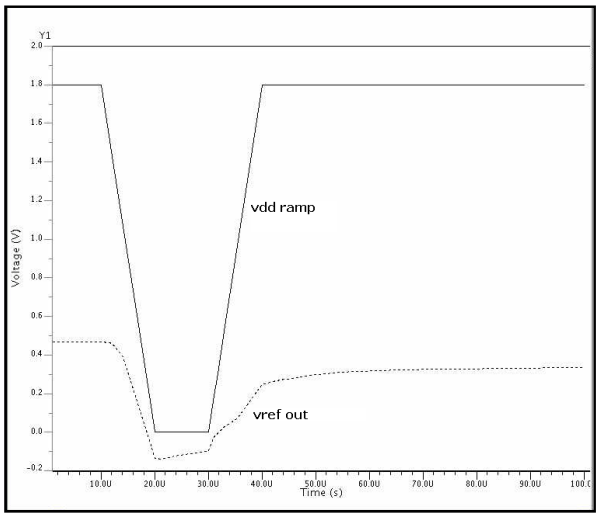

Fig 10 Transient Response with Vdd ramp

Comparison of the present work has been made with other work of sub-1-V generation and summarized in the following table:

	This work	[13]	[14]	[4]	[8]
CMOS Technology	0.18 µm	0.35 µm	0.35 µm	0.25 µm	0.25 µm
Supply voltage (In Volt)	1.8	0.95	3	0.85	0.9
Temp. Coefficient (In ppm/^{0}C)	28.4	33	39	58.1	19.5
Temp. Range (^{0}C)	-20 to 120	-40 to 100	-20 to 80	-20 to 120	0 to 100
Defined at all process Corners	Yes	Yes	Yes	No	No
Use of only MOS transistors	Yes	No	No	No	No

VI. CONCLUSIONS

The design of reference with Vref of 466.5 mV with Vdd=1.8V, temperature coefficient of 28.4 ppm/C, PSR of -30dB at 8KHz has been done successfully. This relatively low PSRR is primarily due to the diode connected transistors (M8, M9, M4) in the architecture, which create low resistance paths at the Vdd & ground rails. In addition, this is much more evident as the lower M8, M9 transistor operate in sub threshold region which in turn reduces its resistance (by increasing g_m in sub threshold region).Nevertheless, circuit has power dissipation of 3.98 µW. The proposed circuit contains 9 MOSFETs and has no resistors and BJTs. This has been done using in 0.18 µm CMOS technology. Layout is extracted in Cadence environment which is verified through DRC and LVS. Post layout simulations are presented after PEX extraction. This circuit can be efficiently used as voltage reference in the chip; also it can be used to provide bias to any of the transistors in the circuit. Circuit is tested at different loads such as resistive and capacitive. It is efficiently able to drive the loads. The architecture for reference generation presented here proves to be robust against process, supply voltage and temperature (PVT).Summary of work has been given with post layout simulations.

Summary of the work:

	Pre-Layout	Post-Layout
Technology	0.18 um CMOS	
Supply Voltage(VDD)	1.8 V	
Voltage Reference (@27^{0}C)	466.5 mV	463.46 mV
Temperature Coefficient (in ppm/^{0}C)	28.4	37.91
Power Supply Rejection (@ 8 KHZ)	-30 dB	-27dB
Layout Area	0.22 mm^2	

Post Layout Corner Simulations:

Corners	Temperature Coefficient
FF Corner	42.15 ppm/^{0}C
SS Corner	44.33 ppm/^{0}C
SF Corner	46.26 ppm/^{0}C
FS Corner	29.00 ppm/^{0}C

VII. ACKNOWLEDGEMENTS

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