A CMOS Voltage Reference Using Compensation of Mobility and Threshold Voltage Temperature Effects

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***Abstract* – A CMOS voltage reference using compensation of mobility and threshold voltage temperature effects is proposed. In this reference, the nested connection of two NMOS transistors supplies a voltage with positive temperature coefficient, and the diode-connected NMOS transistor supplies a voltage with negative temperature coefficient. These two circuits are connected in series via an operational amplifier, and the resulting voltage that appears in the output stage of this amplifier has low temperature coefficient. The calculations are verified by simulations of the reference designed in 0.13 µm CMOS technology. The simulated reference provides a voltage of about 490 mV with the variation of 1 mV in the temperature range 20 to 120°C. The reference is able to operate with sub-1V power supplies.**

Indexing terms: Voltage sources, voltage references, CMOS technology, mobility, threshold voltage, temperature compensation.

I. INTRODUCTION

A voltage reference is an important block in many analog, digital, and mixed-signal circuits and systems in microelectronics. For this purpose, bandgap reference circuits with CMOS-based vertical [1] or lateral [2] bipolar transistors are conventionally used in CMOS technologies. However, these transistors occupy large area to implement. Resistors of large area are frequently required as well. Besides, the bandgap mechanism can be used only if the supply voltage does not drop below 0.8 volts [2].

The above mentioned difficulties resulted in investigation of alternative, non-bandgap references, in particular the references based on compensation of mobility and threshold voltage temperature effects [3-7]. The proposed reference is of this type. It uses operation of transistors in strong inversion. This regime requires higher current than that of references using subthreshold operation. On the other hand, it is advantageous to use such a circuit because it uses the basic transistor models available in any CMOS process. The temperature dependencies of mobility and threshold voltages were well investigated long ago [3]. The proposed reference does not require, as in [3-5], presence of zero temperature coefficient (ZTC) point in the transistor transconductance characteristics. We are using a subcircuit that provides a voltage with positive temperature coefficient, and a diode connected transistor that provides a voltage with negative temperature coefficient. The subcircuit and diode are purposely isolated and connected via a two-stage operational amplifier, and the reference voltage appears in the amplifier output stage.

The paper is organized as follows. Section II presents the description of the core circuit of the proposed reference. Section III describes the modification of the design equations when a frequently used bias circuit is added to the core circuit. Section IV describes the modification improving the bias circuit and shows the start-up circuit used to create complete design. The simulation and layout results are described in Section V. A discussion and conclusions are drawn in Section VI.

II. REFERENCE OPERATION PRINCIPLE

The core circuit of the proposed reference is shown in Fig. 1. It includes the subcircuit with nested connected [8]

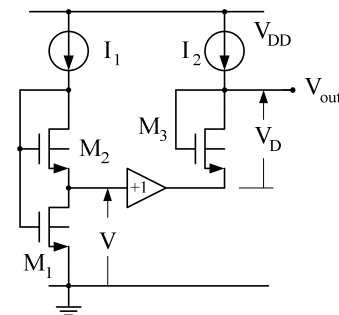

Fig.1 Core circuit of the proposed reference

transistors M_1 and M_2, the ideal unity gain amplifier, the diode connected transistor M_3, and two current sources I_1 and I_2 .

In the nested connection transistor M_1 operates in triode regime, and M_2 operates in saturation. Hence, one can write that

$$I_1 = K_1[(V_{GS1} - V_{TN})V - (V^2 / 2)] \qquad (1)$$

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and

$$V_{GS2} = V_{TN} + \sqrt{(2I_1)/K_2} \tag{2}$$

Here, and in the following $K_i = \mu_n C_{ox}(W/L)_i$, V_{TN} is the threshold voltage of NMOS transistors, and V_{GSi} ($i = 1,2$) is the transistor gate-source voltage (the body effect is neglected). In addition

$$V_{GS1} = V + V_{GS2} \tag{3}$$

Substituting (1) and (3) in (2) one obtains that

$$I_1 = K_1[\sqrt{(K_1/K_2)}\sqrt{(K_1/K_2)+1} + (K_1/K_2) + (1/2)]V^2 \tag{4}$$

Finally, inverting (4) one finds that

$$V = A\sqrt{(2I_1)/(\mu_n C_{ox})} \tag{5}$$

where $A = [\sqrt{(L/W)_1 + (L/W)_2} - \sqrt{(L/W)_2}]$.

Assume, for a while, that the current I_1 is constant. The mobility μ_n is decreasing with an increase of temperature. Hence, the voltage V is also increasing with temperature. The temperature coefficient of this voltage, hence, can be found as

$$\frac{\partial V}{\partial T} = -\frac{A}{2}\sqrt{\frac{2I_1}{\mu_n C_{ox}}}\left(\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T}\right) = -\frac{V}{2}\left(\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T}\right) \tag{6}$$

It is known [3] that $\mu_n \approx \mu_{n0}(T/T_0)^{-2}$ (7)

Substituting this result in (6) one can find that

$$\partial V/\partial T \approx V/T \tag{8}$$

To take into consideration the body effect for M2 one may consider that the threshold of this transistor is increased by

$$\Delta V_{TH} \approx (\gamma V)/(2\sqrt{2|\phi_f|}) \tag{9}$$

and reduce the voltage V in (8) by this value. The simulations show that one may neglect the temperature dependence of the body effect coefficient γ and the Fermi voltage ϕ_f and consider that

$$\frac{\partial V}{\partial T} \approx \frac{V}{T}\left(1 - \frac{\gamma}{2\sqrt{2|\phi_f|}}\right) \tag{10}$$

The voltage V_D at the diode-connected transistor M3 is equal to

$$V_D = V_{TN} + \sqrt{\frac{2I_2}{\mu_n C_{ox}(W/L)_3}} = V_{TN} + V_{ov} \tag{11}$$

where V_{ov} is the overdrive voltage. Using (7) again one finds that

$$\frac{\partial V_D}{\partial T} \approx \frac{\partial V_{TN}}{\partial T} + \frac{V_{ov}}{T} \tag{12}$$

The first term in (12) has a negative value. It is defined by the technology, and in the literature [9] one can find the figures which vary from -0.4 to -4 mV/^{o}C. This value is usually higher than $\partial V/\partial T$. But the second term is positive, and using the different values of I_2 one can adjust the coefficient $\partial V_D/\partial T$ to the value which is required to compensate $\partial V/\partial T$. Hence, the equation

$$\frac{\partial V_{out}}{\partial T} = \frac{V + V_{ov}}{T} + \frac{\partial V_{TN}}{\partial T} \approx 0 \tag{13}$$

should be satisfied in the circuit design. It is not difficult to see that (13) always can be satisfied.

The influence of the body effect of the transistor M3 may be, as with M2 above, in the first approximation, neglected as well.

III. BIASED VOLTAGE REFERENCE

A possible realization of the proposed voltage reference is shown in Fig. 2. The currents I_1 and I_2 are realized via current mirroring of the bias current I_B obtained in the well-known [10] bias circuit (transistors M4 to M7 and resistor R). The unity gain amplifier is realized as an operational amplifier with full feedback (transistors M9 to M15 and the compensation capacitor C_c). The diode-connected transistor M3 is inscribed in the second stage of this amplifier, and transistor M14 provides the current I_2 and serves as the active load of this second stage.

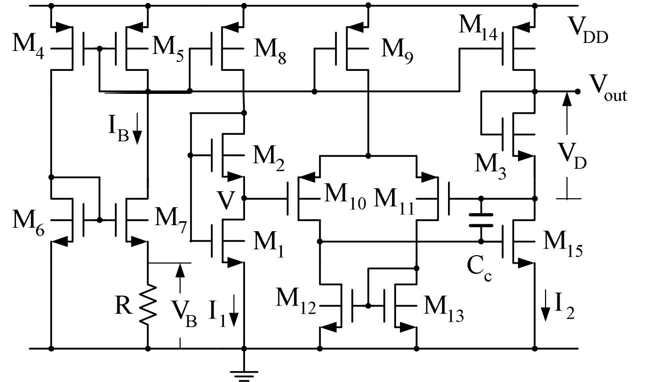

Fig. 2 Voltage reference with bias circuit

It can be shown [10] that, if the transistors M4 and M5 are matched, then the voltage V_B at the resistor R is equal to

$$V_B = B\sqrt{(2I_B)/(\mu_n C_{ox})} \tag{14}$$

where $B = [\sqrt{(L/W)_6} - \sqrt{(L/W)_7}]$. The bias current I_B, from the other side is

$$I_B = V_B/R \tag{15}$$

Substituting (15) into (14) one finds that

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$$I_B = (2B^2)/(\mu_n C_{ox} R^2) \quad (16)$$

Differentiating (16) one obtains that

$$\frac{\partial I_B}{\partial T} \approx I_B \left(-\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T} - \frac{2}{R}\frac{\partial R}{\partial T} \right) \approx -I_B \frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T} \quad (17)$$

The absolute value of the second term in the brackets of (17) is 3 to 5 times less than the first term (for the layers used to design resistors in modern technologies). As the result, the current I_B has a positive temperature coefficient. From the circuit of Fig. 2 one can find that $I_1 = I_B \frac{(W/L)_8}{(W/L)_5}$ and $I_2 = I_B \frac{(W/L)_{14}}{(W/L)_5}$. Hence, the currents I_1 and I_2 both are increasing with temperature.

Using eq. (6) and (11) and simple device scaling these temperature dependencies can be done self-compensating. The reference design requires that the temperature dependencies of mobility and threshold voltage are established by simulations. Then, when the design equation (13) is satisfied using the parameters from standard CMOS design kit, and the bias circuit is finalized, it is easy to introduce the corrections after the bias circuit simulations.

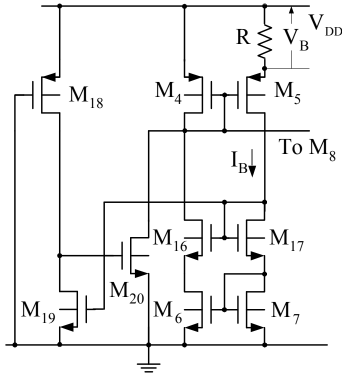

Fig. 3 Finalized bias circuit

IV. Finalized Bias Circuit

The finalized bias circuit is shown in Fig. 3. The resistor is introduced in the p-channel Widlar current source and the bottom n-channel current mirror is of cascode type. In addition this circuit includes a standard [10] start-up circuit (transistors M_{18}, M_{19}, and M_{20}).

V. Simulation Results

The voltage reference was simulated in 0.13 μm CMOS technology with the following parameters: $V_{TN} = 0.305$ V, $\mu_n C_{ox} = 260$ μA/V^2, $\mu_n = 196$ cm^2/V·sec, $\partial V_{TN}/\partial T = -0.52$ mV/^{o}C, $V_{TP} = -0.379$ V, $\mu_p C_{ox} = 82$ μA/V^2, $\mu_p = 67$ cm^2/V·sec, $\partial |V_{TP}|/\partial T = -0.48$ mV/^{o}C. For simplification, we considered that both electron and hole mobility are changing with temperature in accordance with the law $\mu \approx \mu_0 (T/T_0)^{-2}$, and the above indicated values of mobility were considered as the initial ones for the temperature $T_0 = 300\,^o$K. The body-effect coefficient is $\gamma = 0.3$ V$^{1/2}$, and the surface potential in strong inversion is $2|\phi_f| = 0.7$ V. The n-well resistor R=10 kΩ in the bias circuit has the temperature coefficient of $TC_R \approx 3 \cdot 10^{-3}$ 1/^{o}C.

Except of the transistor M_{18} in the start-up circuit which has the length of 10 μm, all other transistors in the reference have the length of 1 μm. With this length we avoided any short-channel effects and reduce offset in the operational amplifier. The widths of transistors are given in Table I. The compensation capacitor is 50 fF.

Table 1 Transistor sizes

Tr-r	M_1	M_2	M_3	M_4	M_5	M_6	M_7
W, μm	2	10	30	30	80	10	10
Tr-r	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}
W, μm	60	30	3	3	4	4	100
Tr-r	M_{15}	M_{16}	M_{17}	M_{19}	M_{20}		
W, μm	60	10	10	20	10		

The reference was simulated with nominal value of power supply 1.2 V and the temperature range -50 to 150°C. The results of simulations are summarized in Fig. 4 and Fig. 5. Fig. 4 shows the temperature characteristics of the output voltage for TT process corner. Fig. 4, a) shows the output voltage variation of 15mV (489mv to 504mv) for full temperature range with ±10% of supply voltage variation (V_{DD}=1.08v, 1.2v, and 1.32v). Fig. 4, b) gives the same characteristics for the range of supposed application of 20 to 120°C. In this case, the output voltage variation is 5mv (489mv to 494mv). Fig. 5 gives the temperature characteristics for possible design corners in CMOS130 technology with ±10% of supply voltage variation. The description of these corners is given in Table II. The result is 156mv (426mv to 582mv) for the range of 20°C to 120°C.

VI. Discussion and Conclusions

The simulations show that compensation of mobility and threshold voltage temperature effects is a viable approach of voltage references of average precision and power consumption. The reference can be designed for less than 0.8 V power supply. The provision of thermal dependencies from different subcircuits and their summation in the output stage of operational amplifier was never used before. This approach may result in new voltage references and deserves further investigation.

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The simulations also show the main deficiency of nonbandgap CMOS voltage references, namely, a strong dependence of the output voltage level on the process variation. This defect requires further attention, and design of additional circuits for the reference voltage tuning (similar to that of the bandgap references [11]).

Table II Design corners used in Fig. 5

Typical NMOS Typical PMOS	Fast NMOS Fast PMOS
Slow NMOS Slow PMOS	Slow NMOS Fast PMOS
Fast NMOS Slow PMOS	Typical NMOS Typical PMOS with Max. Resistance
Typical NMOS Typical PMOS with Min. Resistance	Fast NMOS Fast PMOS with Max. Resistance
Fast NMOS Fast PMOS with Min. Resistance	Slow NMOS Slow PMOS with Max. Resistance
Slow NMOS Slow PMOS with Min. Resistance	Slow NMOS Slow PMOS with Max. Resistance
Slow NMOS Fast PMOS with Min. Resistance	Fast NMOS Slow PMOS with Max. Resistance
Fast NMOS Slow PMOS with Min. Resistance	

REFERENCES

[1]G.A. Rincon-Mora, *Voltage References*, IEEE Press, Piscataway, NJ, 2002.

[2]K. Sanborn, Donsheng Ma, and V. Ivanov, “A Sub-1-V Low Noise Bandgap Voltage Reference”, *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2466-2481, 2007.

[3]I.M. Filanovsky, and A. Allam, “Mutual Compensation of Mobility and Threshold Voltage Temperature Effects With Applications in CMOS Circuits”, *IEEE Trans. Circuits Systems- I :Fundamental Theory and, Applications*, vol. 48, no. 9, pp. 876-884, 2001.

[4]L. Najafizadeh, and I.M. Filanovsky, “A Simple Voltage Reference using transistor with ZTC point and PTAT Current Source”, *Proc. Int. Symposium on Circuits and Systems (ISCAS’04)*, vol. 1, pp. 909-911, 23-26 May 2004.

[5]L. Najafizadeh, and I.M. Filanovsky, “Towards a Sub-1 V Voltage Reference”, *Proc. Int. Symposium on Circuits and Systems (ISCAS’04)*, vol. 1, pp. 53-56, 23-26 May 2004.

[6]De Vita, and G. Iannaccone, “A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator ”, *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1536-1542, 2007.

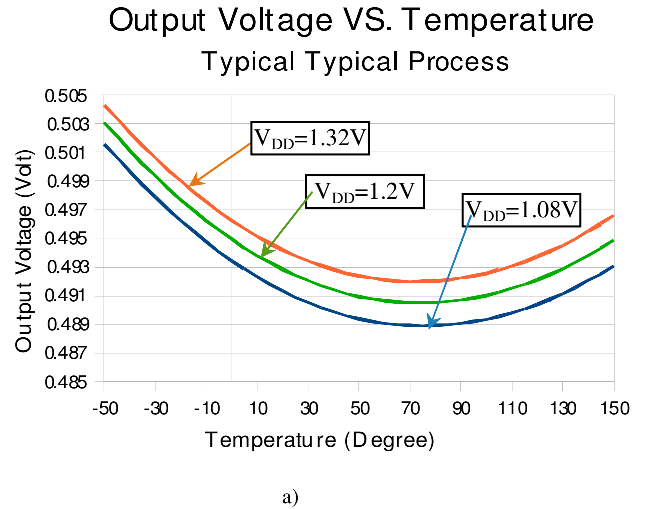
[7]H.C. Lai, and Z.M. Lin, “An Ultra-Low Temperature-Coefficient CMOS Voltage reference”, *IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC2007)*, pp. 369-372, 20-22 Dec. 2007.

[8]I.M. Filanovsky, and H.P. Baltes, Simple CMOS analog square-rooting and squaring circuits”, *IEEE Trans. Circuits Systems-I: Fundamental Theory and Applications*, vol. 39, no. 4, pp. 312-315,1992.

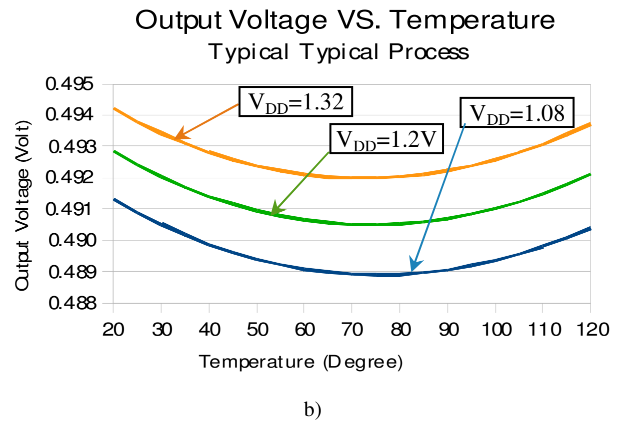
[9]P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th Ed., J. Wiley, New York, 2001.

[10]D.A. Johns, and K. Martin, *Analog Integrated Circuit Design*, New York, J. Wiley, 1997.

[11]V.V. Ivanov, I.M. Filanovsky, *Operational amplifier speed and accuracy improvement*, Kluwer, 2004.



a)



b)

Fig. 4 Temperature characteristics for TT design corner

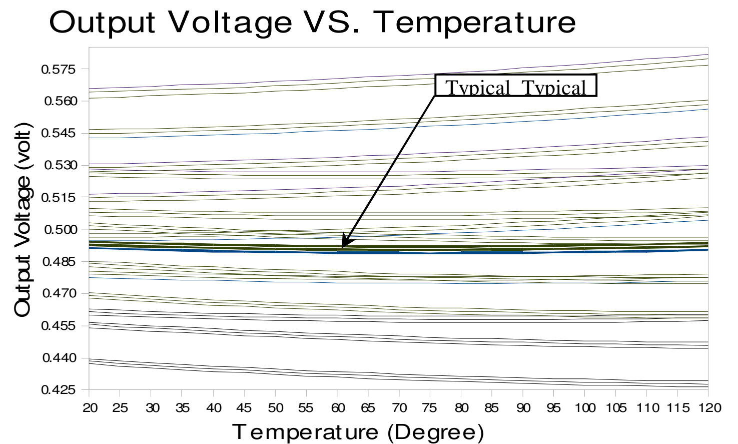


Fig. 5 Temperature characteristics for different design corners

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