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A Low-Power High-PSRR Current-Mode Microphone Preamplifier

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Abstract—Bionic implants for the deaf require wide-dynamic-range low-power microphone preamplifiers with good wide-band rejection of the supply noise. Widely used low-cost implementations of such preamplifiers typically use the buffered voltage output of an electret capacitor with a built-in JFET source follower. We describe a design in which the JFET microphone buffer's output current, rather than its output voltage, is transduced via a sense-amplifier topology allowing good in-band power-supply rejection. The design employs a low-frequency feedback loop to subtract the dc bias current of the microphone and prevent it from causing saturation. Wide-band power-supply rejection is achieved by integrating a novel filter on all current-source biasing. Our design exhibits 80 dB of dynamic range with less than $5 \mu\text{V}_{\text{rms}}$ of input noise while operating from a 2.8 V supply. The power consumption is $96 \mu\text{W}$ which includes $60 \mu\text{W}$ for the microphone built-in buffer. The in-band power-supply rejection ratio varies from 50 to 90 dB while out-of-band supply attenuation is greater than 60 dB until 25 MHz. Fabrication was done in a $1.5\text{-}\mu\text{m}$ CMOS process with gain programmability for both microphone and auxiliary channel inputs.

Index Terms—Current mode, electret microphone, low power, power-supply rejection ratio (PSRR), front-end, preamplifier.

I. INTRODUCTION

HEARING impairment affects almost 10% of individuals in the industrialized world [1]. Individuals with profound deafness are in need of cochlear implants to listen to everyday sounds. Modern bionic implants are designed to fit neatly behind the ear, requiring small low-power wide-dynamic-range front-ends with a minimum of external components and good power-supply rejection. The microphone preamplifiers discussed in this paper address the needs of such systems.

The presence of wide-band clock and telemetry signals in hearing instruments indicates the need for superb power-supply rejection in-band as well as at high frequencies. A fully analog hearing instrument must exhibit good power-supply rejection properties in all of its stages prior to rectification. Hearing instruments based on digital signal processing must also have good power-supply rejection in the analog front-end to ensure that the analog-to-digital (A/D) converter is not exposed to aliasing and distortion errors caused by high-frequency supply noise.

Wide dynamic range is needed to meet patient needs in noisy environments [2], [3]. Hearing instruments are typically limited

to 83 dB of input dynamic range by available microphone technology. That is, peak signals of 110 dB SPL and a microphone noise floor of 27 dB SPL make most hearing tasks possible.

In previous designs, high performance, low-power operation, and power-supply rejection have required a custom external electret structure [4]–[7]. In this paper, we show how to obtain high-performance specifications with ubiquitous noncustom JFET-buffered microphones.

The organization of this paper is as follows. In Section II, we discuss subminiature microphones. In Section III, we discuss our sense-amplifier topology and its anticipated benefits. In Section IV, we discuss designs based on the sense-amplifier approach. In Section V, we discuss experimental results. In Section VI, we conclude by summarizing the main contributions of this paper.

II. MICROPHONES FOR BIONIC IMPLANTS

Subminiature microphones for cochlear implants are typically self-biased MOS devices buffering the voltage from a moving electret capacitor. The output from the buffer is taken at the source of the MOS device, providing a relatively low-impedance voltage output. Fig. 1(a) illustrates the basic microphone circuit showing a depletion-mode MOSFET as the buffer device.

Many manufacturers employ such a self-biased structure to obtain insensitivity to the drain supply voltage V_{DD} . The presence of finite output resistance, however, can make the effect of supply noise on the output signal quite pronounced. This problem can be quite serious as many high-frequency signals are present in the implant environment including carriers for power transfer and communications. Feedthrough of high-frequency carriers is problematic when nonlinear elements rectify this content to in-band signal frequencies. Fig. 1(b) shows a small-signal model of the self-biased buffer structure indicating the output resistance r_O of the MOS device as well as its transconductance g_m .

The block diagram in Fig. 2, constructed from the small-signal diagram of Fig. 1(b), shows the contributing mechanisms for power-supply feedthrough. The output conductance g_o and gate capacitances contribute to power-supply tones at v_{out} . Since the gain of the buffer stage to the transduced electret voltage approaches unity, the power-supply rejection ratio (PSRR) of this topology is simply the inverse of the feedthrough function. Assuming v_{out} is grounded, the short-circuit current measured at v_{out} is due to feedthrough from drain-to-source conductance g_0 , direct capacitive feedthrough, and capacitive-divider and JFET transconductance interaction. These three terms determine i_{sc} , as shown in Fig. 2. The output

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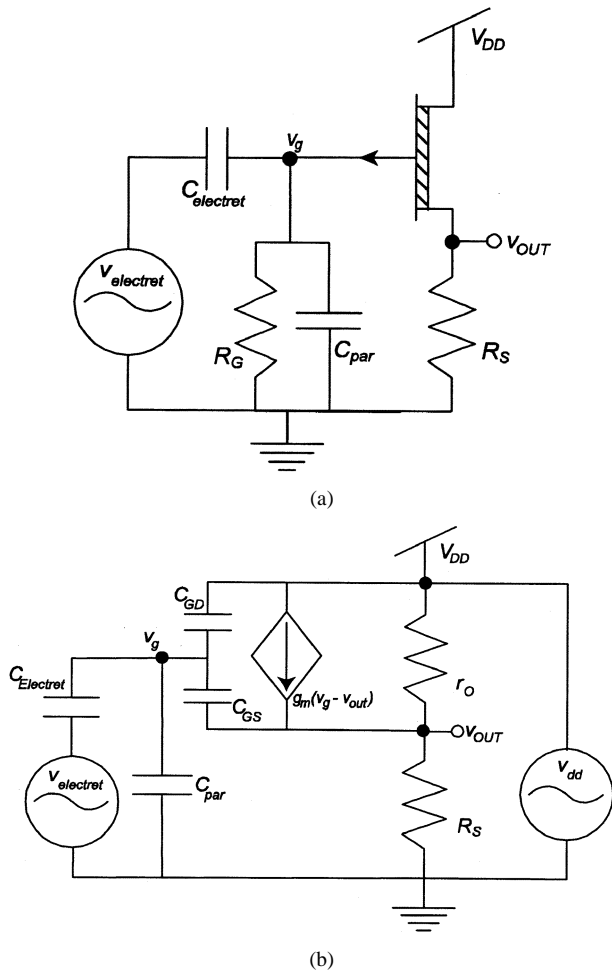


Fig. 1. Subminiature electret circuit. (a) Low-noise depletion-mode FET device shown with source resistance R_S . A large gate resistance is also shown to indicate that the gate is incrementally grounded at low frequency. (b) Small-signal model of the internal structure of the microphone, including the active device and parasitic gate and source resistances.

impedance measured at v_{out} with v_{dd} and v_{in} grounded is given by the feedforward block, $1/(sC_{GS} + g_m + g_0 + g_S)$ if we ignore the $g_m v_g$ term of the dependent source. Including the $g_m v_g$ term of the dependent source adds a feedback block from the output with gain sC_{GS}/C_T as shown in Fig. 2. Combining all these effects and using Black's formula for feedback loops, we get

$$\frac{v_{out}}{v_{dd}} = \frac{\left(g_0 + \left(\frac{C_{GD}}{C_T}\right)(g_m + sC_{GS})\right)}{(g_m + g_S + g_0 + sC_{GS}) - \left(\frac{C_{GS}}{C_T}\right)(g_m + sC_{GS})} \approx \frac{(C_{GD})}{(C_{GD} + C_{Electret} + C_{par})} \quad (1)$$

where $C_T = C_{GS} + C_{GD} + C_{Electret} + C_{par}$. In many cases, a large FET structure, used to get low-noise operation, results in a large gate-to-drain capacitance. As (1) shows, the large gate-to-drain capacitance results in capacitive feedthrough of the supply to the output, directly and via the g_m generator. The challenge of designing high-PSRR front-ends without redesigning the internal structure of modern subminiature microphones requires thorough design efforts. While some designs do away with the

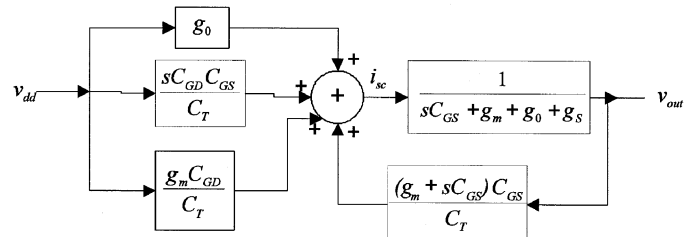


Fig. 2. Conceptual block diagram of the power-supply noise feedthrough. The summer indicates the summing of currents contributing to the source node of the FET buffer.

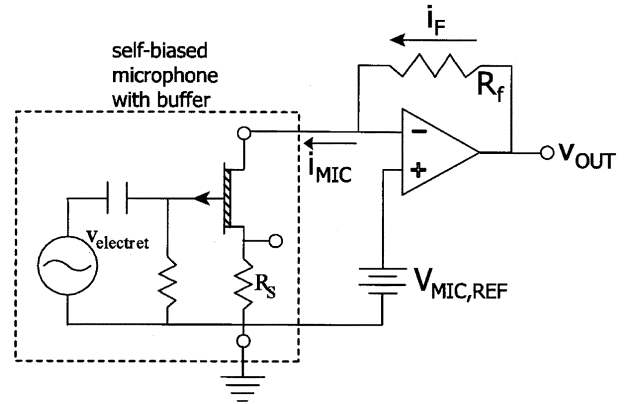


Fig. 3. A sense amplifier can be used to bias the drain of the buffer JFET as well as provide pre-amplification.

FET buffer [5], it is clear that this design choice requires manufacturing modifications which are not available to low-cost producers. In this paper, we describe designs for supply voltages of 2.8 V. This supply voltage is common for cochlear implants while hearing aids typically operate at lower supply voltages of 1–1.5 V.

The microphone used for this work, a Knowles FG-3329A, has an operating drain voltage range of 0.9–1.6 V and draws 15–30 μA from the supply. The source resistance, R_S , was measured to be 20 k Ω . Internal gate-to-source and gate-to-drain capacitances were found to be roughly, 160 and 120 pF, respectively, while measurements of the capacitance at the gate node, including the electret, yield $C_T \sim 1$ nF. The measured power-supply rejection was 22 dB. The total noise from 100 Hz to 10 kHz is less than 4 μV_{rms} at the output node v_{out} .

III. SENSE-AMPLIFIER TOPOLOGY

A conceptual solution to supply rejection problems is shown in Fig. 3. A self-biased microphone structure can be configured as the input to a sense amplifier allowing voltage regulation of the drain node. Essentially, we sense the current from the microphone, rather than its voltage, and convert this current to an output voltage through R_f . The larger the value of R_f , the larger the sensitivity of the output to sound. Traditional inverting-configuration voltage amplifiers amplify their noise because of input impedance at the inverting node. The sense amplifier avoids this condition by using current directly from the microphone and maintaining high impedance at the inverting node.

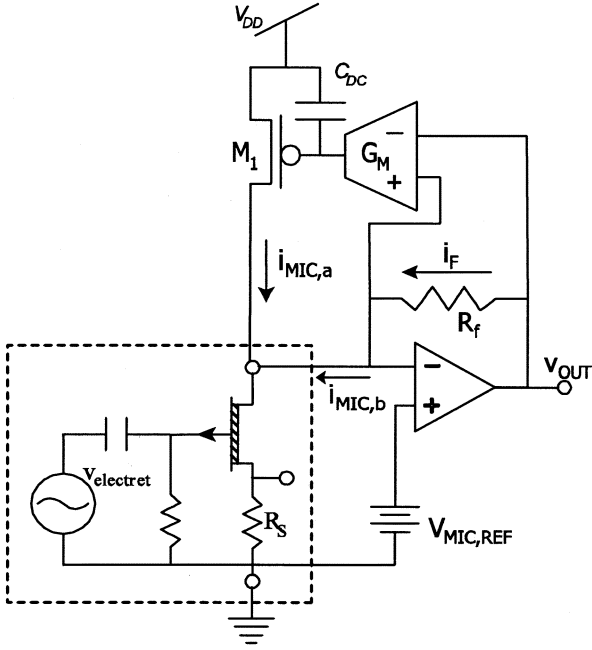


Fig. 4. Sense amplifier topology employing split-frequency feedback. The dc voltage drop in the feedback load is proportional to the dc output current of the amplifier and is regulated to zero by canceling the microphone buffer's dc current with feedback dc current from M_1 .

Biasing current for the microphone flows through the feedback load R_f such that $v_{out} = V_{MIC,REF} + i_f R_f$. Referring this new output to the normal output of the buffer v_{buf} , we obtain

$$\frac{v_{out}}{v_{buf}} = \frac{i_{MIC} R_f}{i_{MIC} R_S} = \frac{R_f}{R_S}. \quad (2)$$

Front-end gain or sensitivity can be programmed by selecting the feedback impedance R_f . The gain matching of this topology is determined by the relative matching of the in-built FG-3329 source resistor and our feedback resistor R_f . Our experiments indicate that such matching is quite good across several microphones to within 5%.

More generally, the feedback resistor can be replaced by a two-port network, Y_f , whose current at the input side and at the output side is a linear function of the voltages at the input and output sides. Since the microphone buffer current is comprised of a large dc component I_{MIC} , the output linear range of the operational amplifier in the sense amplifier is degraded by the voltage drop, $I_{MIC} R_f$. To make high gain possible while preserving linear range, we introduce a split-frequency feedback topology that is not subject to this tradeoff.

As the microphone bias current only changes slowly with time, a slow feedback loop can be set up to subtract the dc bias current of the microphone without affecting the normal ac operation of the sense amplifier. The slow loop then ensures that there is no sensing of the dc current from the microphone while the normal fast sense-amplifier loop transduces the ac current from the microphone into an output ac voltage. Using active feedback avoids having to use a large capacitor to decouple the dc operation of the microphone drain node. Fig. 4 shows how this approach retains the benefit of our current-mode scheme.

Fig. 4 shows that by driving the dc drop across the sense-amplifier resistor to zero with feedback, we can subtract the bias

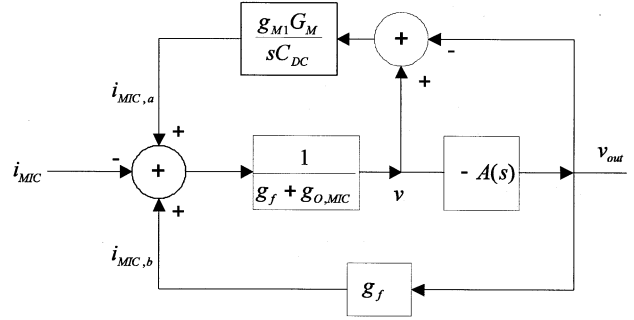


Fig. 5. Small-signal block diagram for the design presented in Fig. 4.

current of the microphone and prevent it from causing saturation effects in the operational amplifier. The cancellation of the dc output current can be imperfect without seriously degrading performance. A feedback block diagram indicating both low-frequency and high-frequency loops in Fig. 4 is shown in Fig. 5. Because the low-frequency loop can be made arbitrarily slow, its dynamics can be designed so as to not interfere with the high-frequency loop stability. Stabilizing the overall system can then be done without considerations for the performance of the low-frequency biasing loop. It is worth noting that microphone response to unwanted low-frequency vibrations can be reduced through selection of the dynamics of the low-frequency loop.

An additional advantage of this approach lies in the flexibility it affords in the choice of feedback elements. If frequency-dependent feedback is to be used, it is no longer required to carry appreciable dc current. If high-pass filtering is desired, as in pre-emphasis filters, a two-port network can be used.

IV. POWER-SUPPLY REJECTION

For obvious reasons, rejection of power-supply noise is a major design constraint for low-noise systems. A variety of nonideal properties of signal processing systems can contribute to signal degradation. In an all-analog signal processor, rectification and distortion can increase in-band noise drastically through mixing of high-frequency power-supply noise [8]. In digital implementations, power-supply noise picked up at the front-end can result in extensive aliasing in the A/D output. Both of these effects indicate the need for broad-band power-supply rejection in the front-end system. While in-band power-supply rejection typically is achieved by employing high-gain feedback, as in our sense-amplifier topology, such feedback only helps when the power-supply noise is modeled as an output disturbance that the feedback attenuates. Indeed, past the closed-loop crossover frequency ω_{CL} , noise from the supply is contributed with little attenuation. From this perspective, it is critically important to implement filters to limit the total amount of power-supply noise accumulated in the out-of-band region.

Since in-band power-supply rejection is accomplished with high-gain feedback which we have already implemented with the sense-amplifier topology, we will focus on filtering of high-frequency supply noise. Several strategies to achieve better noise filtering can be considered. First, we can filter the supply directly, loading the entire supply network with passive elements. Most filters of this type can be implemented with

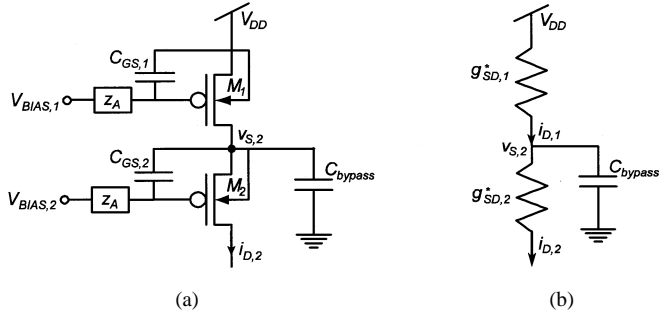


Fig. 6. Power-supply decoupling mechanism. (a) Explicit gate-source capacitors, $C_{GS,1}$ and $C_{GS,2}$, and biasing of p-gates through high-impedance elements, z_A , make M_1 and M_2 behave as small-signal large resistances. (b) A bypass capacitance C_{bypass} filters the supply voltage before it can affect the bias at $i_{D,2}$.

inductors. Typically, these inductors are prohibitively large for operation at the frequencies of interest and resistive-and-capacitive filters need to be employed. The dc drop produced in resistive-and-capacitive filters can be minimized by using small resistors. Low cutoff frequencies demand a correspondingly larger capacitor, making the filter unsuitable for a small-size solution.

Filtering of high-frequency noise at the output of the analog gain stage, before the A/D conversion, is not without challenges as well. Since the output signal of this stage has been given sufficient gain to drive the full-scale input range of the A/D processing system, it is a significant fraction of the supply range. A filter at this stage would require wide dynamic range to handle the large output signals.

Our approach to power-supply filtering is shown in Fig. 6(a), which illustrates how we build a supply-bypassing current source. The bias device M_1 is biased through the large impedance z_A , forming a low-pass filter with the gate-source capacitor $C_{GS,1}$. We implement the element z_A with two parallel diodes with opposite polarity. Our strategy yields a dc current source with little response to changes in its source voltage [9].

We will now explain how the power-supply filtering is obtained. Fig. 7 outlines a block diagram showing a small signal representation of the bias device M_1 . Effectively, the whole device may be replaced by a small-signal conductance of value $g_{ds,1}$ given by

$$g_{ds,1} = \frac{i_{d,1}}{v_{dd}} = \left(\frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} \right) g_{m,1} + \left(\frac{1}{r_o} \right) + s \left(C_{BD,1} + \frac{C_{GD,1} C_{GS,1}}{C_{GD,1} + C_{GS,1}} \right). \quad (8)$$

As $C_{GS,1} \gg C_{GD,1}$ and $(1/r_o)$ is small, (8) can be approximated as

$$g_{ds,1} \cong \left(\frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} \right) g_{m,1} + s(C_{BD,1} + C_{GD,1}). \quad (9)$$

The drain capacitances of the bias device, $C_{GD,1}$ and $C_{BD,1}$, limit the isolation of output current $i_{d,1}$ from variations in the supply voltage v_{dd} . The gate-to-drain capacitance limits the real output impedance of the device by dominating the contribution to $g_{sd,1}$ over the $(1/r_o)$ term in (8). Both the gate-to-drain and the bulk-to-drain capacitances contribute to

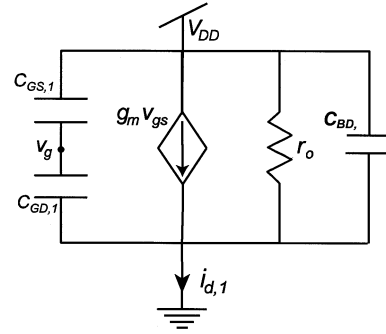


Fig. 7. Small-signal model of M_1 in Fig. 10.

high-frequency feedthrough as the last term in (8) and (9). Making the gate-to-source capacitance artificially large with an explicit capacitor will help to attenuate the first feedthrough term in the right-hand side of (9). To provide additional filtering, a second device M_2 in parallel with a filter capacitor C_{bypass} can be used to obtain low-pass filtering at the intermediate node $v_{s,2}$. The overall filter characteristic for the output current $i_{d,2}$ can be approximated from (9) and Fig. 6(b). Ignoring the large output resistance r_o and the drain capacitances $C_{BD,1}$ and $C_{GD,1}$, and approximating g_{sd} for M_1 and M_2 as having purely resistive components, we get

$$g_{sd,1}^* = \frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} g_{m,1} \quad (10)$$

$$g_{sd,2}^* = \frac{C_{GD,2}}{C_{GD,2} + C_{GS,2}} g_{m,2}. \quad (11)$$

We find the admittance from the supply is

$$g_{supply} = \frac{i_{d,2}}{v_{dd}} = \left(\frac{g_{sd,1}^* g_{sd,2}^*}{g_{sd,1}^* + g_{sd,2}^* + s C_{bypass}} \right). \quad (12)$$

The low-pass filtering effect of the bypass capacitor is clear in (12). If the parasitic drain capacitances of both devices are included as $C_{D,i} = C_{GD,i} + C_{BD,i}$ (assuming $C_{GS} \gg C_{GD}$ in Fig. 7), a limit to the maximum supply rejection is observed from computing the overall supply coupling

$$g_{supply} = \frac{i_{d,2}}{v_{dd}} = \frac{(g_{sd,1}^* + s C_{D,1})(g_{sd,2}^* + s C_{D,2})}{g_{sd,1}^* + g_{sd,2}^* + s(C_{D,1} + C_{D,2} + C_{bypass})}. \quad (13)$$

Two zeros result from the feedthrough caused by the drain capacitances. The pole arises from the high-impedance bypass node produced by both p-devices. By choosing C_{bypass} to be larger than the parasitic drain capacitances, the pole can be made to dominate at lower frequencies, reducing the supply sensitivity at the high-impedance node, $v_{s,2}$ in Fig. 6. At frequencies higher than the corner frequency of this filter, the source voltage at the bypass capacitor has limited attenuation from the supply

$$\begin{aligned} \frac{v_{s,Min}}{v_{dd}} &= \frac{C_{GD,1} + C_{BD,1}}{C_{bypass} + C_{GD,2} + C_{GD,1} + C_{BD,1} + C_{BD,2}} \\ &\cong \frac{C_{GD,1} + C_{BD,1}}{C_{bypass}}. \end{aligned} \quad (14)$$

Consequently, it is desirable to make the bypass capacitance as large as possible to ensure the best filtering at high-frequencies.

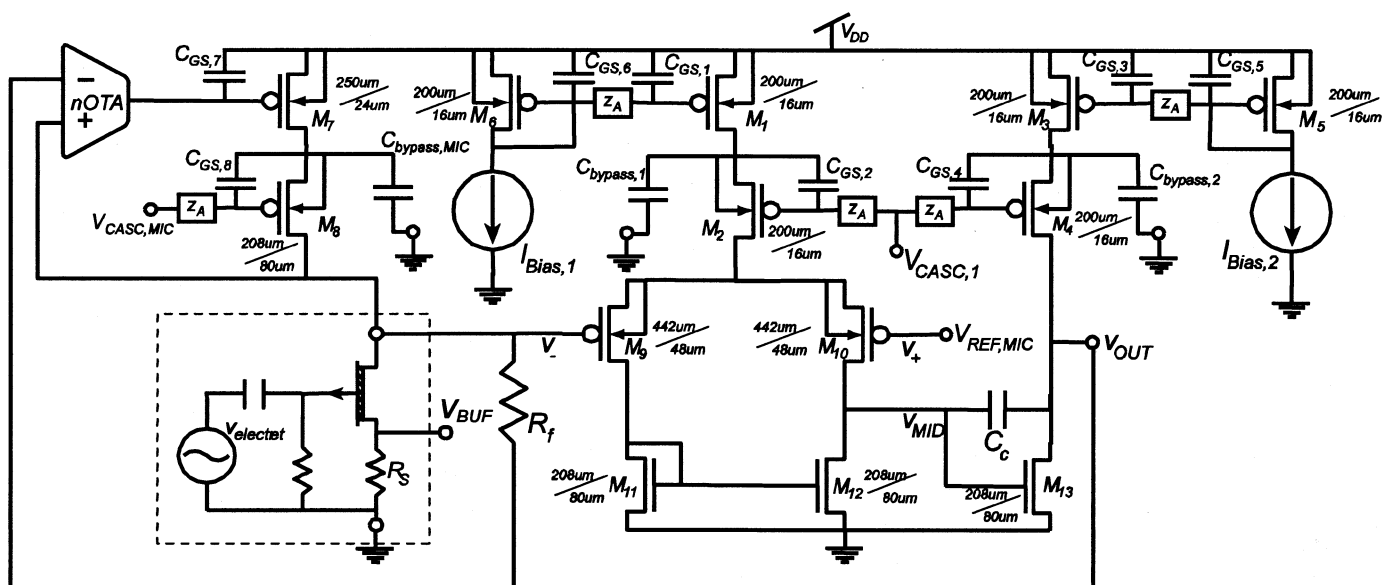


Fig. 8. Complete circuit topology including the supply decoupling networks. The microphone structure is shown at the bottom left in the dashed box.

Due to the presence of a second saturation-region device in the current source of Fig. 6, its available output voltage range is reduced by our technique. However, supply rejection up to frequencies present in the digital or telemetry system can be achieved if the system supply voltage is not prohibitively low, making our design choice worthwhile. On our 2.8-V power supply, we were able to obtain good power-supply rejection without losing headroom, as our experiments in Section V show.

V. EXPERIMENTAL RESULTS

Our pre-amplifier and microphone circuitry were fabricated on MOSIS AMI's 1.5- μm SCMOS process. Fig. 8 indicates the two-stage topology of the operational amplifier and the overall pre-amplifier circuit. A 2.8-V supply provided power for the circuits and a Knowles Electronics FG-3329 microphone was used. Fig. 8 also shows the resistive feedback R_f and supply decoupling structures in the drain circuits. The use of supply filters in all supply biasing was found to be critical for high-frequency rejection performance. The pMOS input stage is comprised of differential-pair transistors M_9 and M_{10} , current-mirror transistors M_{11} and M_{12} , and supply-decoupling current-source devices M_1 and M_2 . Three such current sources are shown. Transistors M_7 and M_8 bias the microphone buffer and sense node. The output of the first stage drives M_{13} in the second output stage. Bypass capacitors were shunted to ground, although another quiet reference could be used. Fig. 9 shows a die micrograph of the circuits.

The input stage of the operational amplifier was biased at 6 μA . The input devices were chosen to obtain a $1/f$ noise corner near 100 Hz. Compensation of the two-stage amplifier was done with the most robust parasitic conditions in mind—the microphone and auxiliary inputs present capacitive loads to the sense node, deteriorating the phase margin of the closed loop. Biasing of the second stage was done to ensure load-drive capability for subsequent stages—typically, 100 pF. Total power con-

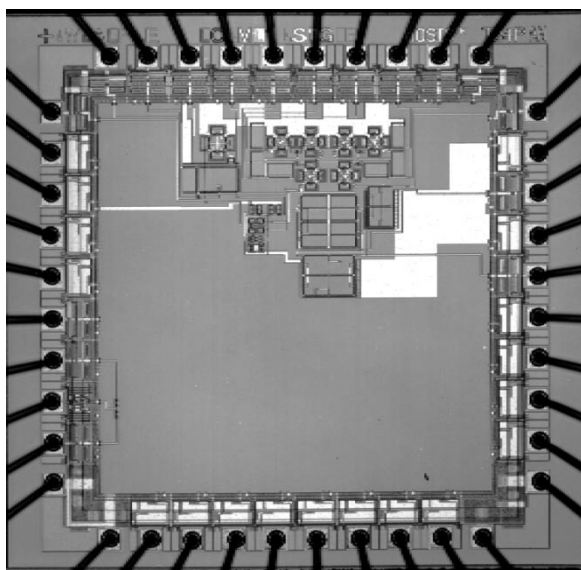


Fig. 9. Die photo of the current-mode pre-amplifier. The chip is a 2.2-mm \times 2.2-mm chip built in a 1.5- μm process.

sumption for the two-stage amplifier was 34 μW . The feedback n-OTA was biased with 1–3 nA while the high-frequency feedback element R_f was chosen around 300 k Ω . The microphone operates at approximately 20 μA , adding almost 60 μW to the power consumption. Total power consumption was measured at 94 μW . To provide the $V_{\text{MIC,REF}}$ reference voltage, an off-chip reference was used. The voltage reference may be constructed on-chip with a power consumption less than 1 μW with standard bandgap reference techniques and more than 60–80-dB PSRR. However, the data shown in this paper were obtained with an off-chip reference.

A. Gain

The top curve in Fig. 10 shows the acoustic gain referenced to the in-band microphone-buffer sensitivity. The FG-3329 has

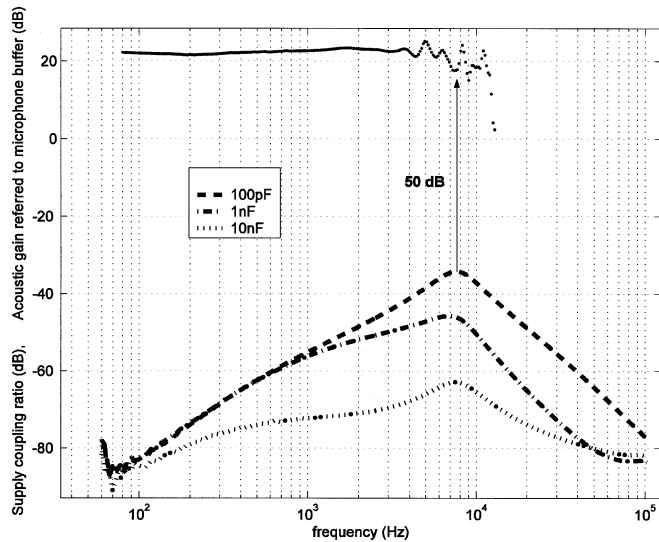


Fig. 10. Frequency response to acoustic excitation with the output supply coupling response normalized to $1\text{-}V_{PP}$ variation of the supply. The supply rejection performance for various bypassing capacitances is shown.

an in-band sensitivity of 17 mV per Pascal at the v_{buf} output in Fig. 3. Thus, in the top curve of Fig. 10, a gain of 20 dB corresponds to 170 mV/pascal. The measured gain was calibrated with respect to a reference microphone in an anechoic environment. The reference microphone and acoustic environment were calibrated Bruel & Kjaer 4232/4188 systems. At frequencies above 10 kHz, the flatness of the reference microphone degraded. Consequently, the gain calibration exhibits peaks and troughs at high frequencies.

B. Power-Supply Rejection

The PSRR for our system is the ratio of the voltage gain from v_{buf} to v_{out} with respect to the voltage gain from v_{dd} to v_{out} in Fig. 3. Note that v_{dd} is not explicitly shown in Fig. 3 but is used to power the operational amplifier. The voltage gain from the supply v_{dd} to the output v_{out} is the sensitivity of the system to supply variations and is shown as the bottom curves of Fig. 10. The top curve of Fig. 10 is the voltage gain from v_{buf} to v_{out} for the inband audio frequencies. Thus, the PSRR in decibels may be directly read off as the difference between the top and bottom curves of Fig. 10 for various values of C_{bypass} . At 300 Hz, 90 dB of PSRR is observed, and at 8 kHz, 50 dB of PSRR is observed. Near 10 kHz, the injection of supply noise current excites second-order dynamic behavior in the overall sense amplifier, producing a peaking effect.

To ensure that supply filtering is occurring properly, feedthrough data were taken up to 26 MHz. This high-frequency rejection data is shown in Fig. 11. As expected, feedthrough effects flatten out at frequencies higher than the dynamics of the supply filter, indicating that the bypass capacitance is dominating the voltage attenuation at the high-impedance filter nodes. Varying the bypass capacitance C_{bypass} changes the attenuation ratio directly, as shown in Fig. 12. The key factor to note is that potential clock and telemetry frequencies, i.e., greater than 2 MHz, are reasonably attenuated even with small capacitances, i.e., with C_{bypass} of

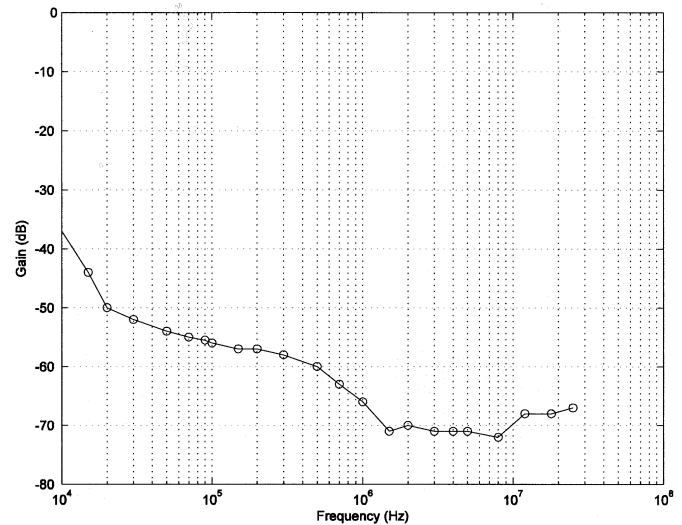


Fig. 11. Supply coupling for frequencies up to 26 MHz.

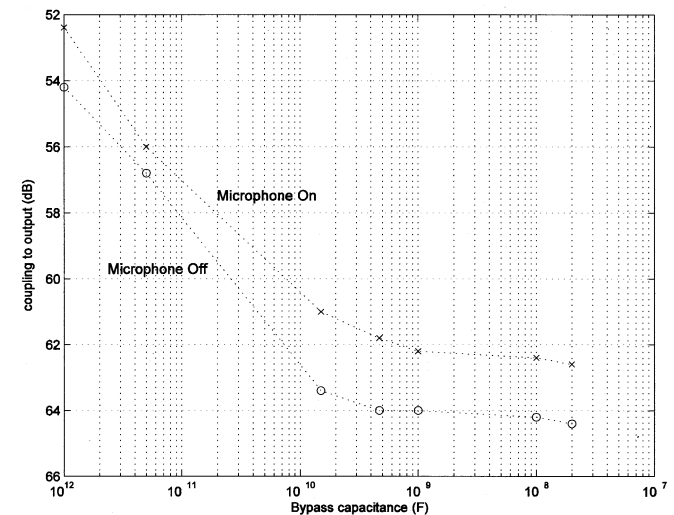


Fig. 12. High-frequency signals are filtered most effectively from the output in the presence of a large bypass capacitor. A static protection resistor in the chip's pads limited the attenuation of the decoupling path to -64 dB.

100 pF. A rough estimate of the parasitic drain capacitance $C_{GD,1} + C_{BD,1}$ contributing to feedthrough is estimated at 28 fF. Beyond bypass capacitances of 500 pF, the coupling to the output does not decrease significantly. This result arises from a static protection resistor built into our chip's pads that limited attenuation.

C. Noise Performance

Fig. 13 indicates the noise performance of the front-end with and without the microphone contribution. The lower trace indicates output noise while the microphone is off. While the microphone is on, the upper trace is obtained. This confirms that the overall noise performance is not limited by the operational amplifier but by the microphone and low-frequency biasing network. The low-frequency feedback network was designed to provide little noise contribution to the sense node. In addition, we confirmed that the output noise of the overall preamplifier was dominated by the amplified noise of the JFET buffer output.

TABLE I
NOISE AND LINEAR RANGE PERFORMANCE

Condition	Total Output Noise (100Hz – 10kHz) (Vrms)	Total Input Noise (100Hz – 10kHz) (Vrms)	Maximum Output Range for 1% Distortion (Vrms)	Maximum Input Range for 1% Distortion (Vrms)
Microphone at 20dB gain Auxiliary Off	52uVrms	5uVrms	530mVrms	52mVrms
Microphone off Auxiliary at 20dB gain	48uVrms	4.8uVrms	510mVrms	51mVrms
Microphone and Auxiliary at 20 dB gain	~ 100uVrms	~ 10uVrms	510mVrms	51mVrms

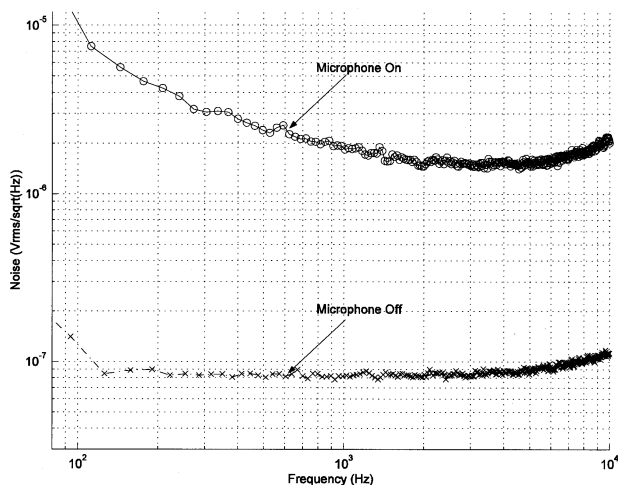


Fig. 13. Without microphone noise, feedback and operational amplifier contribute 80–90 nV_{rms}/sqrt(Hz). The microphone buffer noise dominates when audio input is on. The 1/f nature of the microphone-on characteristic is due in part to the 1/f noise of the dc biasing structure.

Total output noise is 52 μV_{rms} from 100 Hz to 10 kHz. Referred to the microphone-buffer output/input, this yields an input-referred total noise of 5 μV_{rms} from 100 Hz to 10 kHz.

An auxiliary voltage-mode input to the sense amplifier can be added by sourcing voltage to the sense node through a resistor R_{AUX}. Noise in the presence of this auxiliary channel was also measured. For a voltage-voltage gain of 20 dB, the total output noise is 48 μV_{rms} from 100 Hz to 10 kHz for an R_{AUX} of 30 kΩ. Referred to the microphone-buffer output/input, this noise yields an input-referred total noise of 4.8 μV_{rms} from 100 Hz to 10 kHz.

D. Linear Range

The output voltage linear range was limited by the power-supply rejection networks. A total harmonic distortion metric of 1% was chosen for best audio performance. A maximum output signal amplitude of 530 mV_{rms} was obtained for 100-Hz-to-3-kHz operation with less than 1% distortion. Above 3 kHz, second-order distortion due to feedthrough in the low-frequency bias loop was observed. In Figs. 14 and 15, the transition between the well-behaved distortion characteristics and high-frequency effects are shown.

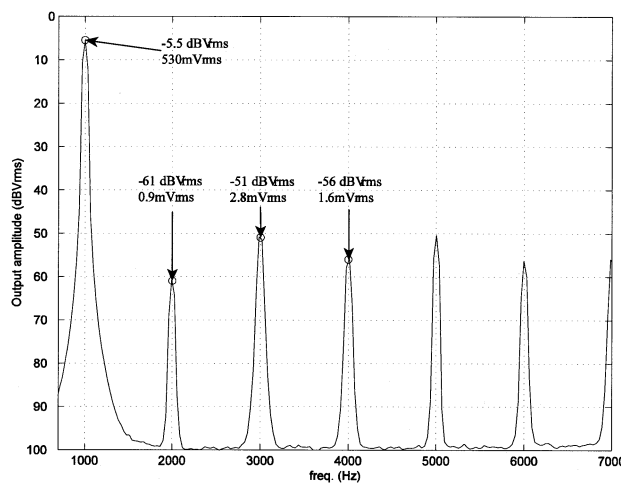


Fig. 14. Distortion products for 1-kHz peak output with 1% distortion.

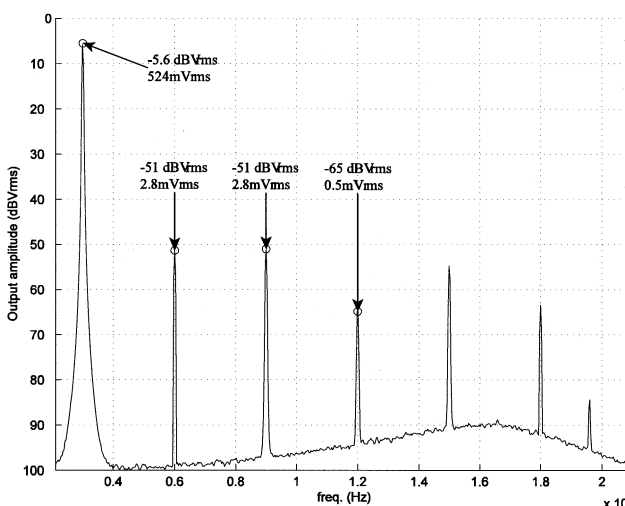


Fig. 15. Distortion products for 3-kHz peak output with 1% distortion.

Fig. 16 indicates the dynamic range as a function of frequency for the microphone transduction system for 1% distortion limits and a minimum detectable signal of 5 μV_{rms} as a function of frequency. The dynamic range varies from 82 to 78 dB from 100 Hz to 10 kHz. Linear range and noise performance are summarized in Tables I and II.

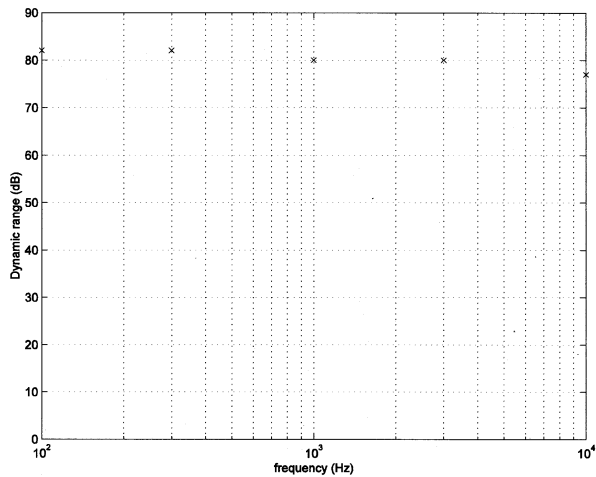


Fig. 16. Dynamic range versus frequency for acoustic inputs.

TABLE II
PERFORMANCE SUMMARY

Specification	Measured
Power Consumption	96 μ W
Dynamic Range at 1% distortion	80dB
Minimum Detectable Signal	5.2 μ Vrms (microphone on) 4.8 μ Vrms (auxiliary on)
PSRR in-band	> 50dB – 90dB
Gain Flatness (auxiliary input)	1dB

VI. CONCLUSION

Cochlear implants with telemetry and mixed-signal processing require versatile low-power and broad-band supply-resilient transduction for input signals. Our 94- μ W 80-dB current-mode sense-amplifier topology addresses these needs by implementing pre-emphasis filtering and dc-biasing control, and achieving an in-band supply rejection of 50–90 dB. A simple power-supply filtering network makes broad-band supply-independent operation possible well into the range of tens of megahertz. Our topology is useful for pre-amplifying sound from buffered electret microphones that are widely used in cochlear implants.

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REFERENCES

- [1] National Health Interview Survey, National Center for Health Statistics, no. 188, ser. 10, 1994. Table 1.

- [2] P. C. Loizou, "Introduction to cochlear implants," *IEEE Eng. Med. Biol. Mag.*, vol. 18, pp. 32–42, Jan.–Feb. 1999.
- [3] B. Kuszta, "Silicon cochlea," in *Proc. IEEE Wescon'98*, 1998, pp. 282–285.
- [4] W. A. Serdijn, A. C. van der Woerd, J. Davidse, and H. M. van Roemund, "A low-voltage low-power fully-integratable front-end for hearing instruments," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 920–932, Nov. 1995.
- [5] J. Silva-Martinez and J. Sorge-Suner, "A CMOS preamplifier for electret microphones," in *Proc. 38th Midwest Symp. Circuits and Systems*, vol. 2, 1996, pp. 1018–1021.
- [6] A. C. Plugers, "A novel microphone preamplifier for use in hearing aids," *Analog Integrat. Circuits Signal Process.* 3, pp. 113–118, 1993.
- [7] G. Nicollini and C. Guardiani, "A 3.3-V 800-nVrms noise, gain-programmable CMOS microphone preamplifier design using yield modeling technique," *IEEE J. Solid-State Circuits*, vol. 28, pp. 915–921, Aug. 1993.
- [8] M. Awipi and A. Al-Smadi, "Effect of analog and digital signal conditioning filters on signal to noise ratio," in *Proc. IEEE Southeastcon'91*, vol. 1, 1991, pp. 65–69.
- [9] M. G. O'Halloran and R. Sarpeshkar, "A low open-loop gain, high-PSRR, micropower CMOS amplifier for mixed-signal applications," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, 2002, pp. 424–427.
- [10] L. J. Stotts, "Introduction to implantable biomedical IC design," *IEEE Circuits Devices Mag.*, vol. 5, pp. 12–18, Jan. 1989.



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