Abstract: Integrated optical components on the silicon platform and optically enhanced electronic sampling circuits enabling the fabrication of various electronic-photonic A/D converter chips that surpasses currently available technology in speed and resolution are demonstrated.

Keywords: Electronic photonic integrated circuits; silicon photonics; high index contrast; optical sampling; optical analog-to-digital conversion; integrated femtosecond lasers.

Introduction
Rapid progress in CMOS technology combined with advances in parallel computing architectures has made Teraflop digital processors a reality. However, the wealth of new system capabilities offered by such processors cannot be fully exploited due to the limited performance of analog-to-digital converters (ADC). ADC performance at high sampling rates is fundamentally limited by the timing jitter of the electronic clocking circuits, typically a quarter of a picosecond or higher. However, optical clock pulses from a mode-locked laser (MLL) exhibit femtosecond timing jitter; thus using photonic sampling has the potential for order-of-magnitude improvement in ADC performance. The goal of this program is to leverage the low jitter properties of mode-locked lasers to develop an electronic-photonic integrated circuit (EPIC) that facilitates high speed ADC beyond the bottleneck set by electronic jitter. Photonic analog-to-digital conversion techniques have been the subject of extensive research in recent years [1,2,3].
The technological roadmap requires the development of a number of devices: low-loss waveguides in high-index-contrast materials (HIC) support higher densities of photonic components and larger free spectral range (FSR) optical resonators; WDM filters that can be tuned dynamically; wideband optical modulators, Ge-photodetectors, femtosecond lasers and novel optically controlled sampling techniques. All these devices and techniques must be integrated on a CMOS compatible technology platform. In the following we discuss progress made towards some of the key components for this optoelectronic sampling technology.

**HIGH INDEX CONTRAST FILTER BANK**

Microring resonators were first proposed as integrated optical wavelength filters by Marcatili in 1969 [6]. Applications that envision complex EPIC functionality such as the proposed ADC chip call for dense optical integration, and require microrings with low loss, a large free spectral range (FSR), and a drive to wavelength-scale resonator sizes. The latter two of these three key requirements invariably call for implementation in high-index contrast (HIC) material systems.

The microring resonator filter design used for fabrication of the WDM filter banks for the proposed ADC converter is very similar to the design discussed in [7]. By utilizing this design with the HIC materials of silicon-rich silicon nitride (n =2.2 @ 1550 nm) and silicon dioxide (n =1.455 @ 1550nm) a very wide FSR of 20 nm is realized. The filter design was optimized to achieve the objective of a 3 dB bandwidth of 50 GHz and less than 30 dB crosstalk for 150 GHz spaced channels. The critical feature size of the gap between the bus and ring waveguides is 160 nm for these filters (Figure 2a).

Direct-write scanning electron beam lithography (SEBL) was used due to its combination of high resolution and high level of dimensional control. The basic fabrication process used is similar to that described in [8].

The resonant frequency of HIC microring resonator filters requires an extremely high level of dimensional control. For the writing technique used, the discrete step sizes are limited to 6 nm and 12 nm for the ring radius and ring waveguide width respectively. To overcome this discretization e-beam dose modulation is used [9]. This technique combined with changing the radius was used to make 8-channel second order filter banks with channel spacing of 90, 104, 120, 140, 145, 150, 155, 160, and 180 GHz to demonstrate our ability for fabricating filter banks with precisely controlled channel spacing, see Figure 3.

It turns out that both the radius (R) and the effective index (n_{eff}) can be controlled with lithography. R is simply controlled by changing the radius of the ring in the design layout whereas n_{eff} can be controlled by changing the width of the ring waveguide.

Detailed optical transmission measurements show that the bandwidth of the filter response is 46.5 GHz, an average channel spacing of 159 GHz, a drop loss averaged over 40 filters of 1.5±0.5 dB and a crosstalk of less than -30 dB. Tuning of the filters to an exact frequency grid by thermal heaters or micro electromechanical devices is in progress.
159 GHz channel spacing. Frequencies are all relative to 1540 nm.

HIGH SPEED SILICON MODULATOR

For the high speed electro-optical modulator the well known plasma dispersion effect in silicon shall be exploited [10,11,12]. Here, we further improve a design based on HIC silicon buried waveguides with minimum optical loss and small figure of merit (FOM)\(= \frac{V}{\pi L} \) [13].

A schematic layout of the proposed Mach-Zehnder modulator is shown in Figure 4(a), and Figure 4(b) shows the electrically driven phase modulator section consisting of forward biased p''n''-sections. Under strong forward bias the carriers drift at nearly the silicon saturation velocity, \(v = 10^7 \text{ cm/s} \). The high velocity of the carriers increases the modulator bandwidth \(f_{3dB} = \frac{2.2}{2\pi \tau} \), where \(\tau \) is the travel time through the intrinsic region \(\tau = \frac{w}{v} \), beyond the value set by the carrier lifetime. Therefore, the modulation speed can be high because the width of the waveguide is sub-micron for the case of a silicon waveguide. We investigated different waveguide structures, with different doping profile and concentrations, see Fig. 4(b) to achieve optimum modulator performance.

The modulation bandwidth is increased by moving the highly doped P''N'' regions in the waveguide as close as possible to the optical mode by decreasing the length of the undoped region \(w_r \) from structure A to structure B. However, structure B then leads to high optical losses and an optimum in terms of low loss and high frequency response is found with structure C where the sidewalls of the waveguide are only weakly doped and higher doping is only applied to those sections of the waveguide that are not touched by the optical field.

GE PHOTODETECTORS

It has been demonstrated in Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer (cap layer) with subsequent annealing, can create a smooth, planar Ge film on a (100) silicon substrate with threading dislocation density on the order of \(10^7 \text{ cm}^{-2} \) [14]. This two-step deposition process has been successfully adapted to an LPCVD system (Applied Materials Epitaxial Reactor). Thus, integrating Ge films onto silicon (Ge/Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors that can be used in an electronic-photonic ADC-chip.

Approximately 2 µm-thick intrinsic Ge films were deposited on p+ (100) Si substrates, and capped with a 0.2 µm N+ polysilicon layer to create a vertical pin-photodiode (Figure 5 inset). The IV characteristics of the photodiodes fabricated with the blanket Ge films are shown in Figure 5. The reverse leakage current at 300K and a –1 volt bias is

Figure 4: (a) Mach-Zehnder modulator with forward biased p''n''-phase modulator sections. (b) Different possible doping profiles for the Si buried waveguides used for the modulators.

Figure 5: IV characteristics of a 100x100 µm diode as a function of temperature. The diode has an ideality factor less than 1.2 at 300K with a perimeter dominated reverse leakage current of ~55 mA/cm² at −1 volt bias. Inset shows a schematic of a diode cross-section.
~55 mA/cm², with the reverse leakage current of the diodes being perimeter dominated for diodes less than 1 mm² in surface area.

At a 1.55 μm wavelength, the Ge film has a responsivity of 0.5 A/W. The frequency response of a 20 μm x 100 μm photodiode was measured by the response of the diode to 1 picosecond pulses of light at a wavelength of 1.04 μm. At a –5 volt bias, the diode is measured to have a 3dB frequency of 1.4 GHz. The photodiodes are required to translate pulse amplitude information into an electrical signal with sufficient linearity to achieve the proposed high effective number of bits (ENOB) for the ADC system. To characterize the linearity, we measured the spur-free dynamic range (SFDR) of the diodes using a test setup designed for cable television (CATV) applications.

To complete the data required to calculate SFDR, the noise floor of the link was measured, roughly integrating over a 2-GHz bandwidth with the microwave spectrum analyzer. This data and the calculated SFDR are shown in Figure 6. The demonstrated 34 dB SFDR of this link would currently allow for 5.6 effective bits if it was the limiting factor in the system’s performance.

In summary, photodiodes with ~40 mA/cm² reverse leakage currents at 300K and ~1 volt bias greater than 0.5 A/W responsivity and a 34 dB SFDR for a 2-GHz noise bandwidth have been fabricated. These diodes also have 3 dB frequencies in the GHz range, and it is believed that improved passivation of the Ge films will further improve the frequency response and the reverse leakage current of these CMOS compatible Ge photodetectors.

CONCLUSIONS

Integration of HIC optical devices on the Si-Technology platform together with electronics may lead to advanced signal processing capabilities in the near future. We discussed three key components of such a system such as filter banks, modulators, and detectors. The presentation will in addition update on progress towards on-chip modelocked lasers, novel sampling techniques, as well as integration of these devices in a CMOS compatible fabrication process which is carried out jointly with MIT Lincoln Laboratory.

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