

Masood Qazi

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EDUCATION

- Ph.D. **Massachusetts Institute of Technology**, Cambridge MA
Electrical Engineering, Expected June 2011
- Thesis Title: *Low-power Embedded Memory Design*
Supervisor: Anantha Chandrakasan
- M. Eng. **Massachusetts Institute of Technology**, Cambridge MA
Electrical Engineering and Computer Science, June 2007
- Thesis Title: *A 4kb Memory Array for MRAM Development*
Supervisor: Anantha Chandrakasan
- B.S. **Massachusetts Institute of Technology**, Cambridge MA
Double major in Physics and Electrical Science and Engineering, June 2006
Undergraduate GPA: 4.9/5.0

PUBLICATIONS

R. Beach, T. Min, C. Horng, Q. Chen, P. Sherman, S. Le, S. Young, K. Yang, H. Yu, X. Lu, W. Kula, T. Zhong, R. Xiao, A. Zhong, G. Liu, J. Kan, J. Yuan, J. Chen, R. Tong, J. Chien, T. Torng, D. Tang, P. Wang, M. Chen, S. Assefa, **M. Qazi**, J. DeBrosse, M. Gaidis, S. Kanakasabapathy, Y. Lu, J. Nowak, E. O'Sullivan, T. Maffitt, J. Z. Sun and W. J. Gallagher, "A statistical study of magnetic tunnel junctions for high-density spin torque transfer-MRAM (STT-MRAM)," IEEE International Electron Devices Meeting, pp. 1-4, December 2008.

Dolecek, L., **M. Qazi**, D. Shah, and A.P. Chandrakasan, "Breaking the Simulation Barrier: SRAM Evaluation Through Norm Minimization," IEEE/ACM International Conference on Computer-Aided Design, pp. 322-329, November 2008.

M. Qazi, M. Tikekar, L. Dolecek, D. Shah, and A.P. Chandrakasan, “Loop Flattening & Spherical Sampling: Highly Efficient Model Reduction Techniques for SRAM Yield Analysis.” To be presented. Design, Automation, and Test in Europe Conference. March 2010.

M. Qazi, K. Stawiasz, L. Chang, A. P. Chandrakasan, “A 512kb 8T SRAM Macro Operating Down to 0.57V with an AC-coupled Sense Amplifier and Embedded Data Retention Voltage Sensor in 45nm SOI CMOS,” To be presented. IEEE International Solid State Circuits Conference, February 2010.

RESEARCH AND ACADEMIC EXPERIENCE

- 1/2007 – present **MIT Microsystems Technology Laboratory**, Cambridge MA
Doctoral Research: Investigating the challenges of low-power embedded memory design. Specifically, circuit solutions and design tools for the increasing process variation of scaled CMOS are being developed. Chip prototypes are designed and tested in multiple memory technologies including SRAM and emerging nonvolatile memories to address challenges of sensing and low-voltage operation.
- 9/2008 – 12/2008 **Digital Integrated Circuits, Department of Electrical Engineering and Computer Science, MIT**, Cambridge MA
Teaching Assistant: Assisted in writing and grading homework and exams for the digital integrated circuits class at MIT. Responsibilities also included meeting several hours per week with students to go over course material and CAD software, discuss homework, and provide guidance on projects. Received student rating of 6.5 out of 7.0.
- 6/2003 – 8/2003 **MIT Laboratory for Electromagnetic and Electronic Systems**, Cambridge MA
Undergraduate Research Assistant: Developed MATLAB programs covering joint probability distributions, two and three state Markov Chains, and the bivariate normal distribution. Were used in lectures for MIT course Probabilistic Systems Analysis.

RELATED INDUSTRY EXPERIENCE

- 7/2008 – 8/2008 **Taiwan Semiconductor Manufacturing Corporation**, Hsinchu Science Park, Taiwan ROC
Engineering Intern: Worked on a technology benchmarking team. Developed 8T SRAM memory macros for simulation across different CMOS technology generations. Also developed new simulation

methodologies for statistical characterization of memory cell stability and peripheral circuit assists.

2/2008 – 6/2008

IBM TJ Watson Research Center, Yorktown Heights NY

Research Intern: Designed and tested a low-power SRAM array in advanced CMOS technology. Developed and implemented novel sensing techniques and circuits adaptive to the statistical fluctuation of device properties. Full suite of industry standard Cadence/Synopsys and IBM internal tools employed for custom design, analysis, layout and verification. Work to be presented at ISSCC 2010.

Summers 2004,
2005, 2006, and
9/2006 – 1/2007

IBM Microelectronics, Essex Junction VT

Engineering Intern: Designed a 4kb MRAM array. Full functionality demonstrated on integrated magnetic hardware. Responsibilities included architecture, transistor-level design, simulation, layout supervision, and hardware test. In addition, created methods to profile write current pulses in MRAM chips. Sole recipient of the “Excellence in VI-A Industrial Practice” award for 2007. Work contributed to IEDM 2008 publication.

AWARDS AND HONORS

- Honor Societies: Phi Beta Kappa, Tau Beta Pi, Pi Sigma Pi
- J. Francis Reintjes Excellence in VI-A Industrial Practice Award (2007) --- Award for best Master’s thesis completed at a company within the EECS VI-A Thesis Program.
- Previous Scholarships: Siebel Scholar 2006, National Merit Finalist, Toyota Community Scholar 2002
- Letters of merit in MIT undergraduate courses: Circuits and Electronics, Signals and Systems, Digital Systems Laboratory, Analog Electronics Laboratory
- Analog Devices Circuit Design Contest 2005 (3rd place)