Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems

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***Abstract*—In electric vehicle (EV) inverter systems, direct-current-link capacitors, which are bulky, heavy, and susceptible to degradation from self heating, can become a critical obstacle to high power density. This paper presents a comprehensive method for the analysis and comparative evaluation of dc-link capacitor applications to minimize the volume, mass, and capacitance. Models of equivalent series resistance that are valid over a range of frequency and operating temperature are derived and experimentally validated. The root-mean-square values and frequency spectra of the capacitor current are analyzed with respect to three modulation strategies and various operating conditions over practical ranges of load power factor and modulation index in EV drive systems. The modeling and analysis also consider the self-heating process and resulting core temperature of the dc-link capacitors, which impacts their lifetimes. Based on an 80-kW permanent-magnet (PM) motor drive system, the application of electrolytic capacitors and film capacitors has been evaluated by both simulation and experimental tests. The inverter power density is improved from 2.99 kW/L to 13.3 kW/L, without sacrificing the system performance in terms of power loss, core temperature, and lifetime.**

***Index Terms*—Direct-current (dc)-link capacitor, electric vehicles (EVs), equivalent series resistance (ESR), parasitic inductance, power density, ripple current stress.**

I. Introduction

RESEARCH on electric vehicles (EVs) has recently intensified due to global warming and other environmental concerns that surround the existing petroleum-based transportation infrastructure [1], [2]. In EVs, the most common power interface between batteries and traction motors is the voltage-source inverter (VSI), as shown in Fig. 1. Current EV inverter research is concerned with aspects of compact design [3]–[5], low cost [6], [7], high reliability [8]–[10], and long lifetime [11]. Several topologies and optimization strategies have been investigated to meet multiple objectives under the stringent operation requirements of EV inverters [12]–[15]. For example, overload conditions of 2–2.5 times rated capacity can last 1–3 min, and power electronic components are expected to tolerate inlet coolant temperatures up to 105 °C [16]. Other design requirements include high efficiency and high power density [17].

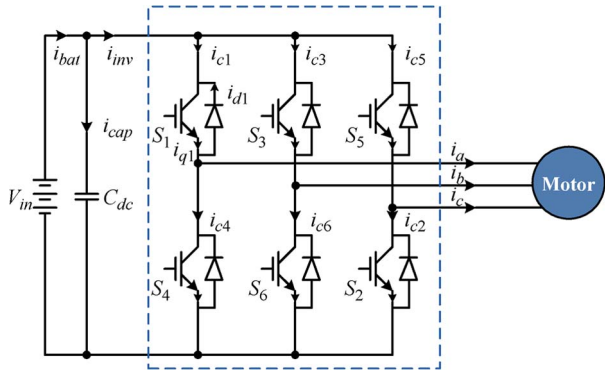

Fig. 1. Schematic of a typical EV drive system, including, from left to right, a battery bank, dc-link capacitors, VSI, and traction motor.

Many efforts have been directed toward improving the power density, which may be quantified as the power density by weight (PDW) and the power density by volume (PDV). For example, the FreedomCAR and Vehicle Technologies (FCVT) program in the U.S. aims at developing energy-efficient and environmentally friendly highway transportation systems [18], [19]. The FCVT program reports that the PDW and the PDV of EV inverters have been increased from 4.08 kW/kg to 10.04 kW/kg and from 2.03 kW/L to 8.82 kW/L, respectively [3]. Further improvement is expected to achieve more than 14.1 kW/L in the PDV of EV inverters according to the FCVT technology roadmap [18]. A corresponding technology roadmap has been defined in China in terms of cost, efficiency, and power density [20]. In an example of high-performance possibilities, the latest inverter that is based on silicon carbide junction gate field-effect transistors shows a potential 51 kW/L PDV while achieving 97.8% efficiency [21]. Table I summarizes the main technical parameters and objectives that correspond to the road technical maps and timelines of EV drive system development programs in the U.S. and China.

In EV inverter systems, direct-current (dc)-link capacitors are essential to provide reactive power, attenuate ripple current, reduce the emission of electromagnetic interference, and suppress voltage spikes caused by leakage inductance and switching operations [24]. DC-link capacitors are bulky, heavy, and expensive [25]. One typical design comprises five electrolytic capacitors, which are connected in parallel with the battery bank to supply an 80-kW motor drive system [26]. Each capacitor is 9.4 cm in diameter and 14.6 cm in height. Because the five dc-link capacitors occupy more than 40% of the volume, the achievable PDV is limited to 2.99 kW/L. Furthermore, the

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TABLE I
SUMMARY OF TECHNICAL ROADMAP TARGETING FOR EV DRIVE SYSTEMS

Subsystem	Parameters	FreedomCar phase I [3]	FreedomCar phase II [3]	Chinese Goals in 2006 [22]	FreedomCar Goals in 2006 [18]	FreedomCar Goals in 2020*[19]	Sic JFET-based Converter [21, 23]
Inverter	PDW (kW/kg)	4.08	10.04	2~5	>12	>14.1	>51
	PDV (kW/L)	2.03	8.82	~	>12	>13.4	>51
	Efficiency @maximum load	80~88%	80~88%	90~92%	92%	94%	97.8%
Motor	Motor types	IM	IM	PM, IM and SRM	PM	PM	PM
	PDW (kW/kg)	0.5~1	0.5~1	0.5~1	>1.2	>1.6	>1,3
	PDV (kW/L)	1.01~	1.01~	1.01~	>3.7	>5.7	>5
	Efficiency	90	90	92~95%	>93%	>94%	>93%
System	Efficiency	72~84%	76~86%	90~92%	92%	94%	>92%
	Cooling mode	Forced air	Liquid	Liquid	Liquid	Liquid or air	Natural air
	Ambient Temp.	-25~50 °C	-25~50 °C	~70 °C	~105 °C	105 °C	120 °C
	Cost($/kW)	-	-	70	<105	<62.7	-
	Total Mileage (km)	-	-	241402 (15 yrs)	241402 (15 yrs)	241402 (15 yrs)	241402 (15 yrs)

* Based on a maximum coolant or air temperature of 105°C

height of dc-link capacitors is higher than most insulated gate bipolar transistor (IGBT) modules and requires a crooked busbar to make the connection. The resulting parasitic inductance may exceed 100 nH, causing voltage spikes, which are a major factor in the failure of power electronic devices. For the aforementioned reasons, an optimum design of dc-link capacitors is critical to achieve the goals shown in Table I. Some basic requirements for choosing and comparing different capacitors for EV inverter applications are listed as follows.

1) DC-link capacitors should handle the ripple current under all VSI operating conditions for EV applications. The battery alternating-current (ac) ripple current should never exceed 10% of the rated battery current to avoid significant degradation on the lifetime of battery.
2) The ripple voltage across the dc bus should be limited to 10% of the rated voltage for all expected load conditions. Low-inductance capacitors are preferred to avoid overvoltage failure of IGBTs.
3) Hot spot temperature should be below 105 °C under maximum ambient temperature for any expected load condition.

Ripple current is one of the main considerations in sizing and selecting dc-link capacitors. Approaches have been proposed to reduce the capacitor current ripple and minimize the capacitor size without violating other constraints by coordinating the modulation strategies between the active rectifier and the pulsewidth modulation (PWM) inverter stages [27], [28]. The coordinating modulation method has been shown to cancel most of the dc-link capacitor ripple current in hybrid EV dc–dc converters and inverter system applications [29]. However, the implementation of coordinating control strategies is infeasible for the EV drive system shown in Fig. 1, where the dc-link capacitors are directly connected in parallel with the battery bank without any power stages in between [30], [31]. For the EV drive system shown in Fig. 1, research mainly focuses on the ripple current analysis and current harmonics calculation [31]–[34]. Most analysis has been based on an ideal capacitor model, which cannot accurately predict power loss and capacitor lifetime. The ideal capacitor model does not properly account for the effects of the variation of load power factor and modulation index in a practical EV system. Models that include equivalent series resistance (ESR) and show the effects of temperature and frequency are investigated and applied to electrolytic capacitors in [35]–[37]. Their modeling approach concentrates on only the characteristic analysis for electrolytic capacitors.

In summary, a systematic comprehensive evaluation of the benefits and drawbacks of film capacitors for EV inverter applications has not been reported. The basic requirements, system constraints, and performance metrics have not been fully and systematically addressed. In EV inverter systems, the capacitor ripple current consists of various frequency components that correspond to different PWM strategies. Therefore, the frequency spectrum analysis of the capacitor current and an accurate model of ESR, considering the temperature and frequency response, are important to properly account for the self-heating process of dc-link capacitors. Furthermore, the electrothermal coupling dynamics must be evaluated to estimate the true core temperature of the dc-link capacitors, which is critical to predict the capacitor lifetime.

This paper presents a comprehensive analysis and evaluation of dc-link capacitors in EV inverter systems to improve the power density. The analysis starts with ESR models of both electrolytic and film capacitors. The mathematical models derived are verified by experiments. The voltage and current stresses are analyzed with respect to the following three common modulation strategies: 1) sinusoidal pulsewidth modulation (SPWM); 2) space vector modulation (SVM); and 3) third-harmonic injection (THI). The frequency spectrum of the capacitor ripple current is also investigated, which corresponds to these modulation strategies over the practical ranges of load power factor and modulation index. Based on the aforementioned analysis, the self-heating process and the resulting core temperature are modeled and analyzed. Two design schemes using electrolytic and film capacitors are compared through simulation and experiments in terms of power loss, core temperature, lifetime, and battery current harmonics.

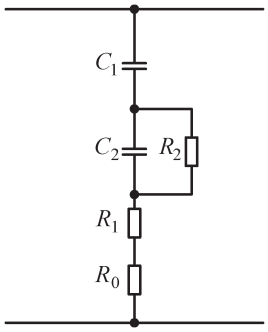

Fig. 2. ESR model of an electrolytic capacitor.

The proposed design has been tested in an 80-kW permanent-magnet (PM) motor drive system.

II. Capacitor Characteristics

This section investigates the ESR models of electrolytic and film capacitors and shows the characteristics of frequency and self heating.

A. Electrolytic Capacitor ESR

Electrolytic capacitors are commonly used as dc-link capacitors due to their large capacitance per unit volume. The ESR model of an electrolytic capacitor is illustrated in Fig. 2 [38], where the resistance R_0 accounts for the sum of resistances of foil, tabs, and terminals R_1 symbolizes the electrolyte resistance, C_1 represents the terminal capacitance, and the parallel combination of R_2 and C_2 represent the dielectric dynamics. The ESR of the capacitor in terms of the frequency responses is accordingly derived as

$$\mathrm{ESR}_e = R_1 + R_0 + \frac{R_2}{1 + (2\pi f R_2 C_2)^2}. \tag{1}$$

For electrolytic capacitors, a rise in temperature causes a decrease in ESR, because the resistance R_1 is reduced by the increased conductivity of electrolyte. The effect of temperature on R_1 is described by [35], [39]

$$R_1 = R_{1b} e^{\frac{T_{\mathrm{base}} - T}{F}} \tag{2}$$

where R_{1b} represents the value of R_1 at a base temperature of T_{base} (27 °C), T is the capacitor core temperature (°C), and F is a temperature sensitivity factor [35].

B. Film Capacitor ESR

A resistance–inductance–capacitance (*RLC*) series equivalent circuit that includes the equivalent resistance R_c, inductance L_c, and capacitance C_c is used to model film capacitors. When the operating frequency is higher than 1 kHz, the ESR value can be modeled as a function of frequency based on [40] as

$$\mathrm{ESR}(f) = (R_s - A_s) + K(f) \cdot A_s \tag{3}$$

where R_s is the base resistance, f represents the frequency, and A_s is a parameter given by the manufacturer, related to the capacitor size. $K(f)$ is the predefined function that shows the effect of frequency, which is usually given by plots in manufacturer datasheets. In this analysis, $K(f)$ is mathematically expressed as a cubic polynomial function, as shown in

$$K(f) = k_3 \cdot f^3 + k_2 \cdot f^2 + k_1 \cdot f + k_0 \tag{4}$$

in which the coefficients k_{0-3} can be established by using least square curve fitting.

In contrast with the electrolytic capacitor, the ESR value of film capacitors increases with frequency. Its temperature sensitivity is less than that of electrolytic capacitors [40], because the ESR of film capacitors results mainly from the tabs and contact resistances but not from the electrolyte [41].

C. Ripple Current Multiplier

Because the ESR values of electrolytic and film capacitors show frequency-dependent characteristics, a ripple current multiplier M_f is defined in (5) to characterize the ripple current that a capacitor can absorb at a given frequency

$$M_f = \frac{I_f}{I_{100}} = \sqrt{\frac{\mathrm{ESR}_{100}}{\mathrm{ESR}_f}} \tag{5}$$

where I_{100} and ESR_{100} are defined as the rated ripple current and the ESR value at 100 Hz, which are usually given by manufacturers. I_f and ESR_f represent the ripple current and ESR at a specific frequency. Electrolytic capacitors are characterized as absorbing more high-frequency ripple current than the low-frequency component. Conversely, film capacitors usually handle less high-frequency ripple current, because the ripple current multiplier drops with increasing ESR_f.

III. Capacitor Ripple Current and Voltage

The battery current i_{bat} is the sum of the capacitor current i_{cap} and dc-link current i_{inv}, as shown in Fig. 1. These current waveforms are greatly affected by the load power factor $\cos\phi$, which determines the current that flows into IGBT devices or free-wheeling diodes of the VSI. As a result, practical EV operating conditions, which are expressed in terms of load power factor and modulation index, must be considered in evaluating the capacitor ripple current and voltage.

A. Capacitor Ripple Current Analysis

Based on the synthesis of inverter input current modulation by SVM [34], the root-mean-square (RMS) capacitor ripple current I_{cap} can be expressed by

$$I_{\mathrm{cap}} = I_N \sqrt{\frac{M}{32\pi}\left[4\sqrt{3}(4\cos 2\phi + 6) - 9\pi \cdot M \cdot (\cos 2\phi + 1)\right]} \tag{6}$$

where M is the modulation index, I_N is the output phase current amplitude, and ϕ is the phase delay of the inverter output current with respect to the voltage fundamental.

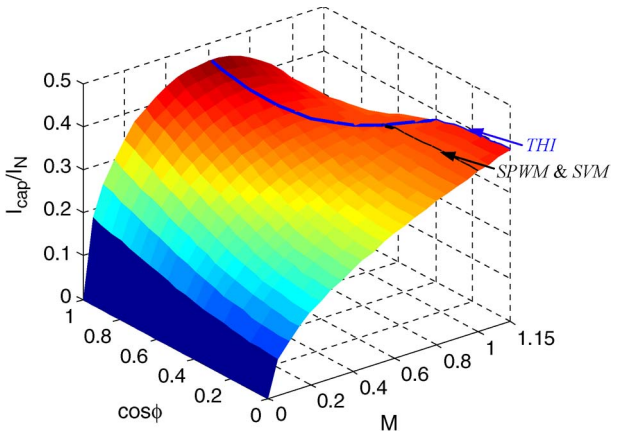

Fig. 3. Ratio of $I_{\rm cap}/I_l$ is a function of modulation index M and load power factor cosϕ.

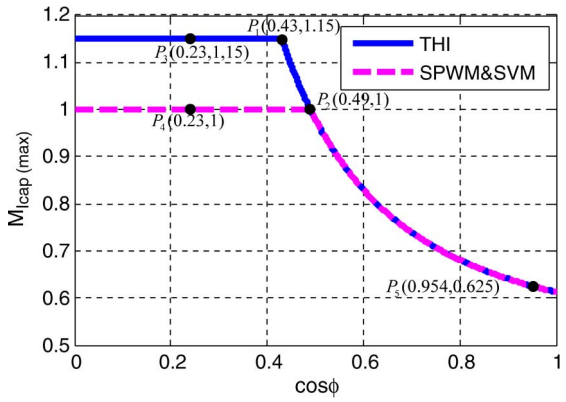

Fig. 4. Distribution of $M_{I_{\rm cap(max)}}$ that corresponds to power factor cosϕ.

Fig. 3 illustrates the dependence of $I_{\rm cap}/I_N$ on the modulation index M and load power factor cosϕ. The modulation index that corresponds to the maximum RMS value of the capacitor ripple current is denoted as $M_{I_{\rm cap(max)}}$, and it somewhat depends on the modulation strategy. SPWM and SVM share the same expression (7) for $M_{I_{\rm cap(max)}}$, and the expression for THI $M_{I_{\rm cap(max)}}$ is given by

$$M_{I_{\rm cap(max)}} = \min\left[\frac{4\sqrt{3}(2\cos 2\phi+3)}{9\pi(\cos 2\phi+1)}, 1\right] \tag{7}$$

$$M_{I_{\rm cap(max)}} = \min\left[\frac{4\sqrt{3}(2\cos 2\phi+3)}{9\pi(\cos 2\phi+1)}, 1.15\right]. \tag{8}$$

In Fig. 3, the blue line illustrates the maximum RMS value of the capacitor ripple current that corresponds to the THI modulation strategy, under which the modulation index can range from 0 to 1.15. The black line indicates the upper bound $(M=1)$ of $M_{I_{\rm cap(max)}}$ when modulation is by SPWM or SVM. To address typical operation conditions, the distribution of $M_{I_{\rm cap(max)}}$ in relation to the load power factor is plotted in a 2-D space, which is shown in Fig. 4. When cosϕ is lower than a certain value of the power factor $\phi_{\rm th}$, the ratio increases with M and reaches the maximum at the upper bound of the modulation range. When cosϕ is larger than $\phi_{\rm th}$, $M_{I_{\rm cap(max)}}$ is located in the middle of the modulation range, no longer at the upper bound. It is noticeable that THI shows a different $\phi_{\rm th}$ value from SPWM and SVM, because the modulation index is up to 1.15. In the case of THI, the threshold value of the load power factor $\phi_{\rm th}$ is 0.43, whereas the corresponding threshold value of the load power factor $\phi_{\rm th}$ is 0.49 in the cases of SPWM and SVM. Based on the aforementioned analysis, five typical operating conditions, which are denoted by P_1–P_5, are defined in Table II.

TABLE II
PREDEFINED TYPICAL OPERATING CONDITIONS P_1–P_5

Operating condition	Modulation index M	Load power factor $cos\phi$
P_1	1.15	0.43
P_2	1	0.49
P_3	1.15	0.23
P_4	1	0.23
P_5	0.625	0.954

TABLE III
DC-LINK CAPACITOR VOLTAGE RIPPLE EXPRESSIONS FOR THREE MODULATION METHODS: SPWM, SVM, AND THI

Modulation Strategies	Voltage ripple of dc-link capacitor (p.u.) [43]
SPWM	$\frac{M}{16}\left[\left(6-\frac{96\sqrt{3}}{5\pi}M+\frac{9}{2}M^2\right)\cos^2\phi+\frac{8\sqrt{3}}{5\pi}M\right]^{0.5}$
SVM	$\frac{M}{16}\left[\left(6-\frac{96\sqrt{3}}{5\pi}M+\frac{108\pi-81\sqrt{3}}{16\pi}M^2\right)\cos^2\phi+\frac{8\sqrt{3}}{5\pi}M\right]$
THI	$\frac{M}{16}\left[\left(6-\frac{96\sqrt{3}}{5\pi}M+\frac{63}{16}M^2\right)\cos^2\phi+\frac{8\sqrt{3}}{5\pi}M\right]^{0.5}$

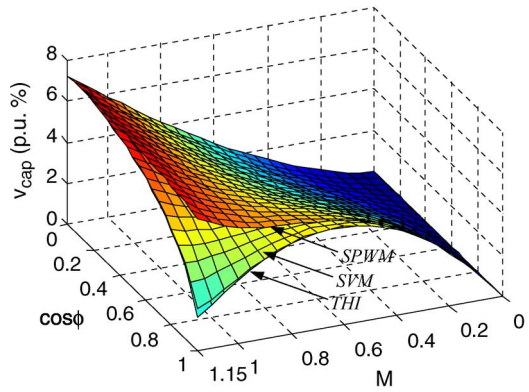

Fig. 5. Characteristics of the voltage ripple across the dc link as a function of modulation index M and load power factor cosϕ for the three modulation strategies SPWM, SVM, and THI.

The maximum current stress on a dc-link capacitor can be estimated by applying (6) over a wide variety of operating conditions for a specific motor, modulation method, and battery. Here, we consider an 80-kW PM motor supplied by a nominal 312-V battery pack. The capacitor maximum current stress is calculated as 105 A, which is used as the base value for capacitor ripple current evaluation.

B. Capacitor Voltage Ripple Analysis

Table III summarizes the expressions for the dc-link capacitor RMS ripple voltage (in per unit) for different modulation

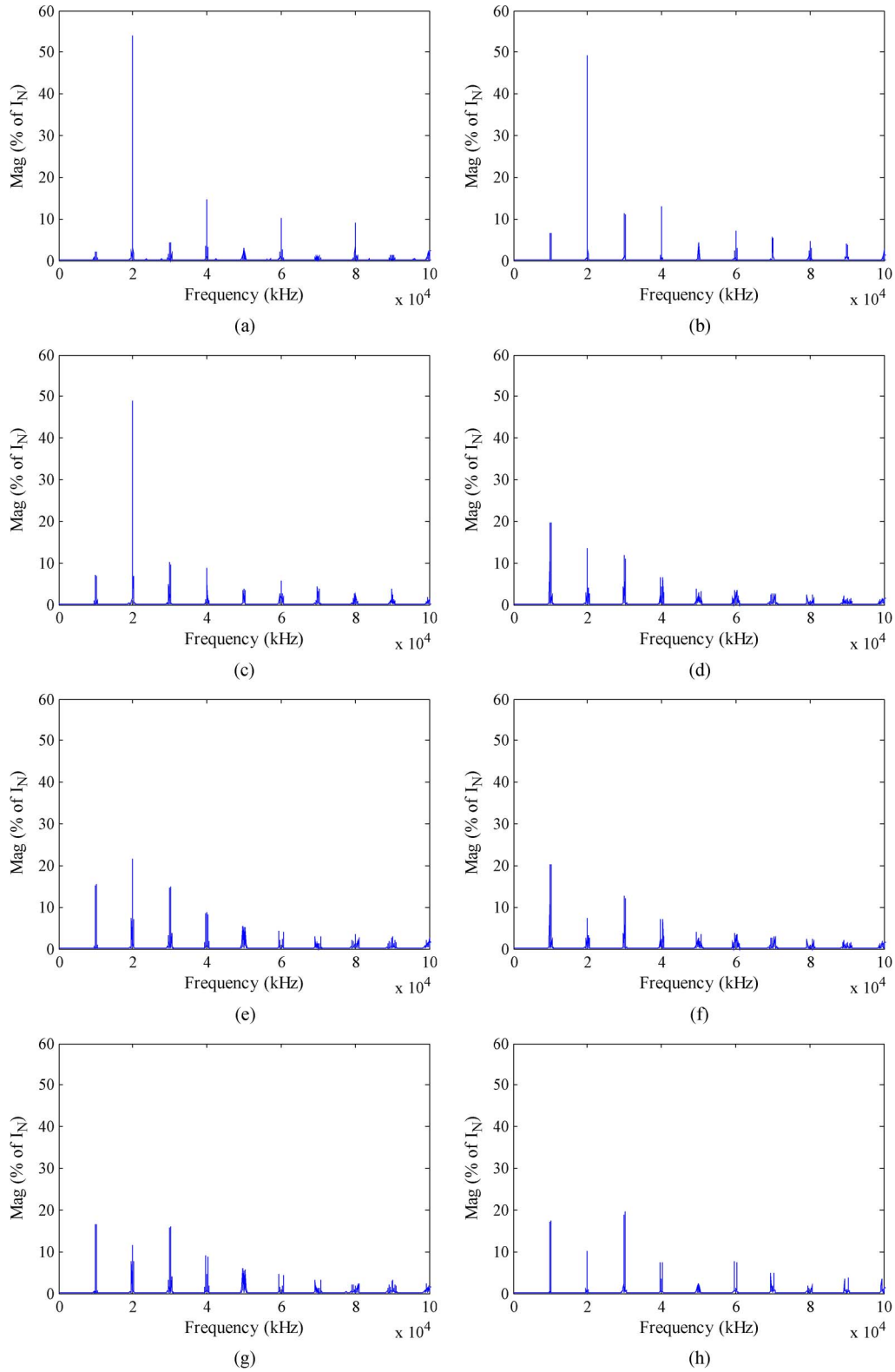

Fig. 6. Frequency spectra of the capacitor current based on modulation strategy and predefined operating condition: Load power factor and modulation index. (a) SVM: P_5 ($M = 0.625, \cos\phi = 0.954$). (b) SPWM: P_5 ($M = 0.625, \cos\phi = 0.954$). (c) THI: P_5 ($M = 0.625, \cos\phi = 0.954$). (d) THI: P_1 ($M = 1.15, \cos\phi = 0.43$). (e) SVM: P_2 ($M = 1, \cos\phi = 0.49$). (f) THI: P_3 ($M = 1.15, \cos\phi = 0.23$). (g) SVM: P_4 ($M = 1, \cos\phi = 0.23$). (h) SPWM: P_4 ($M = 1, \cos\phi = 0.23$).

strategies [33]. The base value is given by

$$V_{b\_\text{volrip}} = \frac{I_N}{C_d f_1} \tag{9}$$

where C_d is the dc-link capacitance, and f_1 is the inverter switching frequency.

Fig. 5 illustrates the characteristics of the dc-link ripple voltage (in per unit) with regard to the modulation index M and

TABLE IV
COMPARISON OF SPECTRAL DISTRIBUTION FOR THE THREE MODULATION STRATEGIES AND FIVE OPERATING CONDITIONS

Operating condition	Modulation	Major three components sorted by magnitude (% of I_N)					
		frequency	magnitude	frequency	magnitude	frequency	magnitude
P_4	*SPWM*	$3f_1$ sbs	19.2	f_1 sbs	17.2	$2f_1$	10.2
P_4	*SVM*	f_1 sbs	16.6	$3f_1$ sbs	15.9	$2f_1$	11.7
P_1	*THI*	f_1 sbs	20.2	$3f_1$ sbs	12.3	$2f_1$	7.3
P_1	*THI*	f_1 sbs	19.7	$2f_1$	13.6	$3f_1$ sbs	11.4
P_2	*SPWM*	$2f_1$	21.7	f_1 sbs	15.4	$3f_1$ sbs	14.7
P_2	*SVM*	$2f_1$	21.7	$3f_1$ sbs	17.4	f_1 sbs	17
P_5	*SPWM*	$2f_1$	49.2	$4f_1$	13.1	$3f_1$ sbs	11.1
P_5	*SVM*	$2f_1$	52	$4f_1$	14	$6f_1$	9.9
P_5	*THI*	$2f_1$	48.8	$3f_1$ sbs	9.9	$4f_1$	8.7

the load power factor cosϕ for the three modulation strategies. When the load power factor is zero, the ripple voltage levels are the same for all three modulation strategies, i.e., SPWM, SVM, and THI. When the load power factor is nonzero, SPWM shows the largest voltage ripple, THI gives the lowest voltage ripple, and SVM demonstrates relatively low-voltage ripple.

C. Frequency Spectrum of the Capacitor Ripple Current

The frequency spectra of the capacitor current $i_{\rm cap}$ for the predefined operating conditions $P_{\rm i}$ and modulation methods, including SPWM, SVM, and THI, are illustrated in Fig. 6 and are summarized in Table IV to demonstrate the interaction of modulation strategy and operating condition. The current spectra contain significant switching frequency f_1 multiples and their sidebands (SBs). At low cosϕ, switching frequency SBs are usually the biggest harmonic components, and the current spectrum is more or less evenly distributed among f_1 SBs, $3f_1$ SBs, and $2f_1$. At high cosϕ (larger than 0.49 for SVM), $2f_1$ is the dominant component, and its amplitude increases with cosϕ. For example, the largest harmonic component is nearly 21% of the output current amplitude at cos$\phi = 0.49$, whereas the corresponding harmonic component reaches as high as 48.8% at cos$\phi = 0.954$. Moreover, the impact of modulation strategy on the current spectrum distribution is obvious at high cosϕ, and the major harmonics for SVM will extend to higher frequency such as $6f_1$. We can see that the ESR characteristic of the dc-link capacitor is highly affected by frequency for both electrolytic and film capacitors. The fast Fourier transform results shown in Fig. 6 and Table IV provide information that is essential to the proper sizing of dc-link capacitors.

IV. PERFORMANCE METRICS

Based on the aforementioned analysis, the following four metrics are proposed to evaluate the performance of dc-link capacitors:

1) power loss;
2) core temperature;
3) capacitor life;
4) battery ripple current.

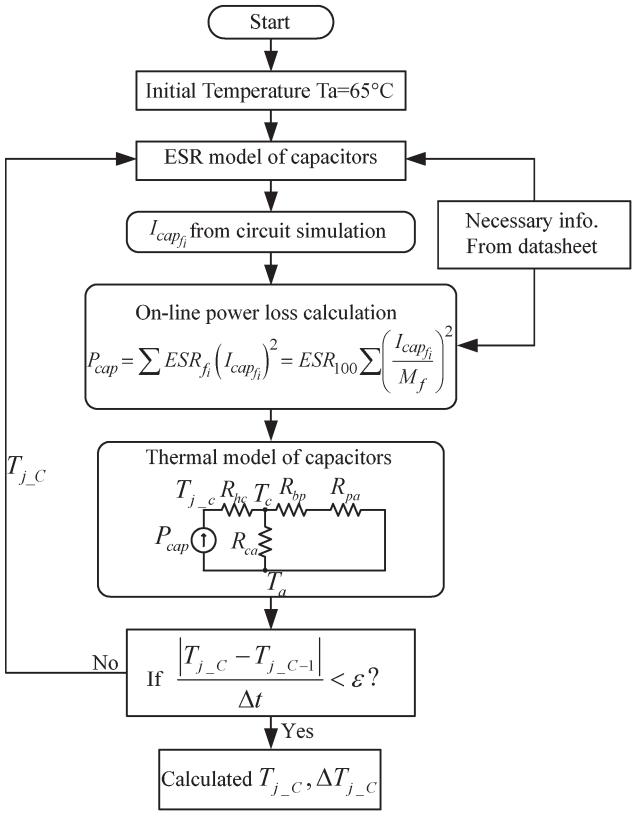

Fig. 7. Flowchart for the iterative solving process of the core temperature and ESR.

A. Power Loss and Core Temperature

The power loss of dc-link capacitors is the sum of the power dissipation of the ESR from individual frequency current components that can be calculated using the ripple current multiplier M_f. The expression is shown in

$$P_{\rm cap} = \sum {\rm ESR}_{f_i}\left(I_{{\rm cap}_{f_i}}\right)^2 = {\rm ESR}_{100}\sum\left(\frac{I_{{\rm cap}_{f_i}}}{M_f}\right)^2. \quad (10)$$

where ${\rm ESR}_{f_i}$ represents the ESR value that corresponds to the specific frequency f_i, and $I_{{\rm cap}_{f_i}}$ is the RMS current absorbed by the capacitor at a certain frequency f_i.

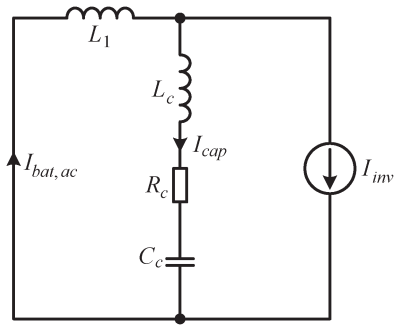

Fig. 8. Equivalent ac circuit of the EV inverter for the battery ripple current analysis.

The self-heating process of dc-link capacitors can numerically be evaluated using the coupled electrothermal method. Fig. 7 depicts the iterative solution process. The computation starts with a given ambient temperature T_a. The capacitor core temperature T_{j_C} is initially calculated by using the capacitor power loss and the equivalent thermal model [40], [42]. Thermal resistances are denoted by R_{hc} from the hot spot to the can, R_{ca} from the can to the ambient, R_{bp} from the can base to the mounting plate, and R_{ha} from the mounting plate to the ambient air. The equivalent thermal resistance from the core of the capacitor to the ambient is given by

$$R_{\text{eq\_cap}} = \left[R_{hc} + \frac{R_{ca} \cdot (R_{bp} + R_{pa})}{R_{ca} + R_{bp} + R_{pa}} \right]. \tag{11}$$

The values of the ESR and ripple current are repeatedly updated using the previous value of T_c for each update. The iterative corrections are repeated until the process converges to within a given tolerance. The core temperature T_{j_C} and the temperature rise ΔT_{j_C} are used for predicting the capacitor lifetime.

B. Capacitor Lifetime

The capacitor lifetime is influenced by the capacitor core temperature and the ripple current and is given in [17] for both kinds of capacitors by

$$L_e = L_b \cdot 2^{\frac{T_{j\_C} - T_a}{10}} \cdot K^{\left[1 - \left(\frac{I}{I_0}\right)^2\right] \cdot \frac{\Delta T_{j\_C}}{10}} \tag{12}$$

where L_b is the capacitor lifetime under its maximum temperature and is commonly given by manufacturer datasheets. I_0 denotes the allowable maximum ripple current at a given frequency, which are also given in datasheets, and I denotes the actual ripple current value. K is a constant, which is typically assigned a value of 2 [17].

C. Battery Ripple Current Analysis

Studies show that the ripple current affects the battery lifetime due to the internal temperature rise [43]. Therefore, the battery ripple current should be maintained under a certain limit to avoid the harmful effect. The dc-link capacitor is represented by an equivalent circuit, including R_c, L_c, and C_c, as shown in Fig. 8. The switching frequency is 20 kHz, and the ESR of the battery pack and interconnects can be neglected, because the impedance of interconnects is dominated by the inductance component, shown as L_1 in Fig. 8. It includes the inductance introduced by the battery pack and interconnects between the battery pack and the inverter. The battery ripple current can be obtained as given in (13) according to the equivalent circuit shown in Fig. 8

$$I_{\text{bat,ac}}(s) = I_{\text{inv}}(s) \times \frac{L_c C_c s^2 + R_c C_c s + 1}{(L_c + \alpha L_{1b}) C_c s^2 + R_c C_c s + 1} \tag{13}$$

$$\alpha = L_1 / L_{1b}. \tag{14}$$

The base value of the inductance L_{1b} is assigned to 10 μH, considering the practical component layout and the parameters of interconnects. The RMS battery ripple current (in percentage) can be defined by the division of the ac RMS value $I_{\text{bat,ac}}$ over the dc RMS current $I_{\text{bat,dc}}$, as shown in

$$\Delta I_{\text{bat}} = \frac{\sum I_{\text{bat,ac}(f_i)}}{I_{\text{bat,dc}}} \times 100\%. \tag{15}$$

TABLE V
MAIN PARAMETERS FOR TWO DESIGN SCHEMES

Parameters	Scheme I	Scheme II
Quantity	5	2
Manufacturer Part	ALS332QP500	FFVE6K0227K
Total Capacitance (μF)	16500	440
Volume (L×W×H, cm)	38×7.7×15	16.8×8.2×8
Ripple current limit (A)	132	200
Cost ($)*	566	176

*Source: http://eu.mouser.com, Date: Feb. 20, 2012

V. EVALUATION RESULT AND DISCUSSION

This section includes the validation of the derived capacitor ESR models by experimental tests and the analysis of the dc-link capacitor current. Then, two configurations of dc-link capacitors are comparatively investigated through simulation and experiment for an 80-kW PM motor drive system in terms of the previously defined performance metrics.

The parameters of two dc-link capacitor designs, schemes 1 and 2, are listed in Table V. Scheme 1 uses five 3300 μF electrolytic capacitors (ALS332QP500), and scheme 2 includes two 220 μF film capacitors (AVX FFVE6K0227K). The capacitor specifications are given in Table XIII in the Appendix. Both schemes meet the base requirements shown in Section I and are comparable, considering product availability, effect of ripple frequency, and temperature.

A. Validation of the Capacitors Model

The ESR values using the derived model are plotted together with the experimental results, as shown in Fig. 9. The ESR values are measured using an HP4263B inductance–capacitance–resistance (LCR) meter. The mathematical model shown in (1) matches the experiment evaluation with regard to the frequency effect. Table VI summarizes the model parameters for the electrolytic capacitor.

The modeling process of the film capacitor is described in Section II-B, which includes the polynomial expression of the

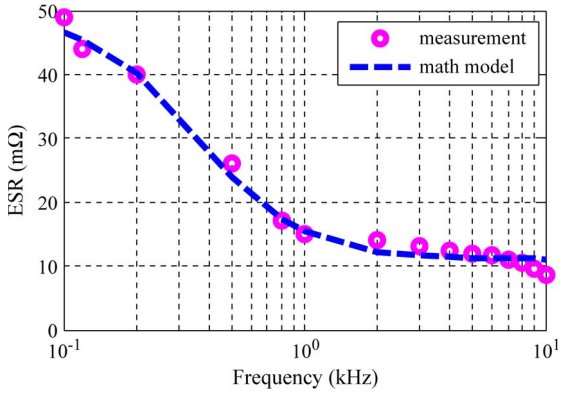

Fig. 9. Comparison of the measured and modeled ESR for the electrolytic capacitor ALS332QP500 at 300 °K.

TABLE VI
MODEL PARAMETERS OF THE ELECTROLYTIC CAPACITOR ALS332QP500

Parameters	Value
Resistance of foil, tabs, and terminals R_0 (mΩ)	5.03
Resistance of electrolyte R_{lb} @ 300°K (mΩ)	6
Temperature sensitivity factor F ($^oK^{-1}$)	21
Dielectric loss resistance R_2 (mΩ)	38.35
Terminal capacitance C_1 (μF)	3300
Dielectric loss capacitance C_2 (μF)	11.6

TABLE VII
MODEL PARAMETERS OF THE FILM CAPACITOR AVX FFVE6K0227K

Parameters	Value
Equivalent series inductance L_c (nH)	40
Equivalent series capacitance C_c (μF)	210
Base resistance R_s (mΩ)	1
Parameter defined by height A_s (mΩ)	0.24
Coefficient of K expression f_3	0.0000003173
Coefficient of K expression f_2	-0.000124
Coefficient of K expression f_1	0.02369
Coefficient of K expression f_0	1.014

frequency-dependent parameter $K(f)$ and the parameter extraction through the comparison with the measured impedance. Fig. 10 shows that the mathematical model matches the experimentally measured frequency response for the 500-V/220-μF film capacitor AVX FFVE6K0227K. Table VII summarizes the equivalent circuit parameters of film capacitors.

The ESR characteristics of the two schemes are compared in Fig. 11. This figure shows that the ESR of scheme 2 is always lower than the ESR of scheme 1 through the frequency span. Furthermore, the ESR of scheme 1 remarkably decreases when the temperature increases from 27 °C to 70 °C.

The capacitor ripple current multiplier M_f was defined in (5) and used to evaluate the capacitor power loss by using (10). Based on the verified mathematical models, the estimated M_f values are summarized in Table VIII, which corresponds to both design schemes.

B. Validation of Ripple Current Analysis

The RMS value of the capacitor ripple current is evaluated by PSpice simulation. The load is a 0.2-Ω resistor that is connected

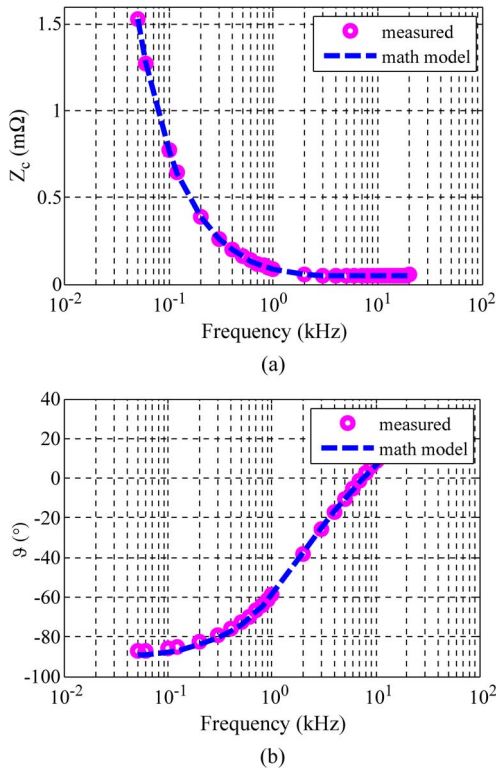

Fig. 10. Comparison of the measured and modeled impedance for the film capacitor AVX FFVE6K0227K at 300 °K. (a) Amplitude characteristic. (b) Phase characteristic.

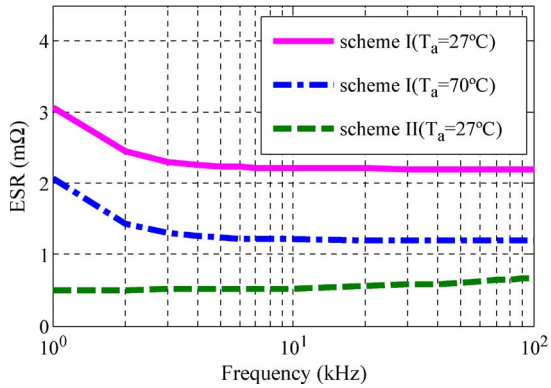

Fig. 11. ESR comparison of the two design schemes for dc-link capacitors with respect to the operating frequency and temperature.

with a variable inductor, which can be used to effect different load power factors. The inverter is modulated by the SVM algorithm, and the switching frequency is 20 kHz. One test case, which corresponds to the constant power operation mode of motors, maintains the constant output current and the constant input voltage. The test condition is designed such that I_N is constant at 84 A and $V_{in} = 312$ V with adjusted modulation indices M. The simulated capacitor current RMS value is compared with the value that was estimated from the mathematical model in (6). Table IX presents the results, which include the simulated capacitor current RMS value $(I_{\rm cap})$, the estimated capacitor RMS current $(I_{\rm cap\_est})$, and the estimation error $(\varepsilon_{I_{\rm cap}})$ under different operating conditions. The root-mean-square deviation (RMSD) is used to evaluate the differences between the mathematical modeling results and the simulation

TABLE VIII
RIPPLE CURRENT MULTIPLIER OF TWO DESIGN SCHEMES FOR DC-LINK CAPACITORS

Frequency (kHz)	M_f for Scheme I	M_f for Scheme II
0.1	1	1
0.2	1.08	1
0.5	1.39	1
1	1.74	1
2	1.95	0.99
5	2.04	0.98
10	2.05	0.97
20	2.05	0.95

TABLE IX
CAPACITOR CURRENT COMPARISON BETWEEN THE SIMULATION AND MODEL ESTIMATION FOR THE CONSTANT OUTPUT CURRENT (84 A) AND INPUT VOLTAGE (312 V)

L (mH)	$cos\phi$	M	I_{cap} (A)	I_{cap_est} (A)	$\varepsilon_{I_{cap}}$ (A)
4	0.16	0.729	27.74	26.97	0.77
2.7	0.23	0.497	23.34	23.11	0.23
1	0.54	0.211	19.72	19.78	-0.06
0.5	0.79	0.145	20.97	20.97	0
0.2	0.95	0.119	22.10	22.04	0.06

TABLE X
CAPACITOR CURRENT COMPARISON BETWEEN THE SIMULATION AND MODEL ESTIMATION FOR THE CONSTANT OUTPUT CURRENT (84 A) AND MODULATION INDEX (0.84)

L (mH)	$cos\phi$	V_{in} (V)	I_{cap} (A)	I_{cap_est} (A)	$\varepsilon_{I_{cap}}$ (A)
4	0.16	261.7	26.79	27.44	-0.65
2.7	0.23	184.8	29.52	28.99	0.53
1	0.54	77.5	31.54	30.83	0.71
0.5	0.79	53.1	33.92	33.32	0.60
0.2	0.95	43.4	35.76	35.22	0.54

results. This result indicates that the RMSD value is 0.36 A, which is small relative to the average capacitor current RMS value of 22.77 A.

The second test case keeps the output current and modulation index constant, where $I_N = 84$ A, and $M = 0.84$. The input voltage is tuned according to the variation of the load power factor. Table X presents the comparison between the simulation results and the model estimation. The RMSD result is 0.61 A, and the average capacitor ripple current RMS value is 31.51 A. The simulation verified the proposed mathematical models and indicated a 1.85% relative modeling error based on the two cases. Furthermore, it exhibits the same trends as in the analysis that was derived in Section II-A and illustrated in Fig. 3.

C. Evaluation of Performance Metrics

The power loss and core temperature are calculated and illustrated in Fig. 12. The main parameters of the two design schemes are defined in Table V. As shown in Fig. 12(a), the capacitor power loss of scheme 2 is significantly lower than scheme 1 due to the reduction of the ESR value. It shows that the capacitor power loss increases with the load power factor and decreases with the ambient temperature T_a in scheme 1. The power loss is nearly constant when T_a varies from 45 °C to 85 °C in scheme 2 due to the insensitive temperature factor of film capacitors. The estimated core temperature of both schemes is illustrated in Fig. 12(b). Scheme 2 shows a lightly higher core temperature, considering the volume difference of dc-link capacitors. The thermal resistance is calculated to be 1.02 K/W for both electrolyte and film capacitors, considering the outer diameters and air flow rate.

The impact of modulation strategy on the capacitor power loss is illustrated in Fig. 13, where the load power factor is constant $(\cos\phi = 0.23)$. Among the three modulation strategies, THI modulation shows the highest power loss due to the frequency spectrum distribution of the capacitor current, which is about 10% higher than that of SVM. SVM shows moderate impact on the power loss of dc-link capacitors, which is roughly 3% higher than SPWM. As shown in Fig. 13(a), the power loss decreases with the increased temperature, which is the characteristic of electrolyte capacitors. For scheme 2, the power loss of dc-link capacitors is lower, as shown in Fig. 13(b), and the temperature variation shows an insignificant impact on the power loss, which is the characteristic of film capacitors.

The lifetime of the two design schemes can be predicted using the mathematical models of the capacitor ESR and ripple current. The lifetime estimation is based on (12), where the key parameters are derived from the product datasheet and shown in the Appendix. Apparently, the temperature and its variation significantly affect the lifetime of dc-link capacitors, as shown in Fig. 14. Moreover, the life expectancy of the film capacitor is about 180 kh and ten times longer than the electrolytic capacitor when the operating ambient temperature is constant at 65 °C.

Twenty-six valve-regulated lead–acid (VRLA) batteries are series connected to form the battery pack, of which the dc bus voltage is rated as 312 V. The battery model is 6-DM-150 VRLA, which is particularly designed for EV applications and manufactured by FENGFAN Company Ltd. The product specification is shown in Table XII. The battery internal resistance is a nonlinear function of the state of charge. The measured internal resistance of the battery packs ranges from 46 mΩ to 182 mΩ.

Battery current harmonics are analyzed for the two design schemes. An upper bound on the ac ripple current is defined as 10% of the rated battery current to avoid degradation of battery life. The main parameters of the two schemes are defined in Table V. The RMS battery ripple current (in percentage) is calculated using the expression in (15) and the equivalent circuit shown in Fig. 8. Fig. 15 shows the analysis results of the battery ripple current, where the symbol α is predefined in (14) and determined by the equivalent circuit shown in Fig. 8. The battery ripple current in scheme 2 is higher than the ripple current in scheme 1 due to the vast reduction of capacitance. The capacitance in scheme 2 is 440 μF, which is about 2.6% of the capacitance in scheme 1. Therefore, to meet the 10% upper bound, α must be larger than 0.6 in scheme 2, considering various combinations of modulation index and load power factor. In practical EV systems, the cable interconnect provides enough impedance to guarantee α to be larger than 0.6, because the inverter and the battery bank are located at some distance.

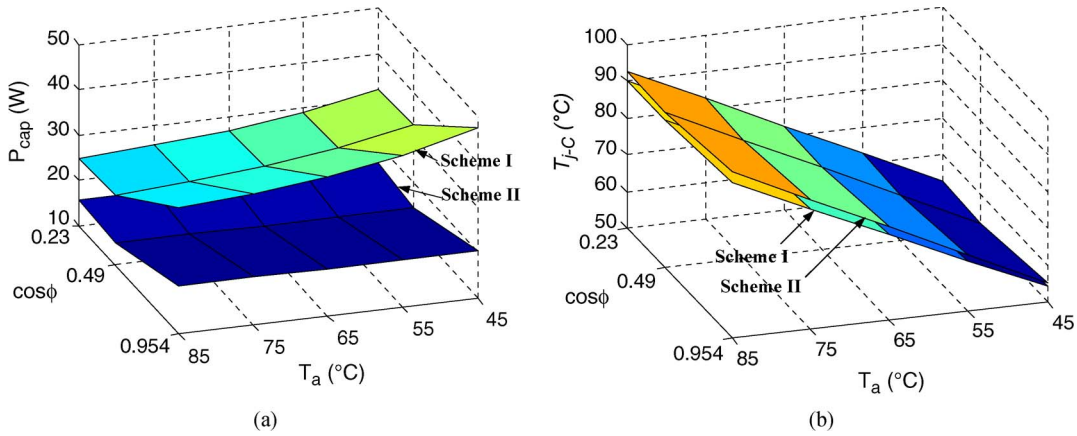

Fig. 12. Performance comparison between two schemes. (a) Power loss. (b) Core temperature.

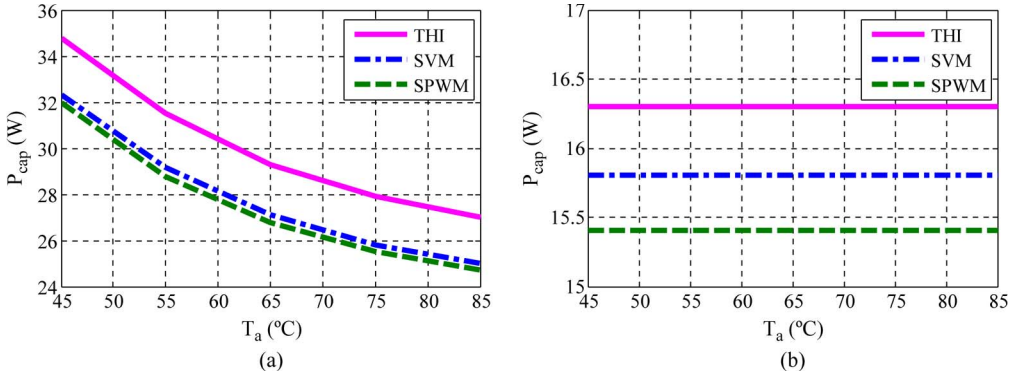

Fig. 13. Power loss of dc-link capacitors among three switching modulation strategies. (a) Scheme 1: Five 3300-μF electrolytic capacitors. (b) Scheme 2: Two 220-μF film capacitors.

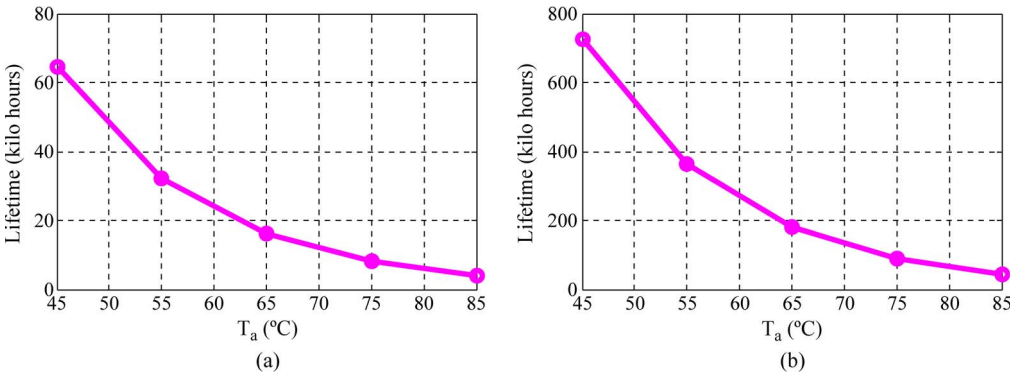

Fig. 14. Life expectancy of the two design schemes for dc-link capacitors, with the ambient temperature spanning from 45 °C to 85 °C. (a) Scheme 1: Five 3300-μF electrolytic capacitors. (b) Scheme 2: Two 220-μF film capacitors.

D. Experiment With an 80-kW PM Motor

The EV drive system is now tested with an 80-kW PM ac motor, the experimental parameters of which being listed in the tables in Appendix. Fig. 16 demonstrates two photos that were taken from the testbed, which consists of the driving motor, the inverter, the digital controller, meters, and the water-cooling mechanism. Fig. 16(b) illustrates the inside inverter assembly, which shows the two film capacitors. In the test, the traction motor is hooked to a dc motor, and the output of dc motor is connected to a power resistor, which dissipates the regenerated power. The control algorithms are implemented by a 32-b digital signal processor (TMS320F2812), which is a Texas Instrument product. The EV inverter system is controlled in open loop based on the operation of variable voltage–variable frequency and SVM.

The experimental switching frequency is 20 kHz, and the output current frequency is 93 Hz. Fig. 17 shows the measured waveforms with respect to the proposed scheme 2. As shown in the oscilloscope screen, CH1 and CH2 represent the output current (upper waveform) and capacitor current (lower waveform), respectively. Fig. 17(b) illustrates a detailed look of the output current and the capacitor current, the overall views of which being shown in Fig. 17(a). The current signals are sensed by Rogowski coils, which are transducers for measuring

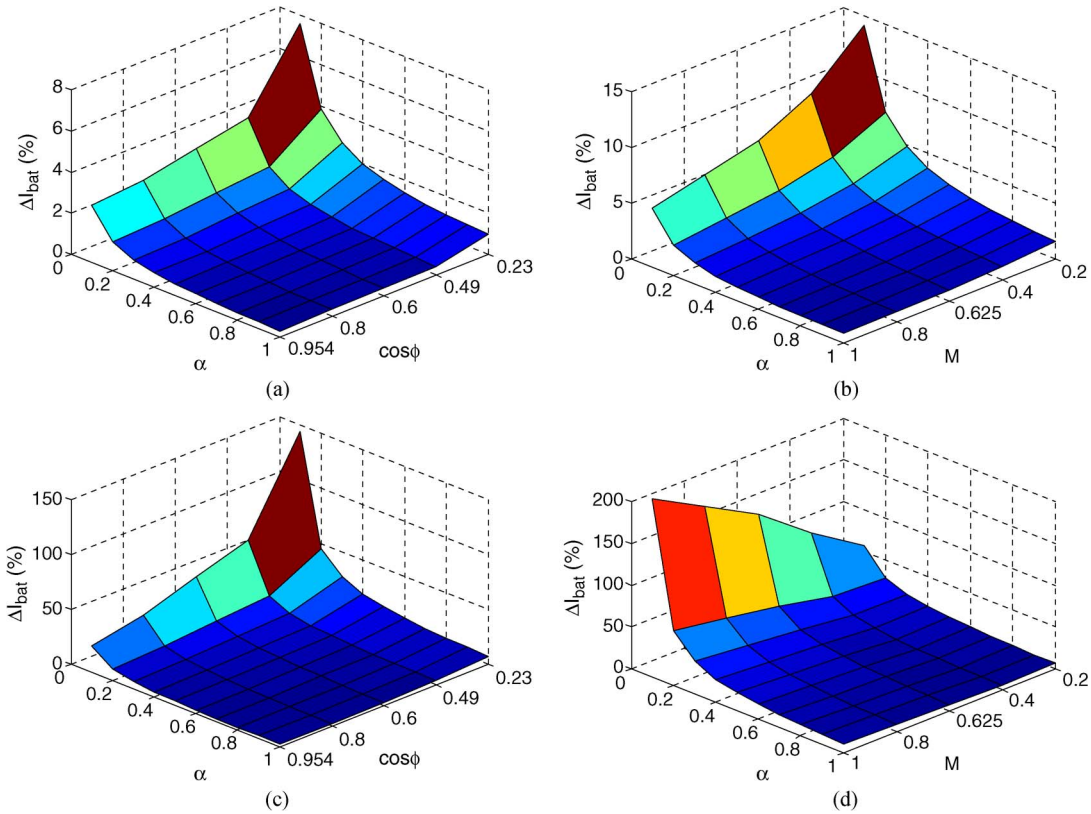

Fig. 15. Battery ripple current analysis for two design schemes (five 3300-μF electrolytic capacitors and two 220-μF film capacitors). (a) $\Delta_{I_{\rm bat}}$ with cosϕ and α in scheme 1. (b) $\Delta_{I_{\rm bat}}$ with M and α in scheme 1. (c) $\Delta_{I_{\rm bat}}$ with cosϕ and α in scheme 2. (d) $\Delta_{I_{\rm bat}}$ with M and α in scheme 2.

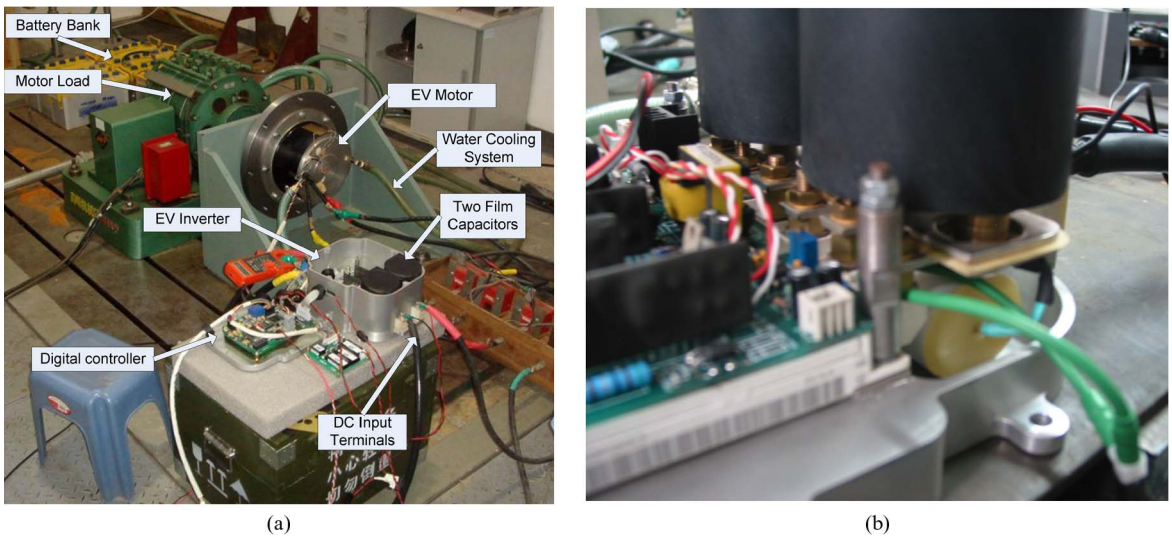

Fig. 16. Photos of the experimental setup and the testbed. (a) Complete EV inverter testbed. (b) Inside the EV inverter assembly, which shows two film capacitors.

ac or high-frequency current pulses. The current waveforms are represented as voltage signals and shown in the oscilloscope screen. Considering that the scale factors are 2 and 1 mV/A for CH1 and CH2, respectively, the actual current scales are 100A/div for both channels.

The experiment shows that the ripple current spectrum contains significant switching frequency multiples and their SBs, as predicted by the analysis in Section III-C. Each film capacitor absorbs 38-A ripple current, as shown in Fig. 17(a) and (b). Thus, the test shows the total ripple current through the film capacitor banks is 76 A when the inverter output current is 135 ARMS. Considering the high load power factor (cos$\phi >$ 0.9) of the PM motor and the modulation index ($M = 0.6$), the measured ratio $I_{\rm cap}/I_N$ was 0.4, which is consistent with (6), as illustrated in Fig. 3.

Fig. 18 shows the experimentally measured waveforms with respect to scheme 1 using five electrolytic capacitors. As shown in the oscilloscope screen, CH1 and CH2 represent the high-frequency capacitor current (upper waveform) and output current (lower waveform), respectively. Considering that the

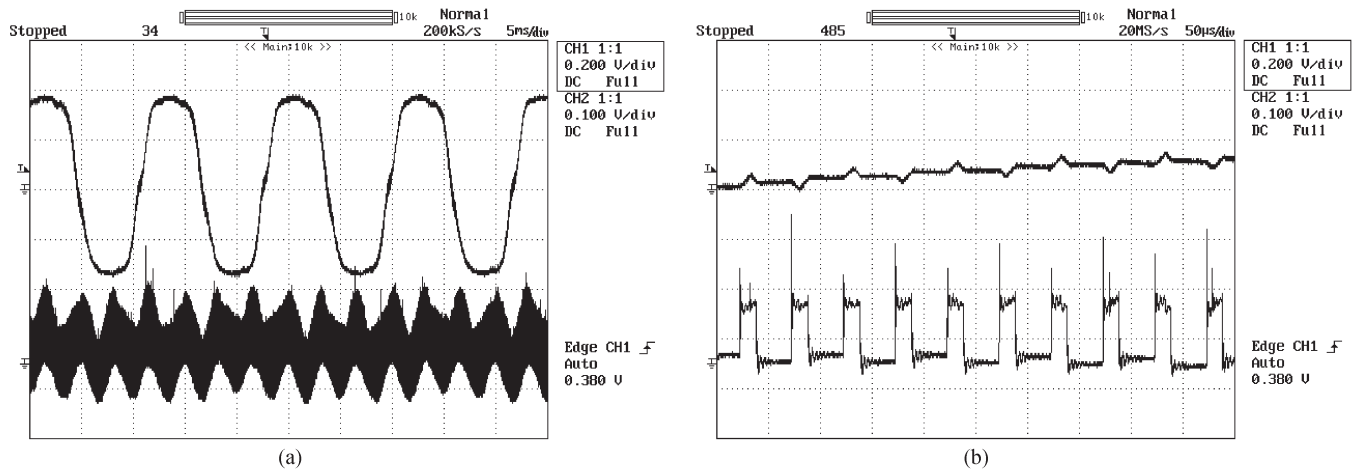

Fig. 17. Measured waveforms of scheme 2 using two film capacitors. (a) Output phase current (the upper waveform with a scale factor of 2 mV/A) and film capacitor current (the lower waveform with a scale factor of 1 mV/A). (b) Zoomed-in detailed look of the output phase current (the upper waveform with a scale factor of 2 mV/A) and film capacitor current (the lower waveform with a scale factor of 1 mV/A).

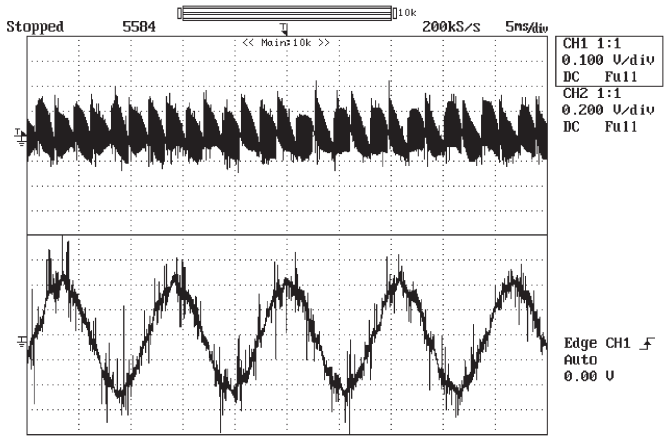

Fig. 18. Measured dc-link capacitor current (the upper waveform with a scale factor of 5 mV/A) and output phase current (the lower waveform with a scale factor of 2 mV/A) of scheme 1 using five electrolytic capacitors to drive the 80-kW PM motor.

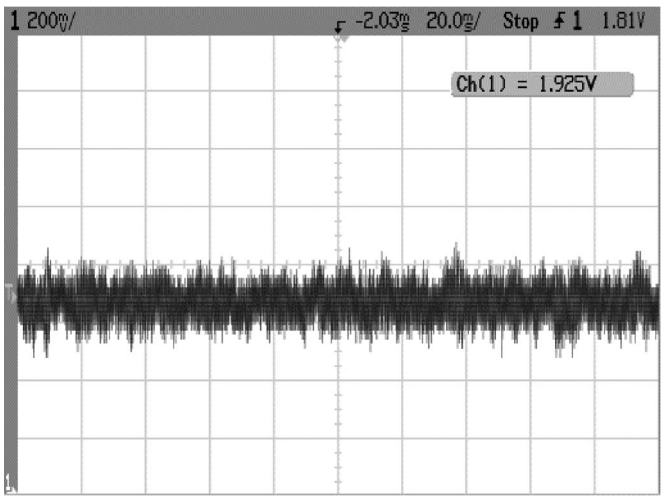

Fig. 19. Measured dc bus voltage using the proposed design scheme with a scale of 0.2 V/div that should be calibrated to 35 V/div, considering the practical measurement circuit.

correspondingly scale factors are 5 and 2 mV/A, the actual current scales are 20 and 100 A/div for CH1 and CH2, respectively. The individual electrolytic capacitor ripple current is 16.2A.

TABLE XI
PERFORMANCE COMPARISON OF TWO DESIGN SCHEMES

Parameters	Scheme I	Scheme II
Capacitance (mF)	16500	440
Capacitor type	Electrolytic	Film
Measured parasitic inductance (nH)	124	34
Measured ripple current (A)	81	76
Power loss (W)**	40.8	20.6
Core temperature (°C)**	73.3	75.5
Life expectancy (Hours) for T_a=65 °C	16092	181530
ΔI_{bat} for α=0.6	1.8%	8.7%
Switching voltage spike across IGBT (V)*	57	35
PDW (kW/kg)	4.67	11
PDV (kW/L)	2.99	13.3

* With 2µF snubber capacitor; **for T_a = 65 °C and cos(ϕ) = 0.954

TABLE XII
SPECIFICATION OF THE VRLA BATTERY (6-DM-150)

Parameters	Value
C20	150 Ah
Cold Cranking Amperes defined by BCI	300 A
Rated voltage	12 V
Weight	32.5 kg

Thus, the five electrolytic capacitors share the total 81-A ripple current through the parallel interconnected capacitor bank. It demonstrates that each film capacitor can handle more ripple current due to the low ESR characteristics.

The dc bus voltage ripple is recorded and shown in Fig. 19 when the drive system is operated at a rated capacity of 80 kW. The measured waveform is zoomed in at the center of the oscilloscope screen for a clear look. A scale of 0.2 V/div represents the actual voltage scale of 35 V/div when the measurement scale factor is considered. The oscilloscope screen shows the measured RMS, and the peak values are 1.81 and 1.925 V, which represent the actual 317-V RMS dc voltage and the actual 337-V peak voltage, respectively. Therefore, the ripple magnitude is recorded as 6.31% of the dc bus voltage.

TABLE XIII
SPECIFICATION OF EVOX RIFA ALS332QP500 AND AVX FFVE6K0227K

Comparison Items	Max ESR at 20 °C/100Hz	Max Impedance at 20°C /10 kHz	Ripple current at 85°C & 10 kHz	Life time L_b at 85°C	Expected ambient temperature T_a
ALS332QP500	51 mΩ	32 mΩ	26.4 A	4000 hrs	65 °C
FFVE6K0227K	1 mΩ	-	100 A	30000 hrs	65 °C

TABLE XIV
MAIN PARAMETERS OF THE AC INDUCTION MOTOR

Parameters	Value
Stator resistor (mΩ)	6.8
Stator leakage inductance (mH)	0.071789
Rotor resistor (mΩ)	4.23
Rotor leakage inductance (mH)	0.0921067
Mutual inductance (mH)	2.2857359
Pairs of poles	3
Rated speed (rpm)	1860

E. Summary of Experimental Results

Table XI summarizes the performance comparison between the two design schemes. The main parameters of two schemes are defined in Table V. Scheme 2 shows significant advantages with regard to the small size, low parasitic inductance, long lifetime, reduced bus voltage spikes, and improved power density. It is shown that the power density increased to 13.3 kW/L by applying scheme 2, in contrast with an increase of 2.99 kW/L by using scheme 1. For the battery ripple current, the constraint of $\alpha > 0.6$ is required for scheme 2. This is achievable by considering the practical layout of EVs.

VI. CONCLUSION

This paper has presented a comprehensive analysis and comparative evaluation of dc-link capacitors to meet the EV system requirements of long lifetime, high reliability, low cost, and high power density. The main findings and contributions of this paper are summarized as follows.

1) *Modulation strategy*. With regard to the dc-link capacitor ripple current, the three modulation strategies, i.e., SPWM, SVM, and THI, approximately show the same RMS values. Considering the ripple voltage, THI modulation shows the lowest value across the dc-link capacitors, followed closely by SVM. However, THI results in the highest capacitor power loss, which is 10% higher than that of SVM. Capacitor power losses correspond to the ripple frequency spectrum, which is different among modulation strategies. SVM shows a moderate impact on the capacitor power loss, which is roughly 3% more than that of SPWM.
2) *Influence of operating conditions*. Operating conditions of EV inverters may be expressed in terms of the practical ranges of load power factor $(\cos\phi)$ and modulation index M. When $\cos\phi$ is less than 0.43, the peak ripple current always results from the upper bound of M. After the threshold (0.43), an increase in the load power factor $\cos\phi$ causes a decrease in $M_{Icap(max)}$, the modulation index that refers to the maximum RMS value of the capacitor ripple. Furthermore, the power factor has a great impact on the frequency spectrum of the dc-link capacitor ripple current. For low $\cos\phi$, the ripple current spectrum is fairly evenly distributed along the switching frequency (f_1) SBs, $3f_1$ SBs, and $2f_1$. For high $\cos\phi$ (larger than 0.49 for SVM), $2f_1$ is the dominant component, and its amplitude increases with $\cos\phi$. The largest harmonic component is nearly 21% of the output current amplitude at low $\cos\phi$, whereas the corresponding harmonic component reaches as high as 48.8% at the high $\cos\phi$.
3) *Modeling of the ESR and self-heating characteristics*. The ESR models of electrolytic and film capacitors are derived and experimentally validated. Two dc-link capacitor designs are used for the comparative evaluation. The ESR of scheme 2 (film capacitor) is always lower than the ESR of scheme 1 (electrolytic) throughout the frequency spectrum. The ESR value of scheme 1 decreases with increasing temperature, which is more significant than that of scheme 2. Furthermore, the RMS values and frequency spectra of the dc-link capacitor current are analyzed. The self-heating effect is subsequently considered and numerically evaluated using the iterative simultaneous solution for core temperature and ESR by an electrothermal coupling method to predict the core temperature. Lifetime estimates are based on the capacitor core temperature.
4) *Experimental evaluation of two design schemes*. The applications and performance of electrolytic capacitors (scheme 1) and film capacitors (scheme 2) were tested, compared, and evaluated in terms of power loss, core temperature, lifetime, and battery current harmonics based on a practical 80-kW PM motor drive system. The comparison verifies that the film capacitor application shows significant advantages in terms of the improved power density, low power loss, low parasitic inductance, and long lifetime. The capacitor power loss that was introduced by scheme 2 is roughly half that of scheme 1 due to the lower ESR value. The analysis shows that the values of the capacitor core temperature are close to each other in both schemes. At the rated ambient temperature of 65 °C, the lifetime of the film capacitors is ten times longer than that of scheme 1. With regard to the battery ripple current, both schemes meet the 10% upper bound limit, considering the practical EV system layout. Furthermore, the parasitic inductance is reduced to 34 nH in contrast with the value of 100 nH for scheme 1. A power density of 13.3 kW/L was achieved by applying the proposed scheme 2, which is compared with 2.99 kW/L for scheme 1.

APPENDIX

See Tables XII–XIV.

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