

Signal Pre-amplification and Peak Detection

Figure S1

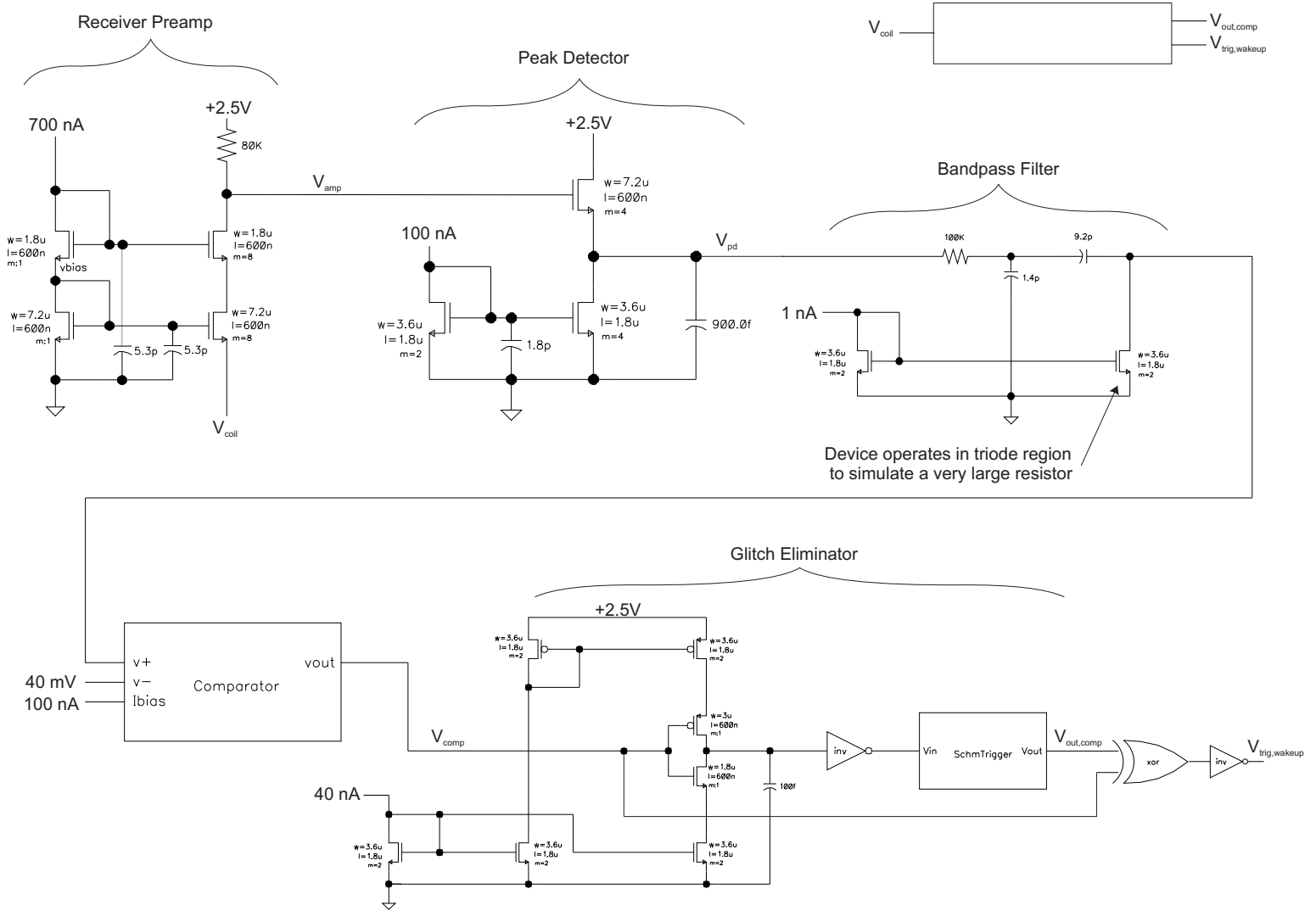
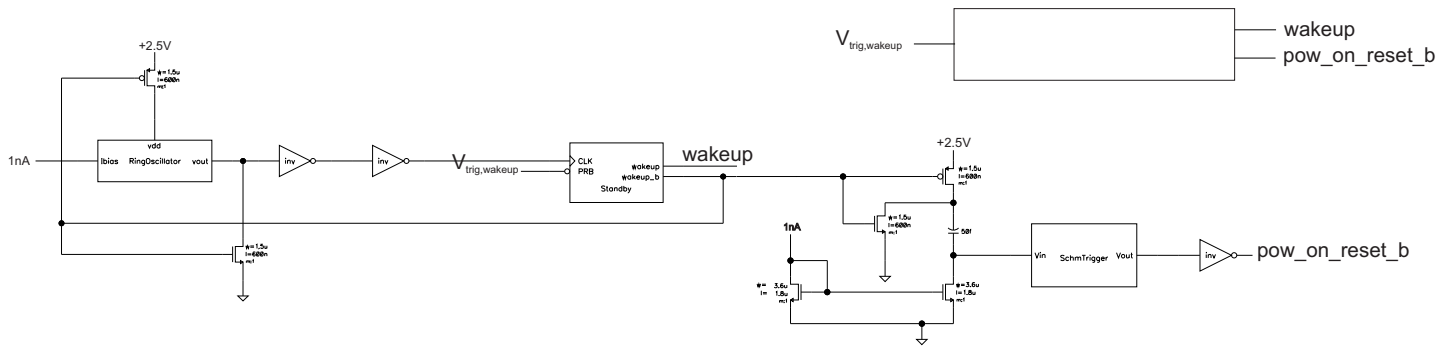
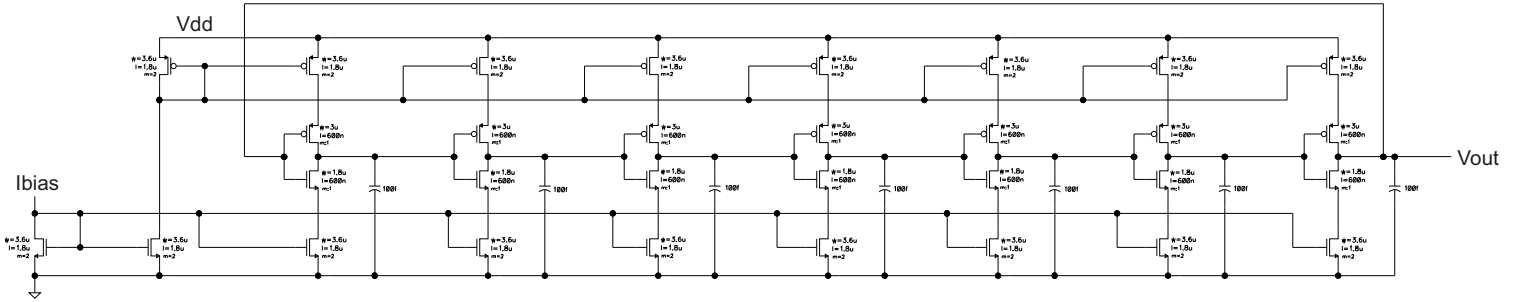


Figure S2

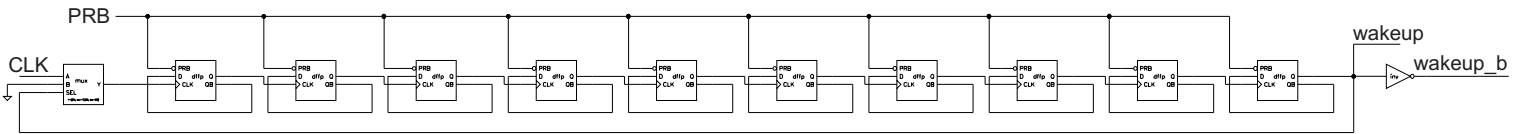
Wakeup Controller (including power-on reset)



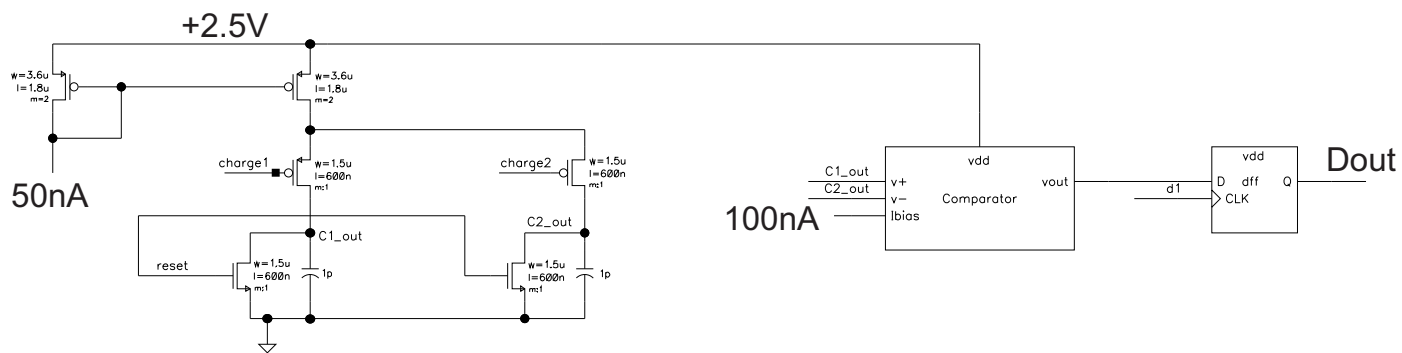
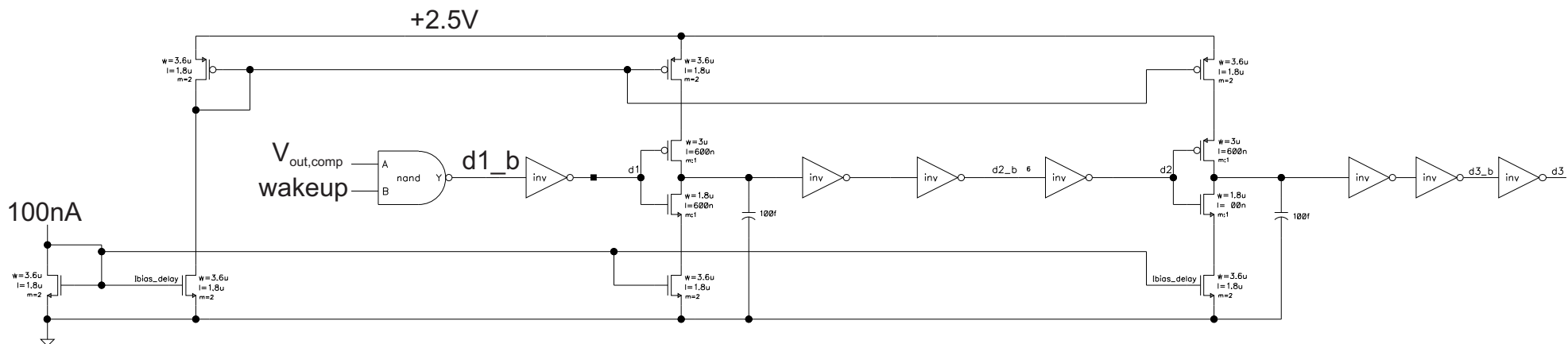
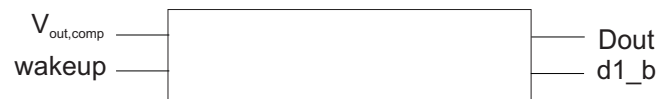
Ring Oscillator



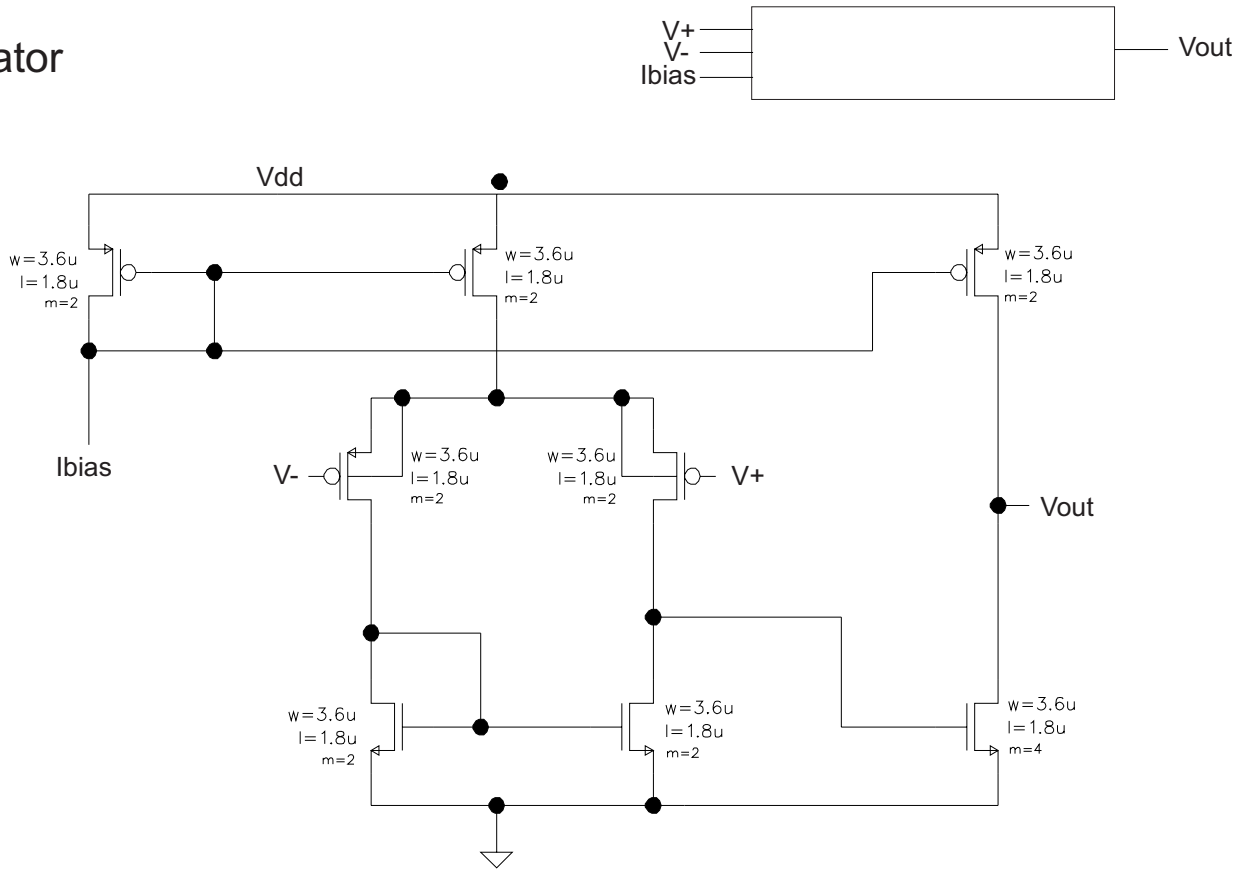
Standby (Counter)



Pulse-Width Demodulator



Comparator



Schmitt Trigger

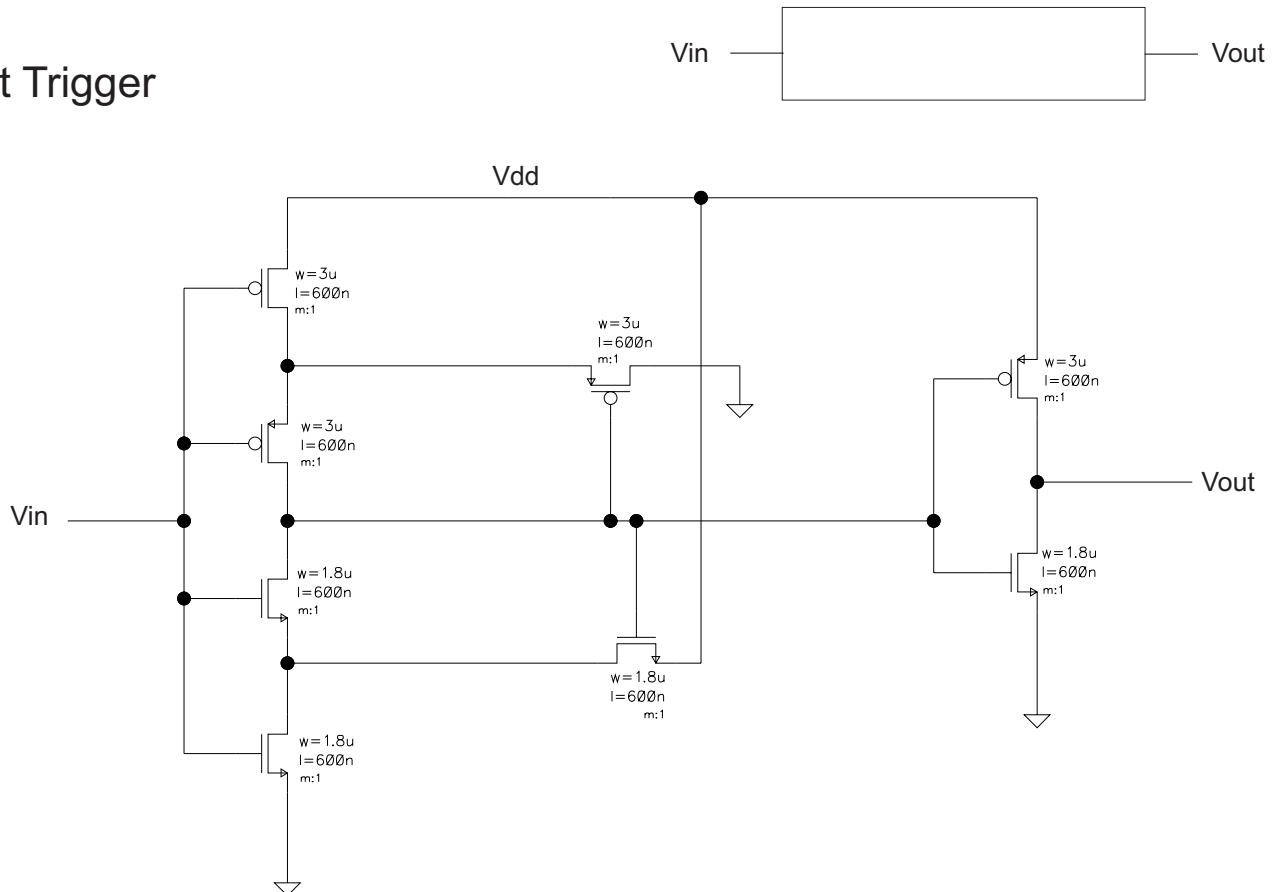


Figure S5

Data Decoding and Stimulus Control

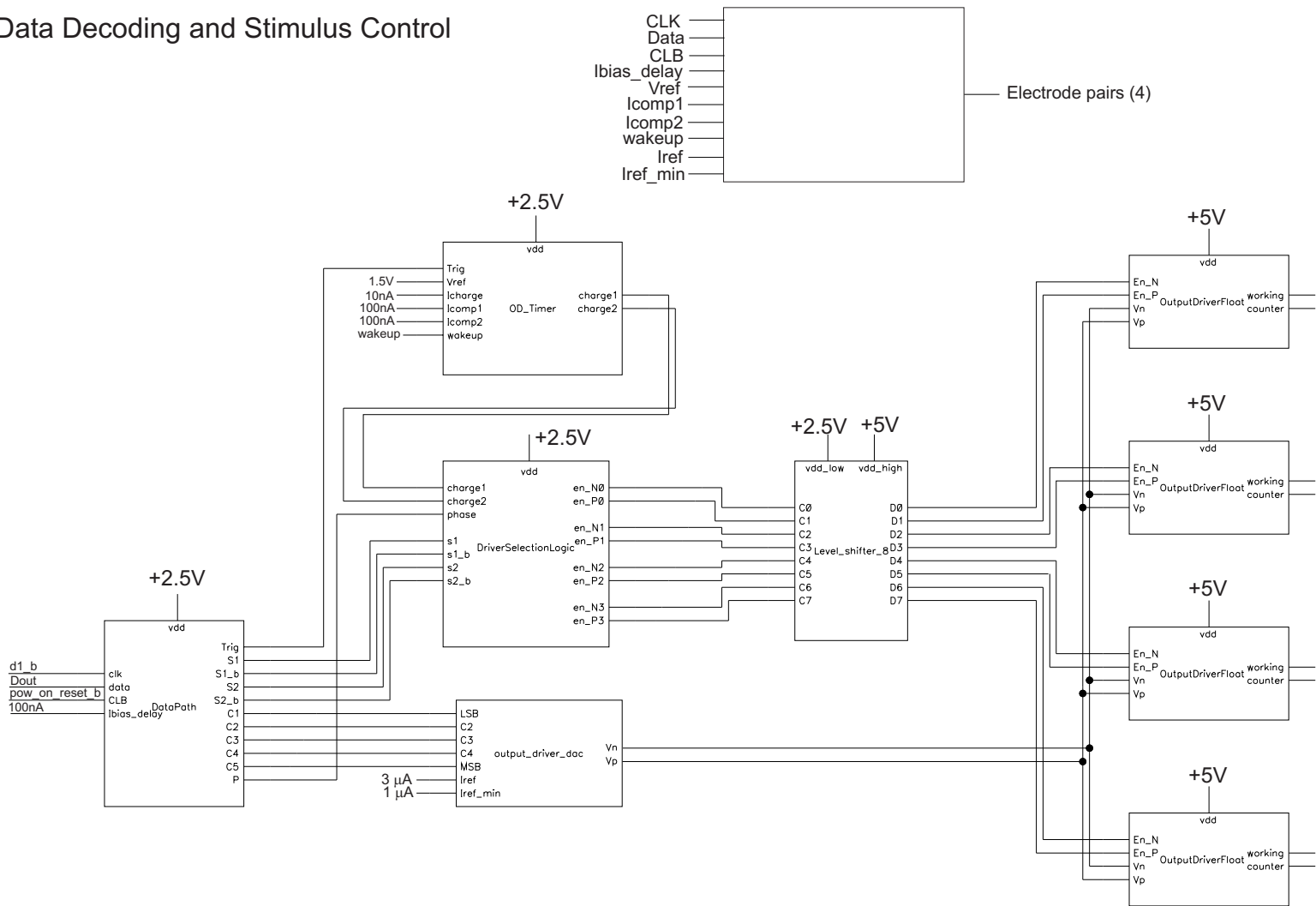
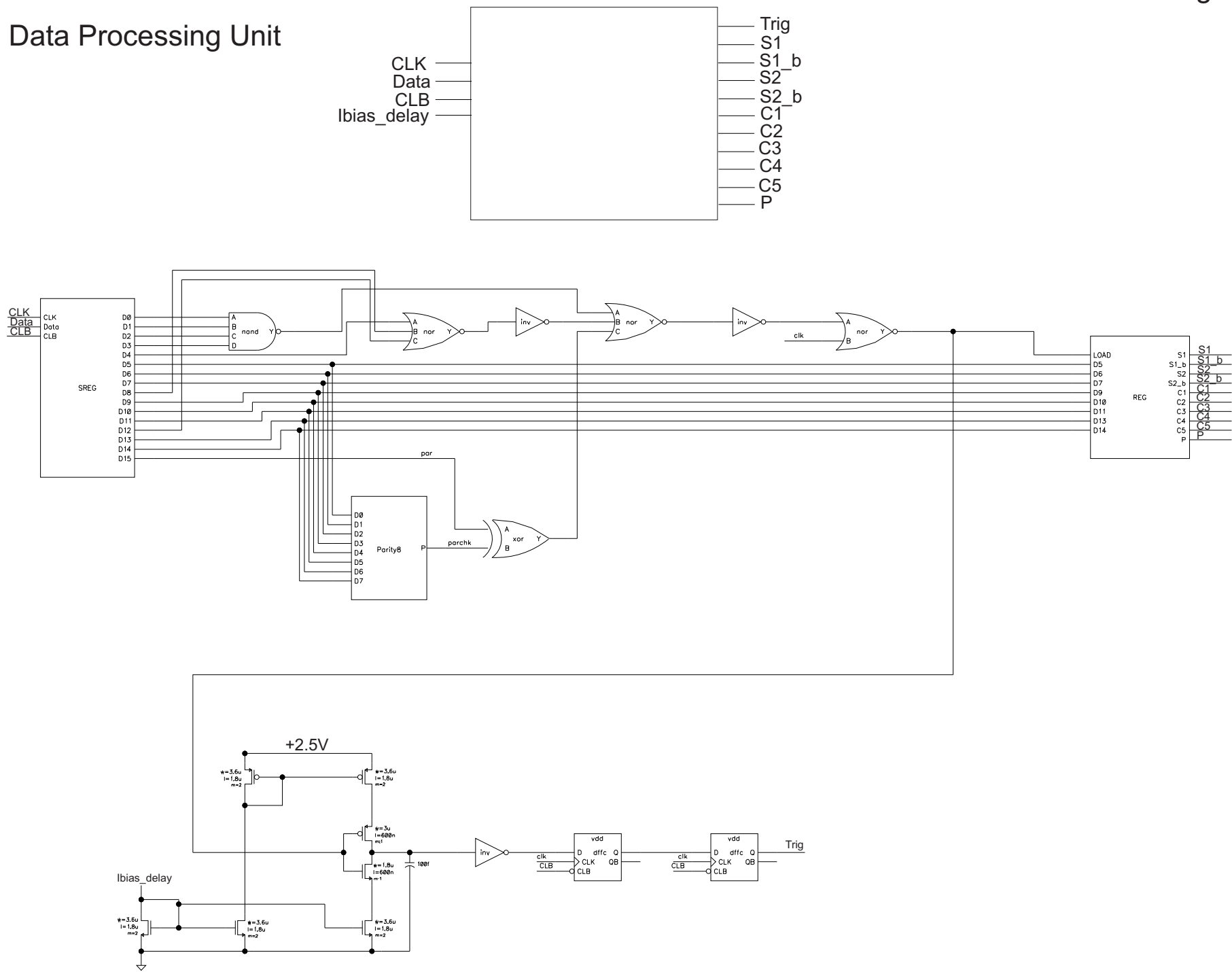


Figure S6

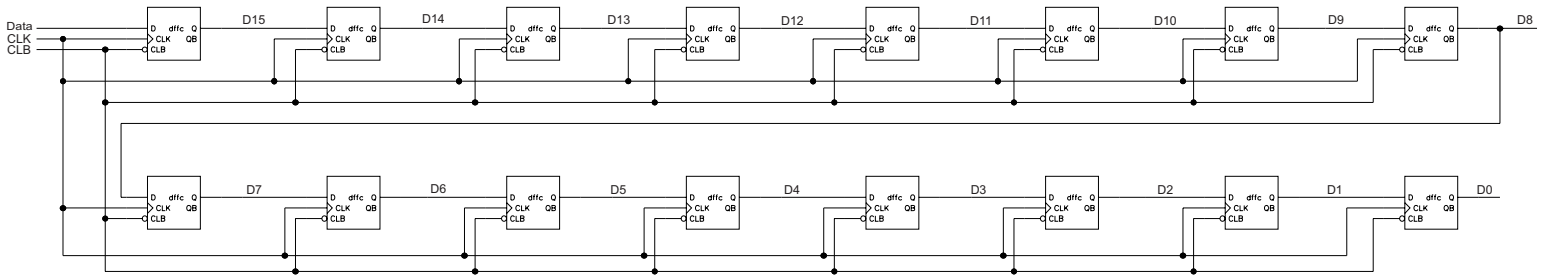
Data Processing Unit



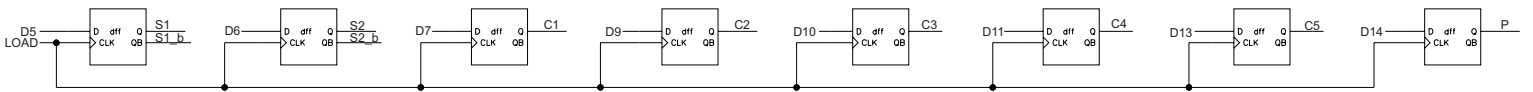
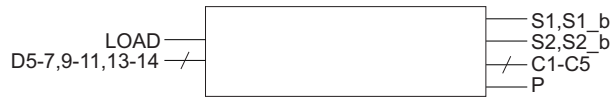
Data Shift Register



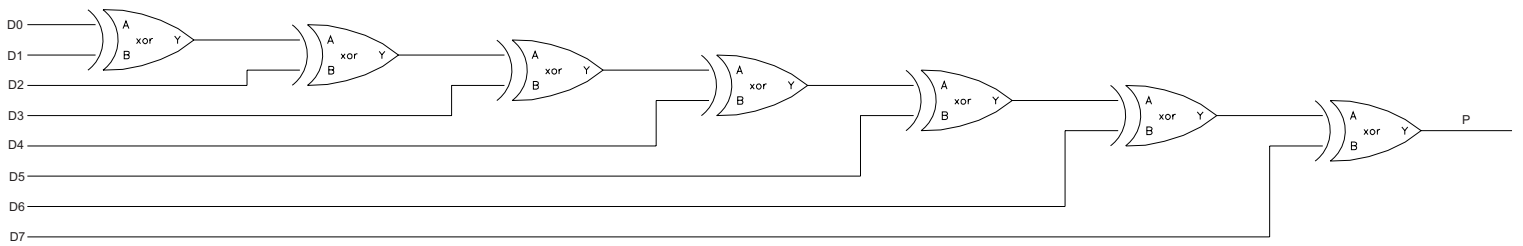
Figure S7



Data Memory



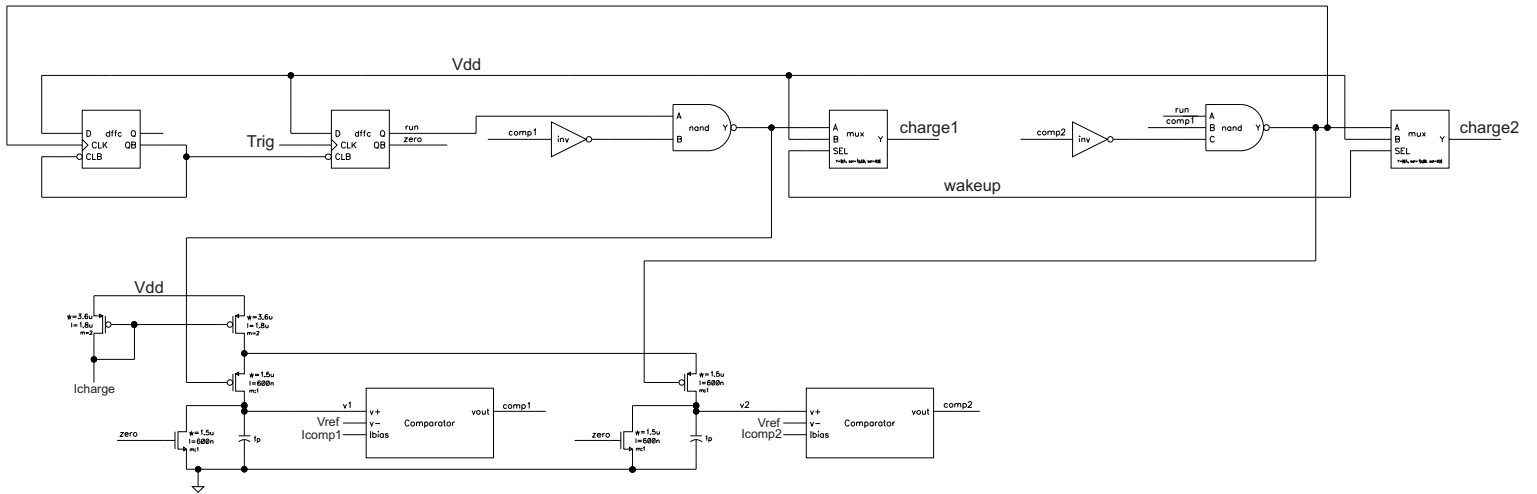
Parity Check



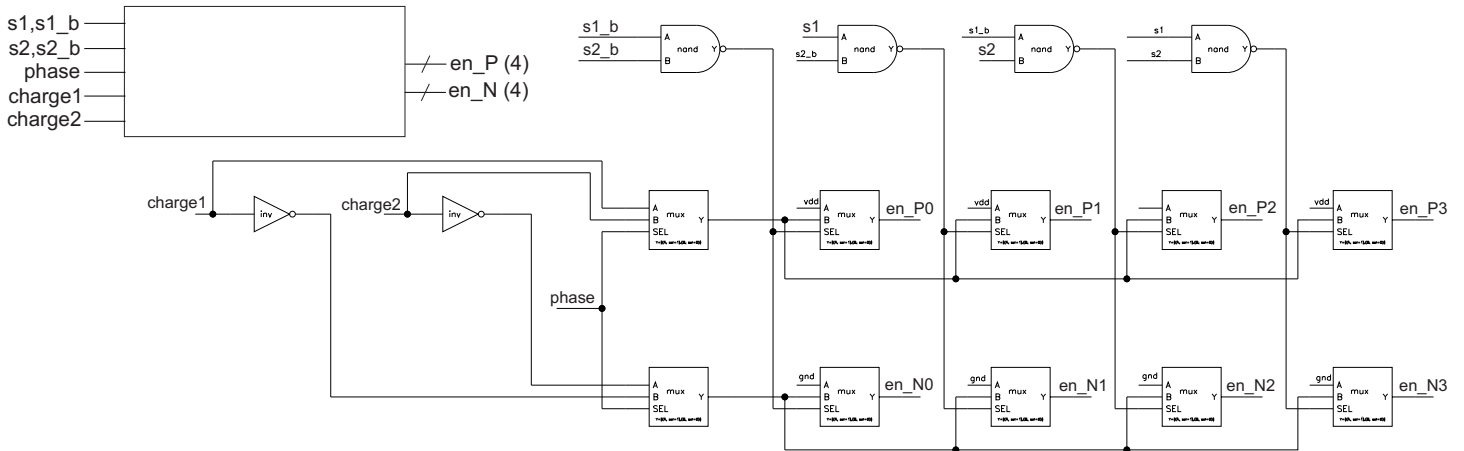
Output Driver Timer



Figure S8



Output Driver Selection Logic



Output Driver (x4)

Supplementary Figure 10

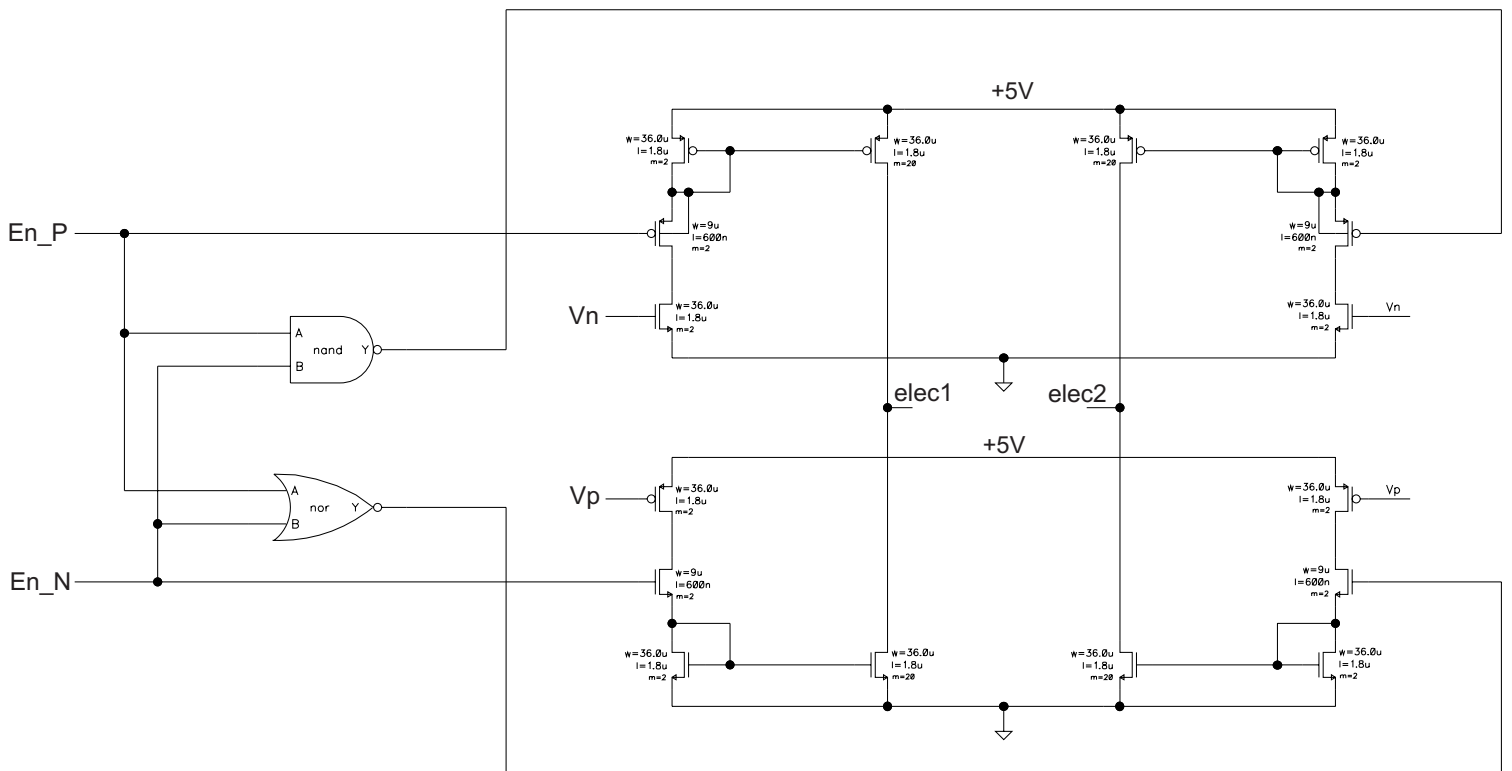
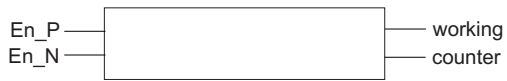
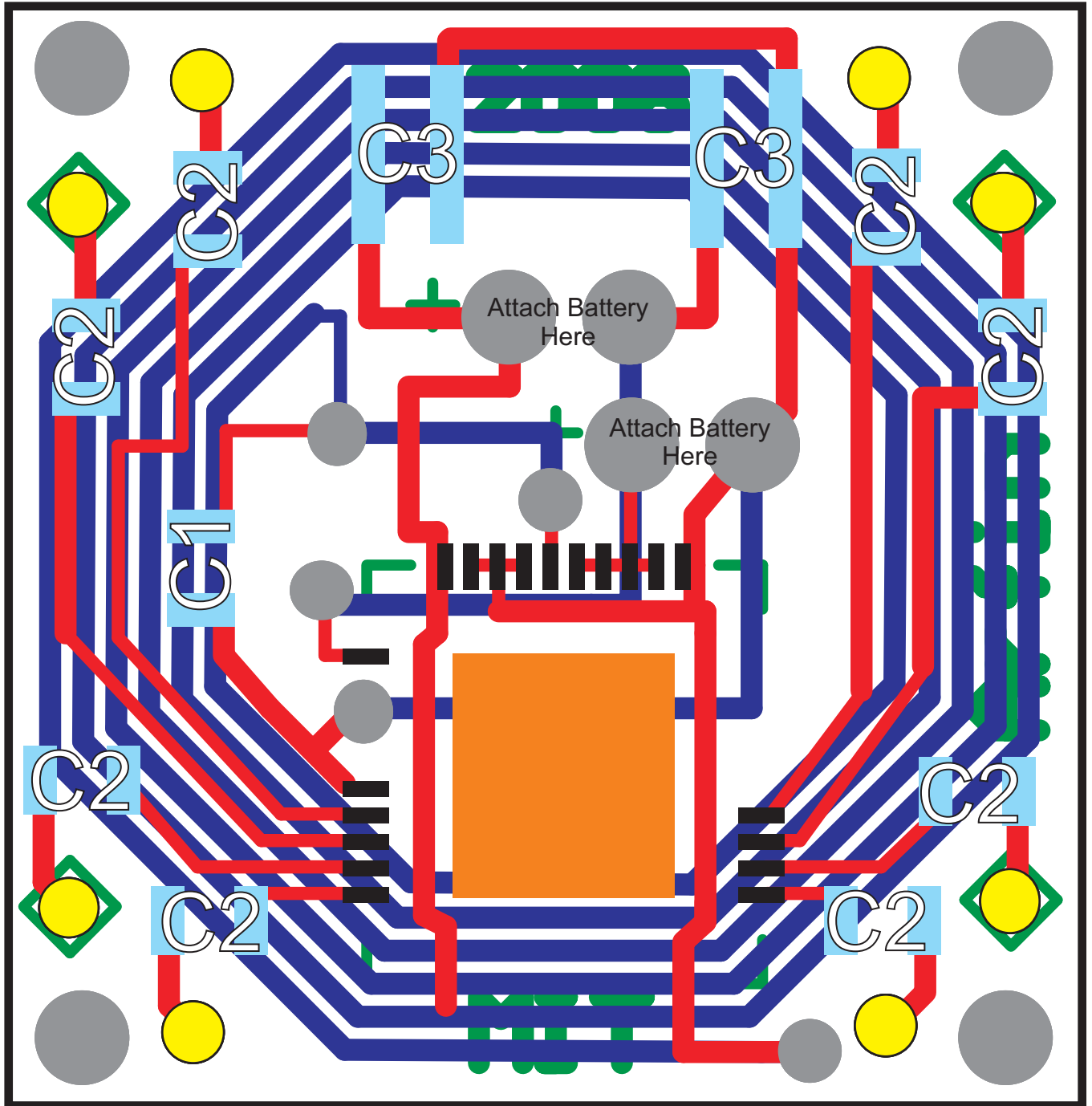










Figure S12



-  Top Metal
-  Bottom Metal
-  Silkscreen
-  Drill/Via
-  Capacitor Pad (top metal)
-  Chip Wirebonding Pad (top metal)
-  Die attach paddle (top metal)
-  Electrode wire connection point (via)

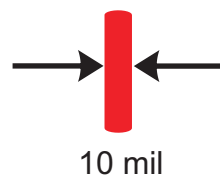
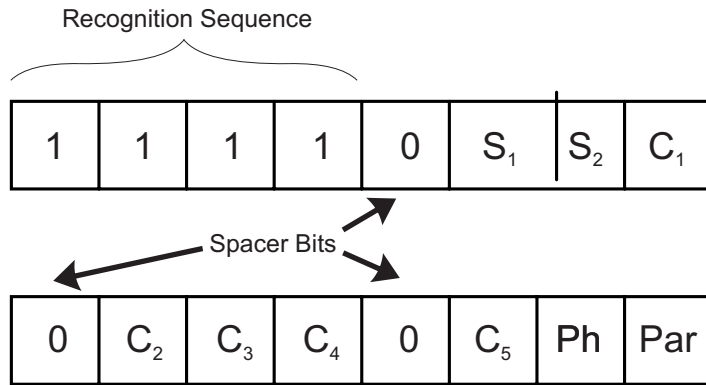


Figure S13



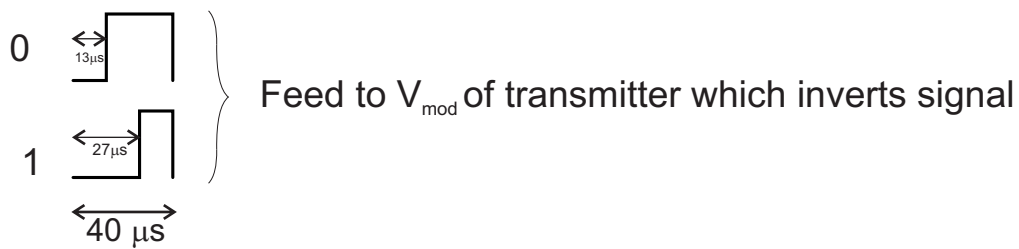
S_1 - S_2 : Output driver selector bits

C_1 - C_5 : Current level selector bits
















Ph: Phase selector bit

Par: Parity check bit

Encoding data with PWM



Glossary of Symbols

	Capacitor
	Resistor
	Inductor
	NPN bipolar junction transistor (BJT)
	N-channel metal-oxide-semiconductor field-effect transistor (MOSFET)
	P-channel MOSFET
	Latched comparator
	Schmitt trigger
	Inverter
	NAND
	NOR
	Exclusive OR (XOR)
	Switch
	Pulse voltage source
	DC current source

Figures S1-S11 present the complete schematics for the custom integrated circuit used in the wireless neural stimulation device. Each schematic shows a portion of the overall circuit and gives a summary of its inputs and outputs as a block. Also included are all MOSFET length and widths, resistor, capacitor, and bias current values.

FIGURE LEGENDS

Figure S1. Signal pre-amplification and peak detection. Schematics are given in detail for the receiver preamplifier, peak detector, bandpass filter, comparator (Figure S4), and glitch eliminator. The bandpass filter conditions the peak detector waveform by removing any high frequency ripple due to the RF carrier and AC-couples the signal to the comparator. The glitch eliminator uses a current-limited inverter to reject any digital pulses that are too narrow in width (as determined by the load capacitor and limiting current). A Schmitt trigger (Figure S4) ensures that the edges of $V_{out,comp}$ are fast. The glitch eliminator also produces the delayed copy of the comparator signal needed to produce $V_{trig,wakeup}$ every time a transition in the comparator signal is detected.

Figure S2. Wakeup controller, with ring oscillator and standby counter. The circuit schematic of the wakeup controller is given in detail. When the signal $V_{trig,wakeup}$ is received, the standby counter (constructed using a ripple cascade of flip-flops) is preset such that all state variables are 1. The wakeup trigger also turns on a ring oscillator which clocks the standby counter, decreasing its stored value by 1 each clock cycle. The output of the final flip-flop in the counter determines the value of *wakeup*. If the chip is receiving a stream of data, $V_{trig,wakeup}$ is received repeatedly which keeps resetting the counter to the maximum value. If the counter reaches zero before another $V_{trig,wakeup}$ trigger pulse is received, the chip will go to sleep. The duration of the timeout is set by the size of the counter and the frequency of the ring oscillator. In this design, a 10-bit counter encoding 1024 values is designed to run down in about 1 second.

Figure S3. Pulse-width demodulator. This schematic is a more detailed version of that given in Figure 2C. This circuit and all subsequent circuits are inactivated when *wakeup* is low. A set of current-limited inverters produce delayed copies of the input signal, $V_{out,comp}$. Combinations of the input and delayed copies of itself are used to produce the four timing phases needed for the pulse-width demodulator.

Figure S4. Comparator and Schmitt trigger. Full schematics provided.

Figure S5. Data decoding and stimulus control. The data recovered by the PWM demodulator is passed into a Data Processing Unit (Figure S6). Once the data is decoded, a digital-to-analog converter (DAC) (Figure S9) is configured and the appropriate output driver is selected (Figure S10). A timer circuit (Figure S8) controls the timing of the stimulus. A set of level shifters (Figure S9) convert the control signals from the low-voltage power supply (2.5 V) to the high-voltage power supply (5.0 V). The stimulus itself is supplied by the output driver circuit (Figure S10).

Figure S6. Data processing unit. The data processing unit (DPU) receives demodulated data from the PWM demodulator. These data are fed into a shift register (Figure S7). The DPU looks at the data in the shift register in parallel and checks for a recognition sequence of all 1's in bit positions 0-3. It also checks that bit positions 4, 8, and 12 contain 0's. This is required so that is impossible for other data, when transmitted correctly, to mimic the recognition sequence. Additionally, it also calculates a parity bit (Figure S7) for the actual stimulation parameters (bits 5-7, 9-11, 13-14) and compares that to the parity bit transmitted (bit 15). If all checks pass, the stimulation parameters are transferred from the shift register into another set of memory registers (Figure S7). Once the stimulus parameters are stored in memory, a trigger pulse is generated to initiate the stimulus. Because the stimulation parameters are now stored in memory, new data can be transmitted and loaded into the shift registers.

Figure S7. Data shift register, data memory, and parity check. The data shift register and data memory registers use ordinary flip-flops. Any general purpose flip-flop design should be acceptable. The parity bit is calculated by a simple XOR applied to all inputs simultaneously.

Figure S8. Output driver timer and output driver selection logic. The output driver timer is based on a one-shot topology, where a current charges a capacitor to a threshold. This times the first pulse. Once the threshold is reached, a current charges a second capacitor to the same threshold. Once both thresholds are reached, the voltage on both capacitors is reset to zero. This results in a stimulus consisting of two identical pulses. The output driver selection logic works by taking the stimulus timing and passing it to the correct output driver using a set of combinational and multiplexer based logic. Only the selected output driver receives the timing pulse.

Figure S9. Output driver DAC, OTA, and level shifter. The DAC provides a reference voltage to the output drivers. Based upon the stimulation parameters selected by the user, the DAC generates a scaled copy of the intended stimulation current using a combination of binary-weighted current sources. The DAC outputs this current as a transistor gate voltage for both NMOS and PMOS transistor types. Because the PMOS voltage must be reference to the higher 5 V power supply, a regulated cascode implemented using an operational transconductance amplifier (OTA) is used to make a more accurate current mirror.

Figure S10. Output driver. The output driver circuit is essentially a current-mirror which accepts the voltages V_n and V_p generated by the DAC to generate a reference current which is scaled up by 10x before being sent to the output. Enable switches controlled by the timer circuit and driver selection circuitry turn the output current on and off. The driver is said to be "floating" because the current source has two outputs, labeled *elec1* and *elec2*, neither which need to be connected to ground.

Figure S11. Current reference. The current reference produces a constant output independent of the supply voltage. This current is automatically generated by the chip

and then scaled using a series of current mirrors to provide the bias currents to all circuits on the chip. See Mandal, S. Arfin, S. Sarpeshkar, R., "Fast startup CMOS current references," *Proceedings of the IEEE Symposium on Circuits and Systems (ISCAS 2006)*, pp. 2845-2848.

Figure S12. PCB Layout.

Parts Table

Capacitor	Value	Digikey Part Number
C1	270 pF	PCC1714CT-ND
C2	0.22 μ F	PCC2272CT-ND
C3	1 μ F	PCC2189CT-ND

C_1 is the resonant capacitor in parallel with the receiver coil. C_2 are the DC blocking capacitors in series with every electrode output. C_3 are power supply bypass capacitors, placed in parallel with the batteries. The chip is placed on the die attach paddle and wirebonded to the board and covered in epoxy encapsulation. The only electrical connections required are for the batteries, the input from the coil, and the 8 outputs corresponding to the 4 electrode pairs.

Figure S13. Data packet organization.

Figure S14. Glossary of symbols.