

# Sub- $\mu$ Hz MOSFET $1/f$ noise measurements

S. Mandal, S.K. Arfin and R. Sarpeshkar

The  $1/f$  noise in integrated NMOS transistors at sub- $\mu$ Hz frequencies was measured by developing a simple and inexpensive common-mode noise-cancellation technique to attenuate the effects of temperature fluctuations. The noise has a power-law spectrum with slope  $-1.2$  and an approximately Gaussian amplitude distribution.

**Introduction:** Previous work in bulk semiconductors has shown that  $1/f$  noise continues down to  $0.5 \mu\text{Hz}$  [1], but we were unable to find MOSFET  $1/f$  noise spectra at such low frequencies. The amplitude distribution, which is important for evaluating reliability, was also unavailable for MOSFETs. However, Gaussian distributions have been measured in bulk semiconductors and discrete carbon resistors [2–4], as predicted theoretically [5]. Deviations from Gaussian behaviour have been found in small ( $\mu\text{m}$  scale) resistors [6] and thin resistive films [7]. The main challenge of such long-term measurements is eliminating temperature fluctuations. The usual approach has been to carry out the experiment inside a temperature-stabilised oven, but such equipment is expensive and hard to obtain. In this Letter, we describe a noise-cancellation technique that attenuates the effects of temperature fluctuations and allows us to perform such measurements simply and inexpensively.

**Methods:** Our experimental setup is shown in Fig. 1. The test devices were two NMOS transistors of size  $3.6 \times 1.8 \mu\text{m}$  and  $9 \times 3.6 \mu\text{m}$  fabricated in the AMI  $0.5 \mu\text{m}$  CMOS process. The transistors were biased at the same gate voltage, resulting in average drain currents of  $\bar{I} = 10 \mu\text{A}$  and  $5 \mu\text{A}$ , respectively. Each current was converted into a voltage with a resistor of value  $R_L = 100 \text{ k}\Omega$ . Each voltage was sampled at a rate of  $0.946 \text{ Hz}$  with a Keithley 2400 source-meter. The setup was powered by a 5Ah lead-acid battery with a fully-charged open-circuit voltage of  $V_{bat} = 2.15 \text{ V}$  and placed inside a grounded metal box to reduce noise pickup from environmental electromagnetic fields. It was kept in a room where the temperature fluctuated around  $298 \text{ K}$  by approximately  $\pm 1 \text{ K}$ .

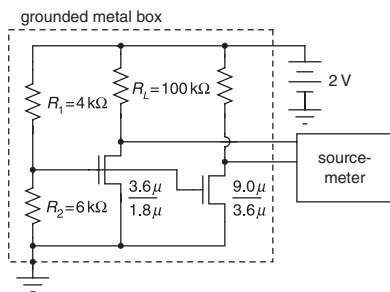


Fig. 1 Experimental setup

A potential source of measurement error arises from the well-known fact that discrete resistors themselves exhibit  $1/f$  noise. We therefore ran a calibration test where we replaced our experimental setup with a simple resistive divider connected between  $V_{bat}$  and the ground. Two resistors identical to  $R_L$  ( $0.5 \text{ W}$ , carbon) were used in the divider. The measured noise in this case was significantly lower than that seen with the transistors present, and even lower than the  $\pm 10 \text{ pA}$  resolution of our source-meter. Therefore any noise due to the resistor or the battery is negligible compared to the transistor noise.

**Results:** The gate voltage  $V_G$  droops along with the battery voltage:  $\Delta V_G \simeq 0.6 \Delta V_{bat}$ . As a result, the average drain current of both transistors decreases with time. We decided to limit this decrease to 10% of the initial current to avoid non-stationarity in the noise process. It is easy to show that the allowable battery droop is limited by this requirement to  $0.6 (\Delta I/\bar{I}) V_L$ , where  $\Delta I/\bar{I}$  is the percentage change and  $V_L = \bar{I}/g_m$  is the linear range of the transistor. Using  $\Delta I/\bar{I} = 0.1$  (i.e. 10%) and  $V_L = 180 \text{ mV}$  gives us  $\Delta V_{bat} = 30 \text{ mV}$ . Experimentally, the battery voltage drooped at an approximately constant rate of  $0.5 \text{ mV/day}$ , corresponding to a maximum time-span of 60 days and limiting our

lowest measurable frequency to  $\simeq 0.2 \mu\text{Hz}$ . The droop was removed from the time-domain record before further signal processing.

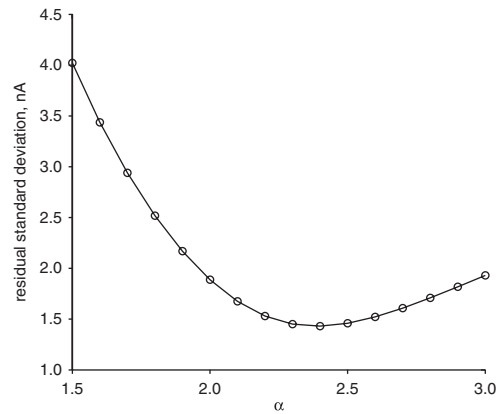


Fig. 2 Measured standard deviation of  $\Delta I' = \Delta I_2 - \alpha \Delta I_1$  against parameter  $\alpha$

The main goal of measuring two transistor currents simultaneously was to eliminate the effects of temperature fluctuations. The total drain current fluctuation  $\Delta I$  can be divided into a temperature-independent part  $\Delta I_n$  and a temperature-dependent part  $\Delta I_T$ , i.e.  $\Delta I = \Delta I_n + \Delta I_T$ . However, the transistors are located close to each other on the same die and share the same temperature. Therefore the  $\Delta I_T$  term is correlated across the two transistors, while the  $\Delta I_n$  term is not. MOSFET currents depend polynomially on temperature via two parameters: threshold voltage and carrier mobility in the channel. Since temperature fluctuations  $\Delta T$  are much smaller in magnitude than the average room temperature of  $298 \text{ K}$ , both polynomials can be linearised. As a result,  $\Delta I_T$  is linearly related to  $\Delta T$ , i.e.  $\Delta I_{Ti} = \beta_i \Delta T$ , where  $i$  is 1 or 2 depending on which transistor is being referred to, and  $\beta_i$  is bias-dependent. We now define  $\alpha = \Delta I_{T2}/\Delta I_{T1}$ , where  $\alpha \equiv \beta_2/\beta_1$ . The effects of temperature fluctuations are therefore eliminated in the linear combination  $\Delta I' = \Delta I_2 - \alpha \Delta I_1$ .

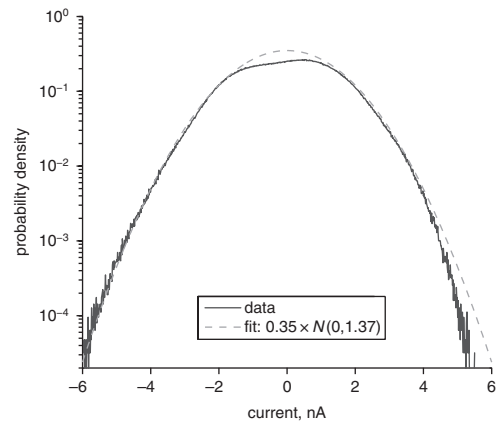


Fig. 3 Measured amplitude distribution and fit to a Gaussian with zero-mean and  $1.37 \text{ nA}$  standard deviation, denoted by  $N(0, 1.37)$

Fig. 2 shows the standard deviation of  $\Delta I'$  against  $\alpha$  for 60 days of data. We use  $\alpha = 2.4$  since, as shown in the Figure, this choice minimises the standard deviation of  $\Delta I'$ . The existence of a unique minimum indicates that our assumption of a linear dependence of drain current on temperature is correct. For  $\alpha = 2.4$ , the standard deviation of  $\Delta I'$  is only  $1.46 \text{ nA}$ , compared to  $4.86$  and  $10.18 \text{ nA}$  for  $\Delta I_1$  and  $\Delta I_2$ , respectively. Most of this excess variance accumulates at frequencies below  $0.1 \text{ mHz}$  because of diurnal temperature fluctuations.

To verify that the time-domain samples arise from a stationary random process we divided them into 8 and 16 time windows. The mean square value of the samples in each interval were calculated. This sequence of values was subjected to the runs test, a standard non-parametric test of stationarity [8]. The sequence passed the test with a probability value close to 1 in both cases, indicating that the random process was stationary. Fig. 3 shows the stationary amplitude distribution of  $\Delta I'$  for  $\alpha = 2.4$ . It is well described by a Gaussian with zero mean. The power spectral density (PSD) is calculated using Welch's method with eight

overlapping time-domain windows [9]. Fig. 4 shows the measured PSD of  $\Delta I$  for  $\alpha = 2.4$ . We can see that the spectrum is very nearly a uniform power law with a slope of  $-1.2$  down to approximately  $0.9 \mu\text{Hz}$ , with no traces of diurnal periodicity. Such periodicity, caused by temperature fluctuations, reappears if our cancellation scheme is not used, i.e.  $\Delta I_1$  and  $\Delta I_2$  are analysed separately.

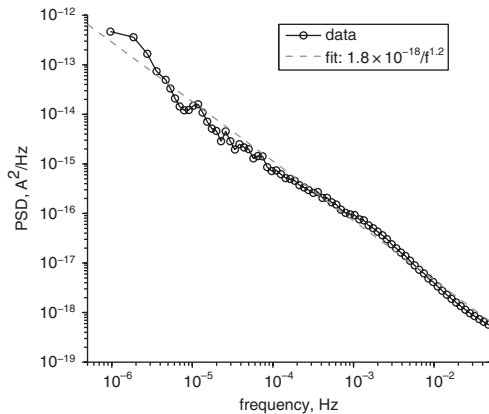


Fig. 4 Measured power spectral density and power-law fit

**Conclusion:** The measured current noise power spectrum of integrated NMOS transistors closely approximates a power law with a slope of  $-1.2$  and shows no signs of flattening out at frequencies as low as  $0.9 \mu\text{Hz}$ .

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S. Mandal, S.K. Arfin and R. Sarpeshkar (*Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, USA*)

E-mail: rahuls@mit.edu

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