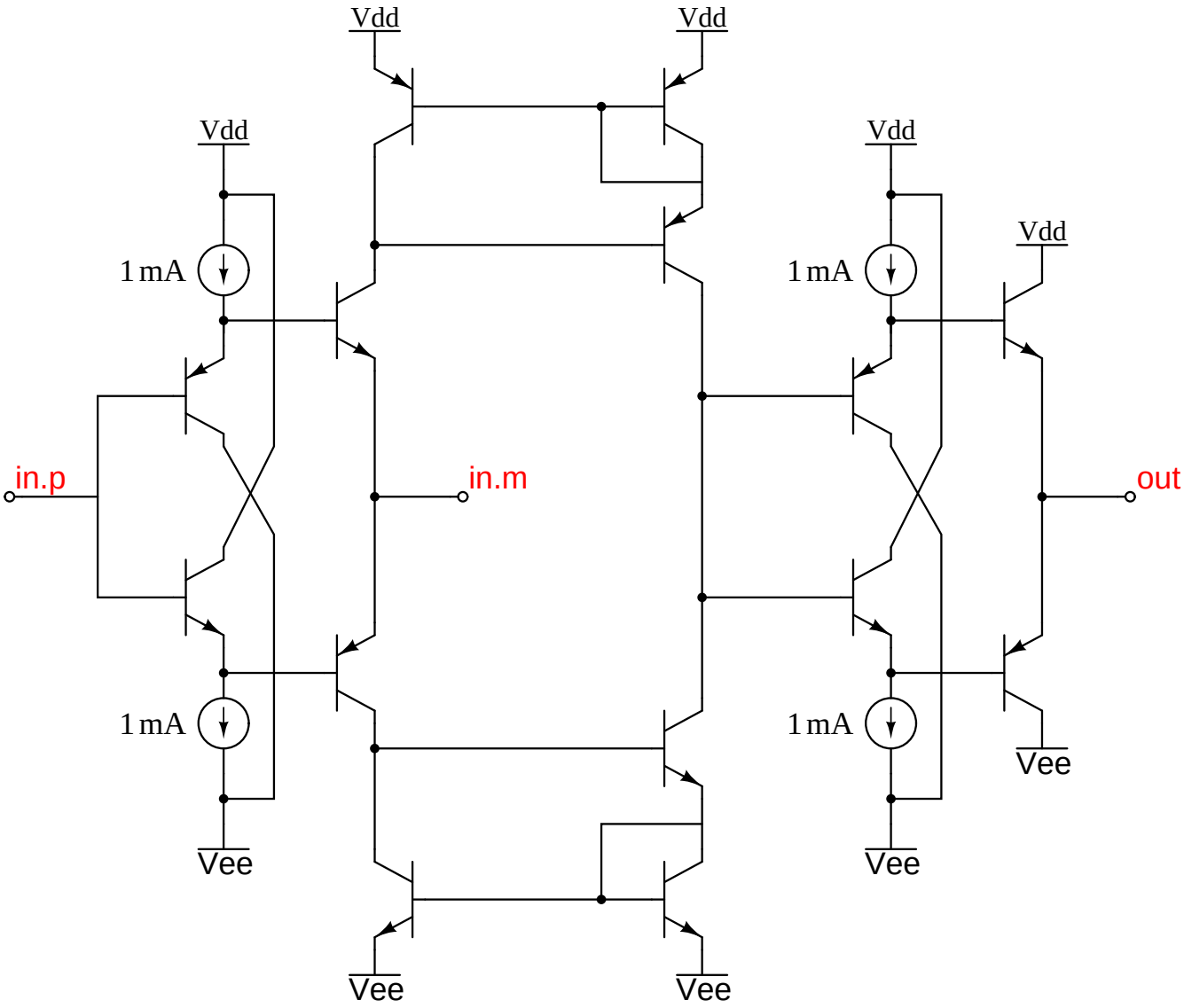


	Specification	Calculated	Simulated
Open-loop transimpedance	> 200 kΩ	500 kΩ	800 kΩ
Input common mode	±10 V	±13.8 V	14.8 V
Output swing	±10 V	±13.8 V	±14.3 V
Output current	± 10 mA	-	±250 mA
Power consumption	< 250 mW	210 mW	205 mW
Phase margin	$> 70°$		74°

Design Process

The three key components of the transimpedance amplifier are the input buffer, current mirror, and output buffer stages. The input buffer is provided for us as a diamond buffer configuration. This leaves the current mirror and output buffer design.

For the current mirror, we want a mirror with low error and a high output resistance. This output resistance will form the transimpedance of the amplifier, and thus needs to be sufficiently large (greater than 200 kΩ). Using a Wilson current mirror, we achieve very low error ($\frac{2}{\beta^2}$) and a high output resistance ($\frac{\beta r_o}{2}$).

For the output buffer, we use the same structure as the input buffer, a diamond buffer. This buffer has low offset, due to the matching V_{be} drops, and a current gain of β^2. The buffer also has a large input impedance to create the high impedance node.

Design Calculations

Open-loop transimpedance

PNP Wilson mirror: $R_{O,\text{PNP}} = \frac{\beta r_o}{2} = 625$ kΩ

NPN Wilson mirror: $R_{O,\text{NPN}} = \frac{\beta r_o}{2} = 5$ MΩ

Output buffer: $R_I = (r_{\pi,\text{NPN}} + \beta_{\text{NPN}}(r_{\pi,\text{PNP}} + \beta_{\text{PNP}}1\text{k}\Omega))||(r_{\pi,\text{PNP}} + \beta_{\text{PNP}}(r_{\pi,\text{NPN}} + \beta_{\text{NPN}}1\text{k}\Omega))$
$R_I = 5.1$ MΩ

$Z = 500$ kΩ

Input and output range

Our input and output buffers are designed to go nearly rail to rail, requiring only the 0.6 V margin for the V_{be} drops. However, the current mirror adds an extra V_{be} drop, so our final input and output swings are $\pm$13.8 V.

Output current

Since our output buffer has a current gain of $\beta_{\text{NPN}}\beta_{\text{PNP}} = 1000$, we need an input current of only 10 μA to produce an output current of 10 mA.

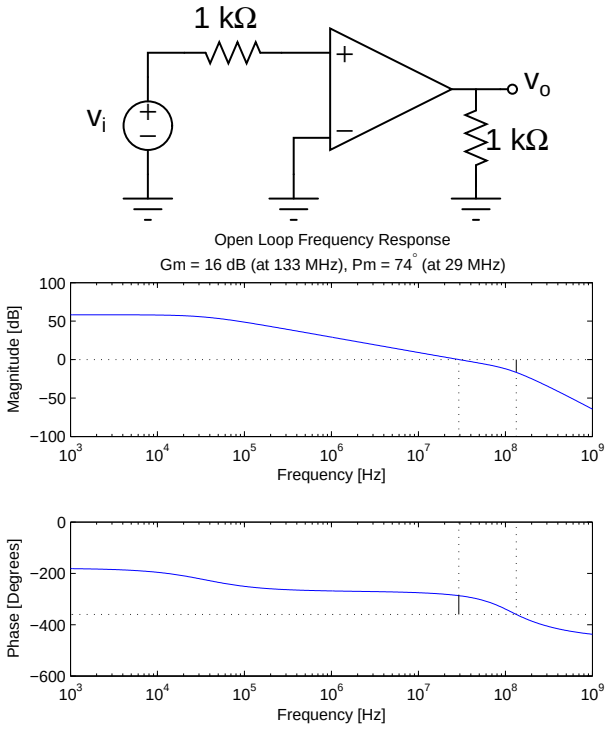
Power consumption

Our power consumption is made up of the 4 current sources driving our diamond buffers, and the current that is mirrored in the second half of the buffers and in the current mirror. If we drive the buffer with a current I, we have a total current draw of $7I$, so we set I to 1 mA, setting a power consumption of 210 mW, which is below our specification of 250 mW.

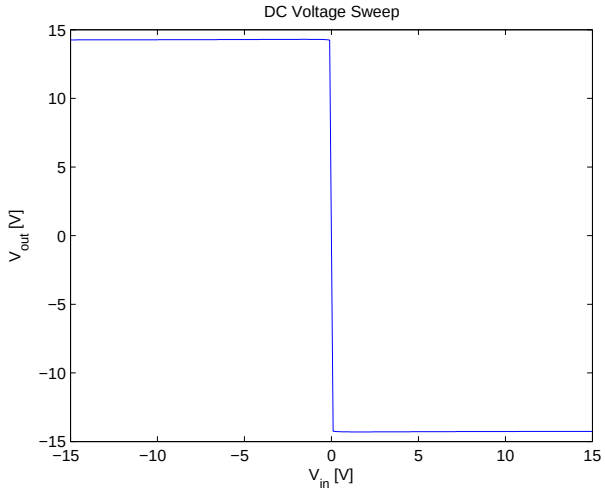
Spice Deck

```
*6.301 Design Project
*Transconductance Amplifier

.option post
.OP
**For AC Sweep
.AC DEC 100 1e3 1e9
.print ac vm(out) vp(out)
**For DC Sweep (output swing and current)
*.DC Vin -15 15 0.1
*.print dc v(out)

*Compensation test circuit
Vhigh vcc 0 DC 15
Vlow vee 0 DC -15
Vin 1 comm AC 1 0
R1 1 minus 1k
R2 out 0 1k
Voffs plus comm DC -12.7m
Vcm comm 0 DC 0
Xamp plus minus out vcc vee transamp

**Amplifier test - gain=11
*Vhigh vcc 0 DC 15
*Vlow vee 0 DC -15
*Vin plus 0 AC 1 0
*R1 out minus 1k
*R2 minus 0 100
*Xamp plus minus out vcc vee transamp

**Buffer test - measure common mode
*Vhigh vcc 0 DC 15
*Vlow vee 0 DC -15
*Vin plus 0 AC 1 0
*Rout out 0 1k
*Xamp plus out out vcc vee transamp

.SUBCKT transamp in.p in.m out vcc vee

*input diamond buffer
Q1 vee in.p 1 qpnp
Q2 3 1 in.m qnpn
Q3 vcc in.p 2 qnpn
Q4 5 2 in.m qpnp
I1 vcc 1 DC 1m
I2 2 vee DC 1m

*upper current mirror
Q5 3 4 vcc qpnp
Q6 4 4 vcc qpnp
Q7 7 3 4 qpnp

*lower current mirror
Q8 5 6 vee qnpn
Q9 6 6 vee qnpn
Q10 7 5 6 qnpn

*compensation capacitor
Cc 7 0 3pF

*output diamond buffer
Q11 vee 7 8 qpnp
Q12 vcc 8 out qnpn
Q13 vcc 7 9 qnpn
Q14 vee 9 out qpnp
I3 vcc 8 DC 1m
I4 9 vee DC 1m
.ENDS transamp

.MODEL qnpn npn
+ is=150fA bf=200
+ vaf=50 cje=10p
+ tf=750p cjc=1p

.MODEL qpnp pnp
+ is=150fA bf=50
+ vaf=25 cje=10p
+ tf=750p cjc=1p

.END
```

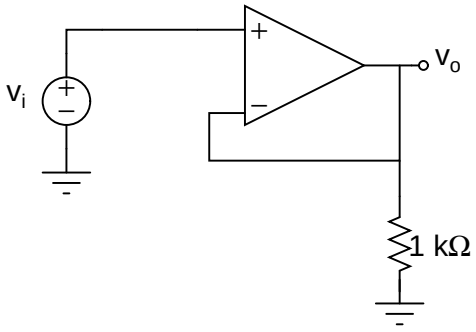
Simulation Results

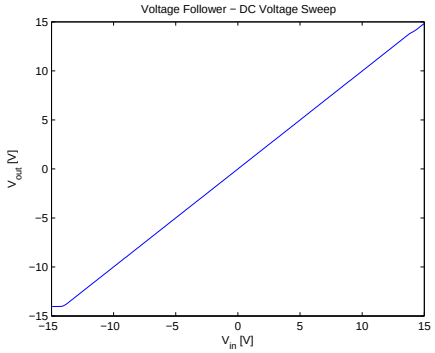


In the graph above, we see the results of simulating the amplifier running open loop. The low frequency gain 58 dB implies an open-loop transimpedance of 800 kΩ. To achieve the required phase margin, a 3 pF capacitor is connected to the high impedance node in the amplifier, raising the phase margin to 74°.

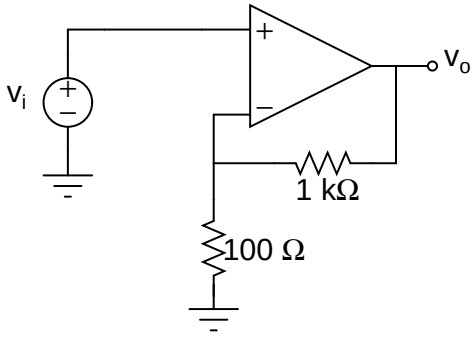


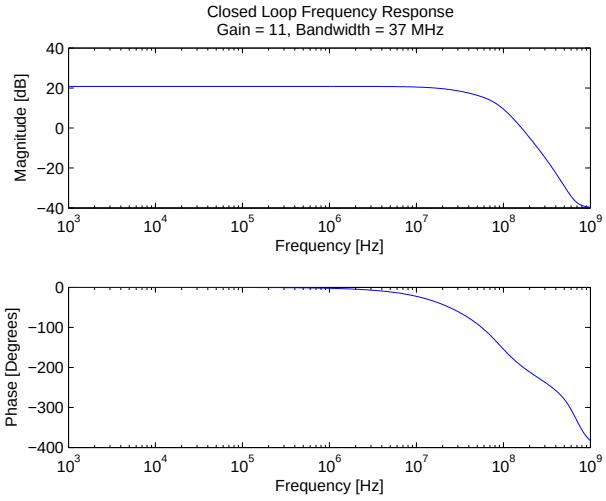
The DC sweep shows that the output swing is ±14.3 V, and that the output current is ±14.3 mA. By decreasing the load resistor to 10 Ω, we find that the maximum output current is ±250 mA.





By using a voltage buffer, we can show that the amplifier can handle common mode inputs sweeping almost from rail to rail, with a common mode range of ± 14.8 V.





The frequency response of the closed loop system shows that we achieve the expected gain of 11 from the amplifier, with a bandwidth of 37 MHz.