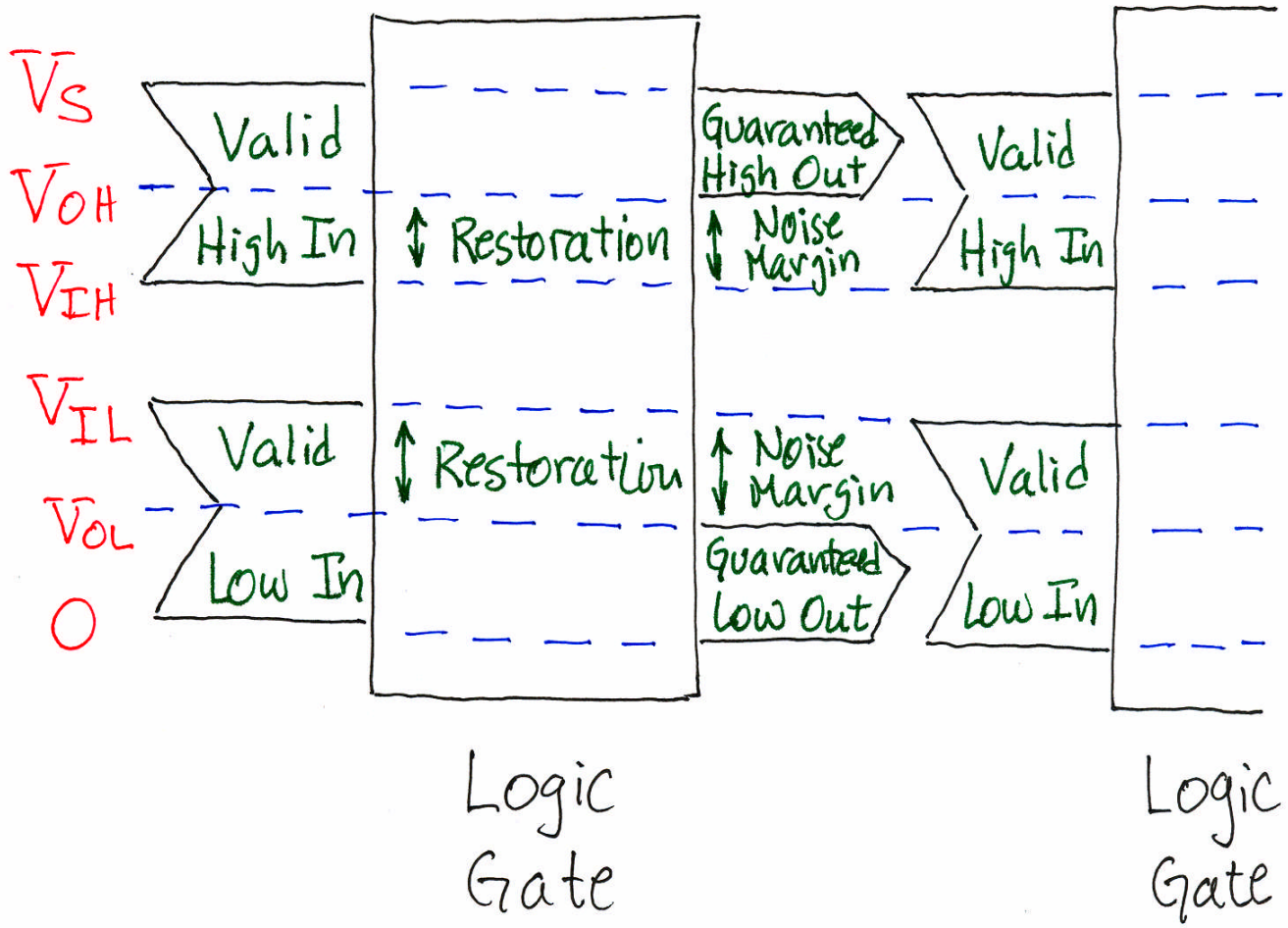
6.002 - Lecture 5

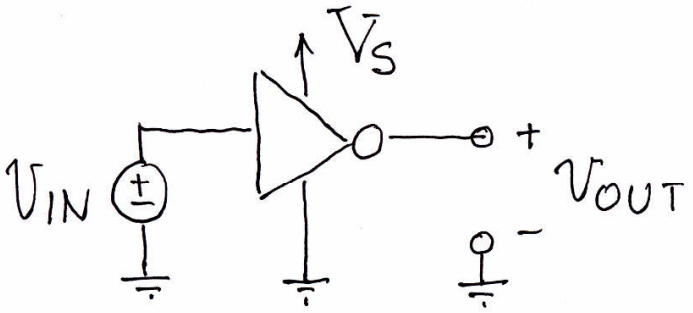
Digital Logic Gates

- Electrical Requirements
- Electronic Switch
- MOSFET Switch
- Gate Design & Operation

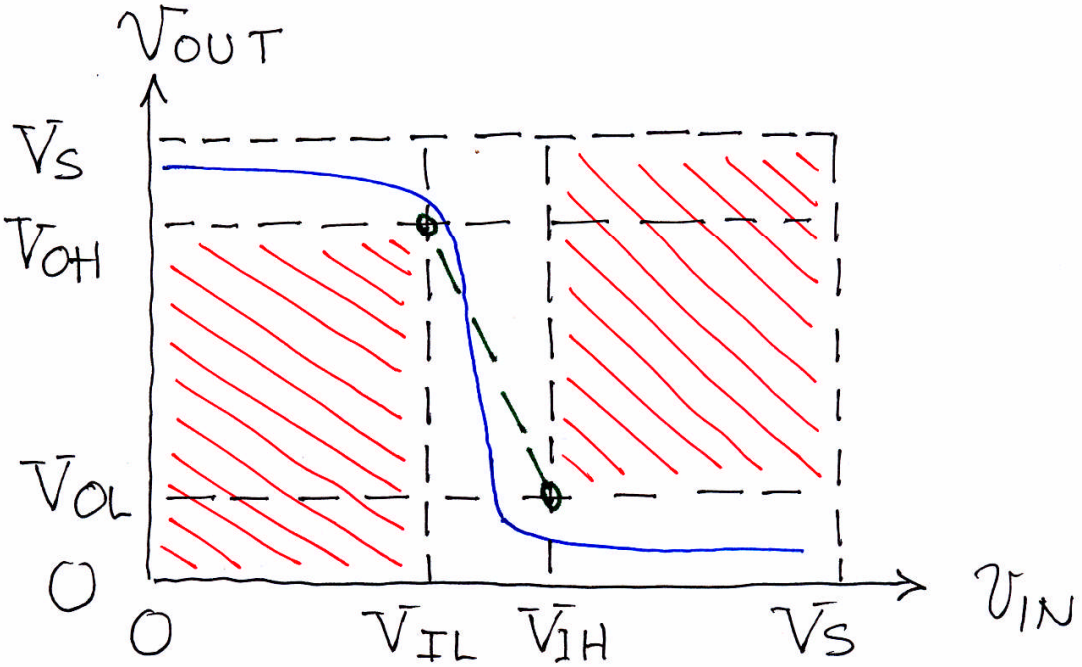
Static Discipline



Inverter Electrical Requirements



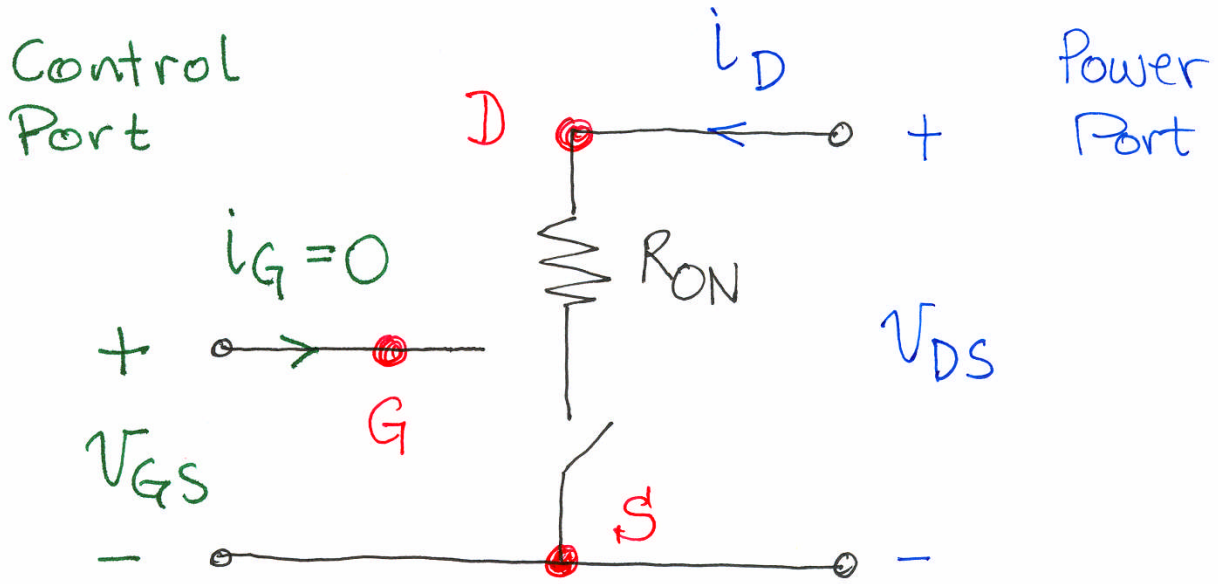
IN	OUT
L	H
H	L

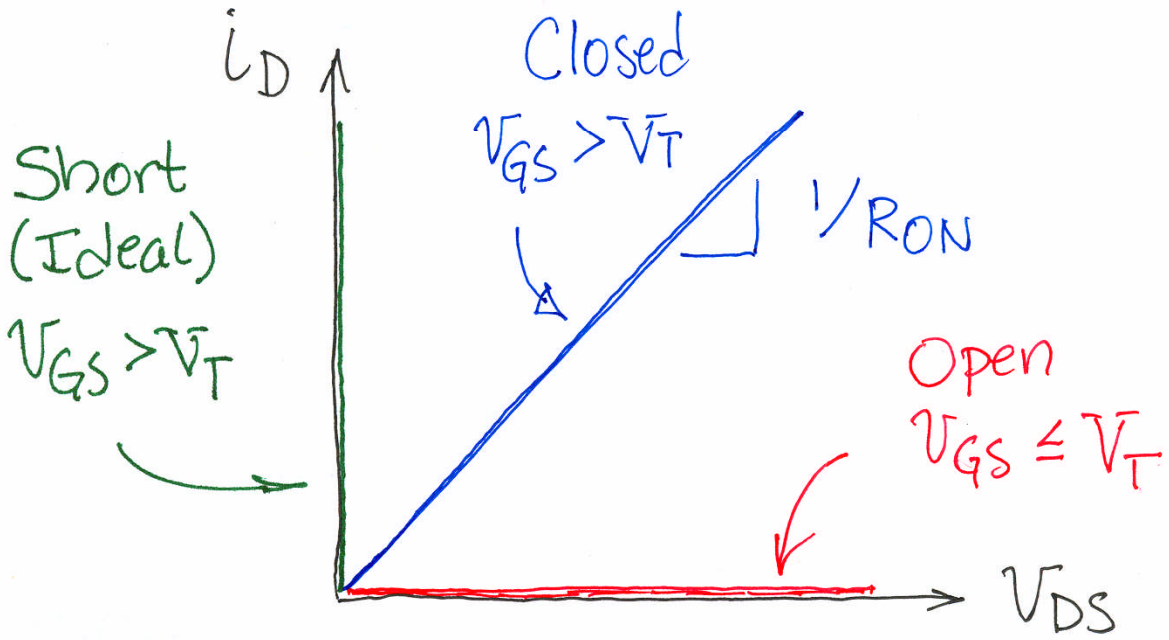


$$0 \leq V_{OL} < V_{IL} < V_{IH} < V_{OH} \leq V_S$$

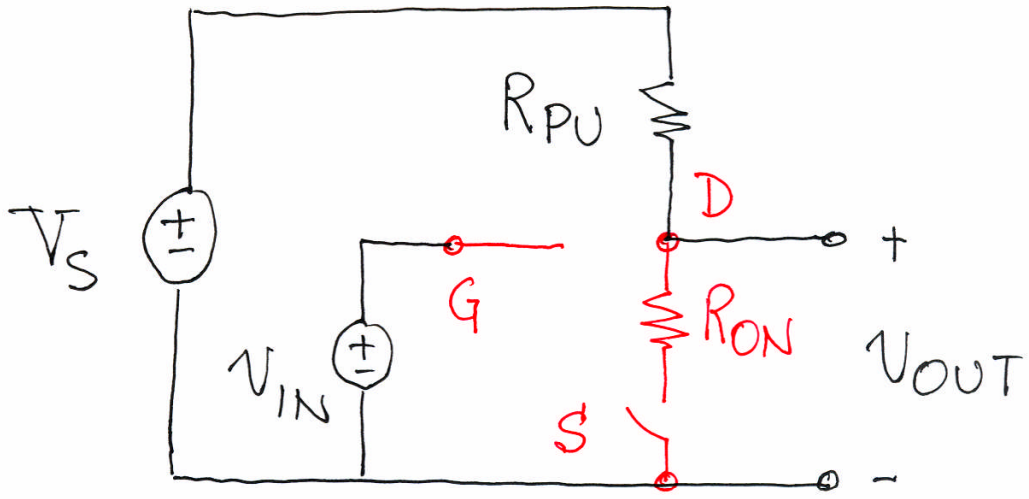
$$|\text{Slope}| \geq \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} > 1 \Rightarrow \text{Need new device!}$$

Three-Terminal Electronic Switch

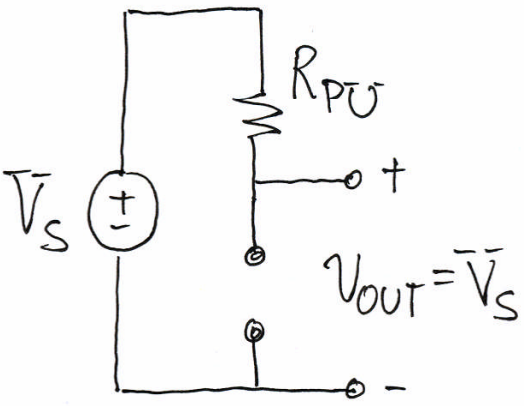




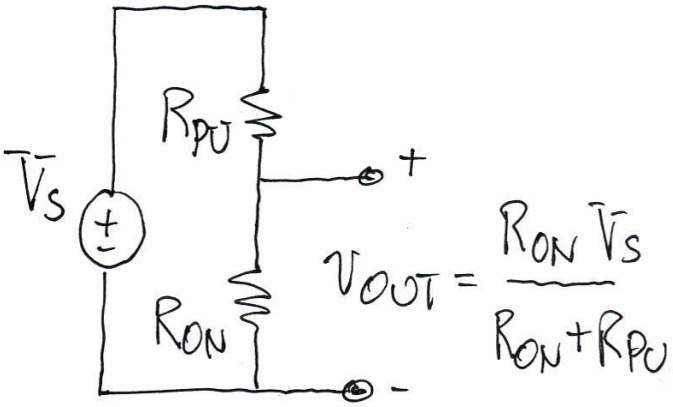
Inverter Design



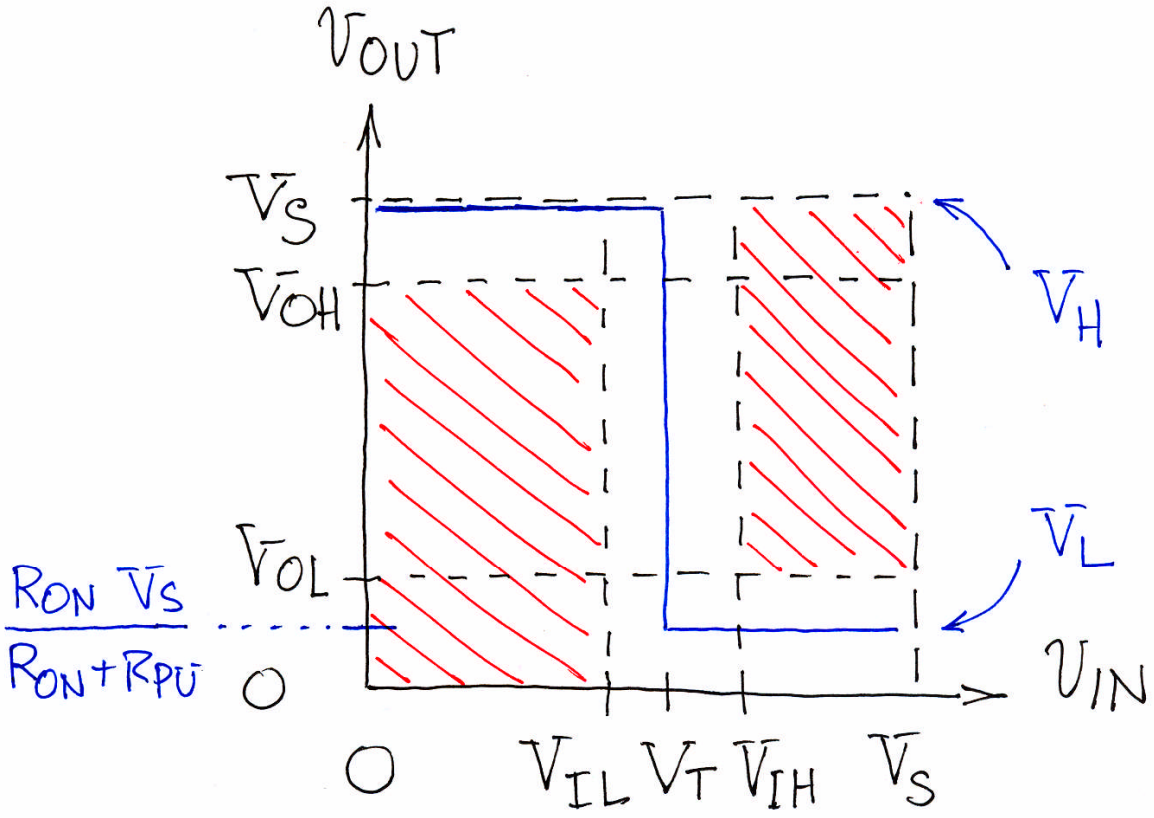
$V_{IN} \leq V_T$



$V_{IN} > V_T$



Inverter Analysis



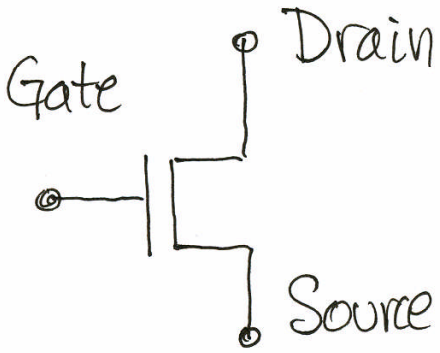
V_L Noise Margin Noise Margin V_H

$$0 \le \frac{R_{ON}\,V_S}{R_{ON}+R_{PU}} \le V_{OL} < V_{IL} < V_T < V_{IH} < V_{OH} \le V_S \le V_S$$

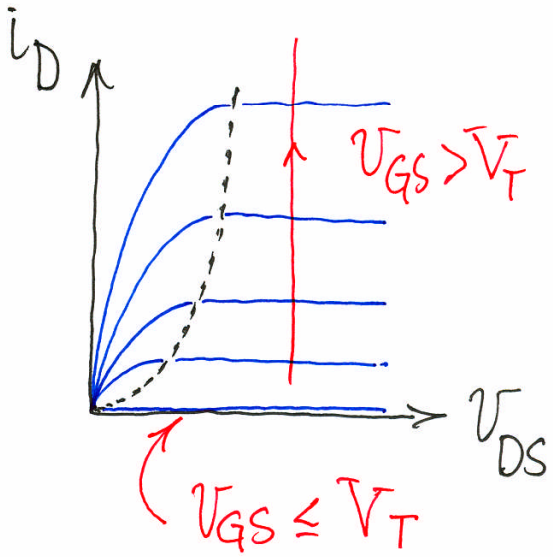
Free — Design — Design — Design — Free

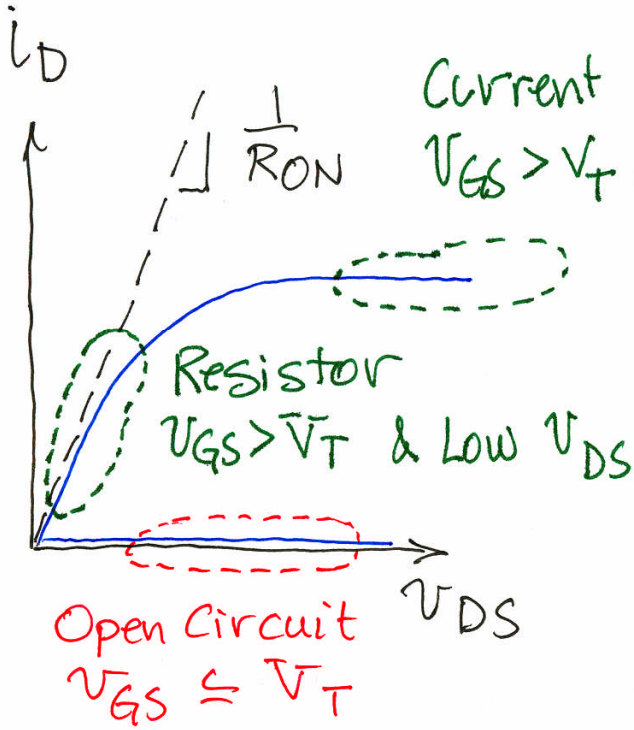
Static Discipline

n-Channel MOSFET As A Switch



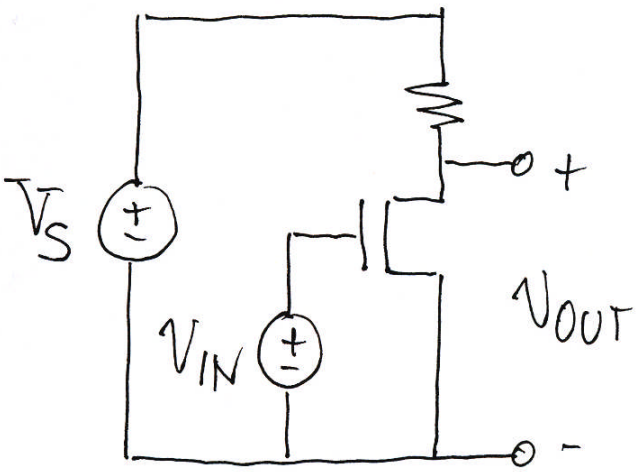
Defn $\Rightarrow$ $v_{DS} \geq 0$





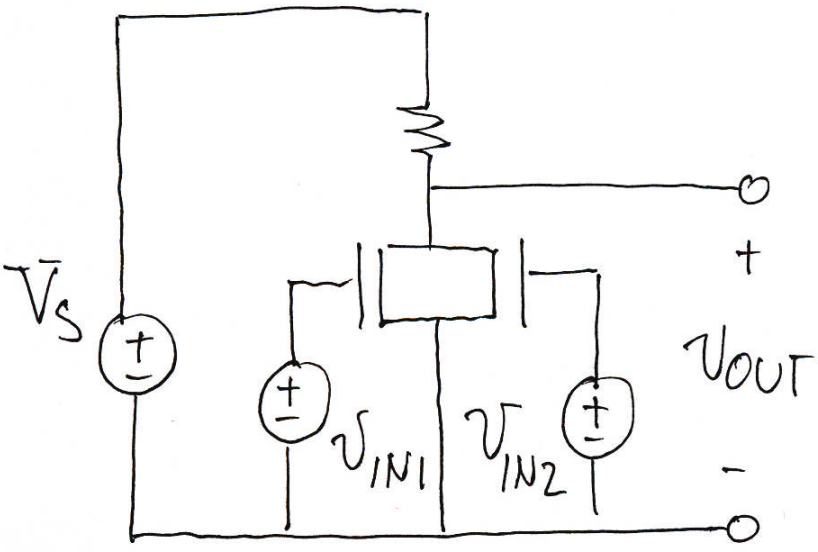
$\Rightarrow$ Switch-Resistor Model For Logic

Digital Gates (NMOS)



Inverter

IN	OUT
L	H
H	L



NOR Gate

IN1	IN2	OUT
L	L	H
L	H	L
H	L	L
H	H	L