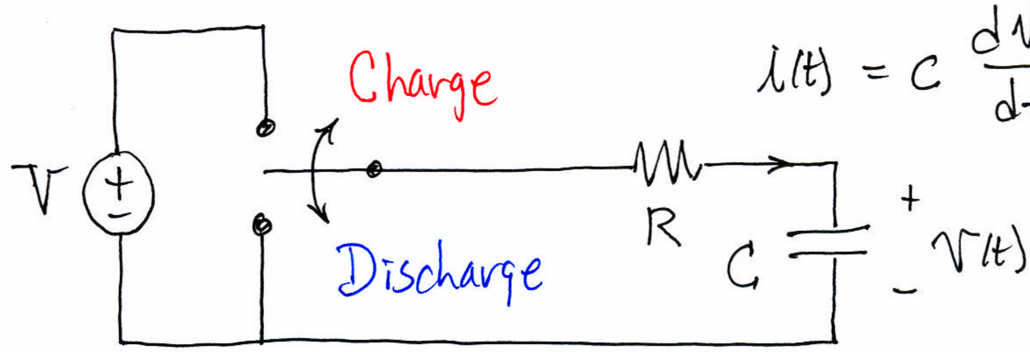
6.002 - Lecture 12

Power Dissipation In Logic

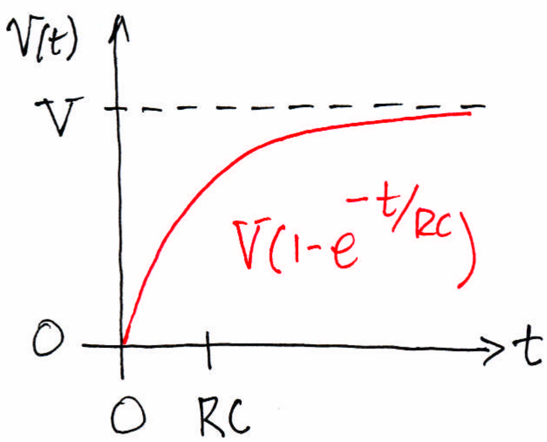
- Energy Accounting During RC Transients
- Power Dissipation In NMOS Logic
- CMOS Logic & Power Dissipation
- p-Channel MOSFET

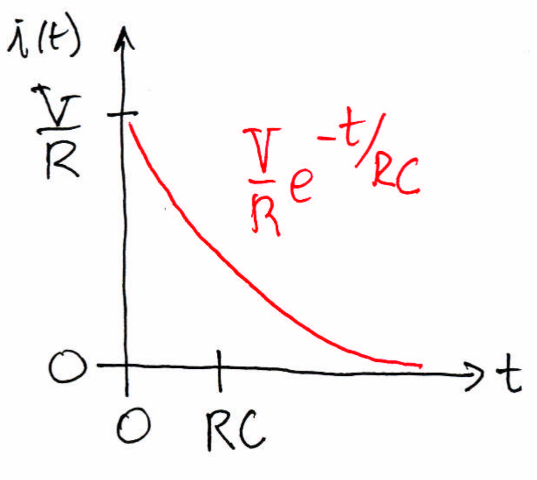
RC Transients



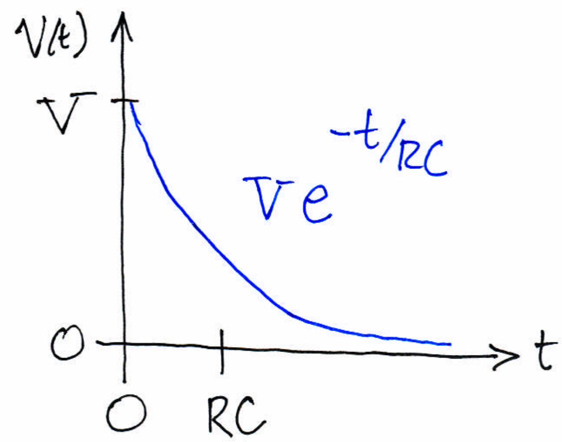
$$i(t) = C\,\frac{dv(t)}{dt}$$

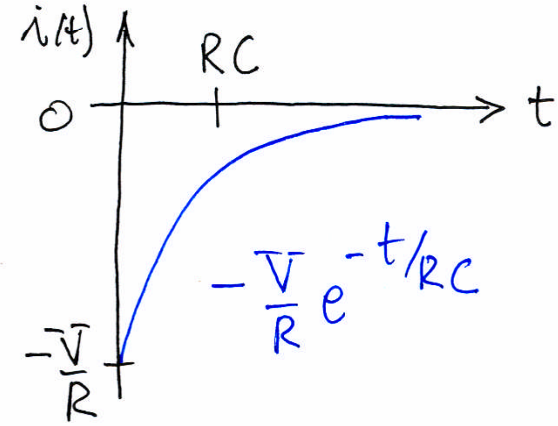
Charge At $t=0$





Discharge At $t=0$





Charge & Energy Conservation

$$\int_0^\infty i(t)\,dt = \int_0^\infty \pm \frac{V}{R} e^{-t/RC}\,dt = \pm CV$$

Charging: Source charges capacitor plates to $\pm CV$.

Discharging: Resistor discharges capacitor plates.

$$\int_0^\infty R\,i^2(t)\,dt = \int_0^\infty \frac{V^2}{R} e^{-\frac{2t}{RC}}\,dt = \frac{1}{2} C V^2$$

Charging Energy:

$CV \cdot V = CV^2$ from source

$\frac{1}{2} CV^2$ to capacitor (storage)

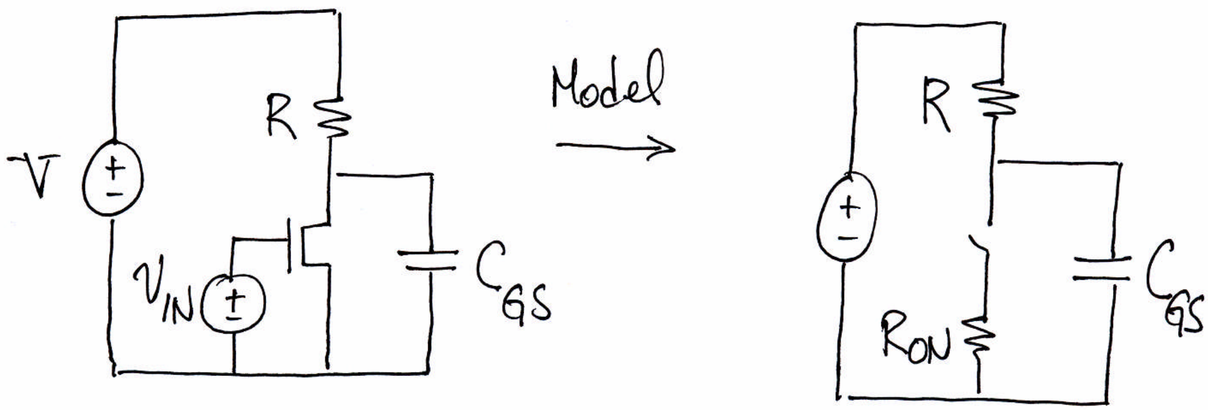
$\frac{1}{2} CV^2$ to resistor (loss)

Discharging Energy:

$\frac{1}{2} CV^2$ from capacitor

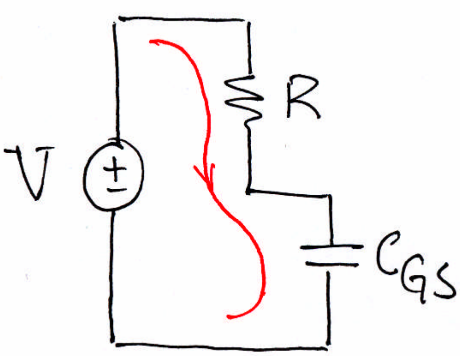
$\frac{1}{2} CV^2$ to resistor (loss)

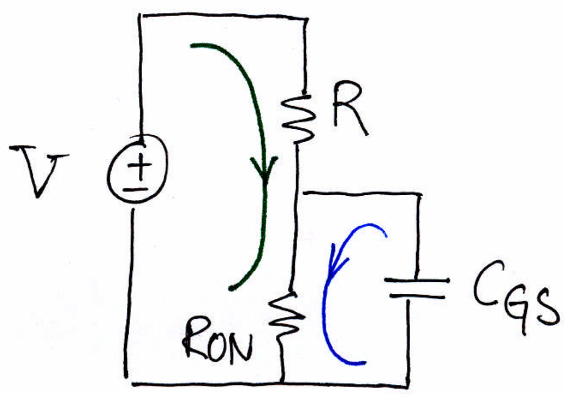
NMOS Logic Operation



v_{IN} = Low
MOSFET = Off

v_{IN} = High
MOSFET = On





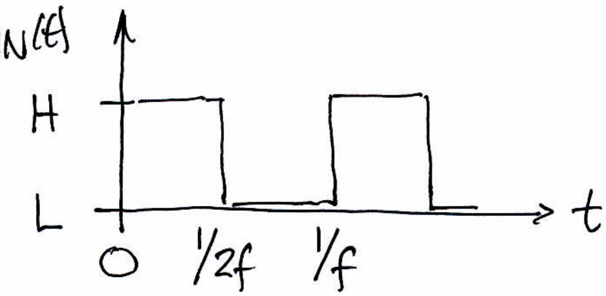
C_{GS} Charges

C_{GS} Discharges ($R_{ON} \ll R$)

R Conducts

NMOS Power Dissipation

Assume: * $V_{IN}(t)$



* $R_{ON} \ll R$ & $RC_{GS} \ll 1/2f$

V_{IN} H → L : Dissipation $= \frac{1}{2} C_{GS} V^2 f$

V_{IN} L → H : Dissipation $= \frac{1}{2} C_{GS} V^2 f + \frac{V^2}{2R}$

$$\text{Total Dissipation} = \underbrace{C_{GS} V^2 f}_{\text{Dynamic Loss}} + \underbrace{\frac{V^2}{2R}}_{\text{Static Loss}}$$

$$\frac{\text{Static Loss}}{\text{Dynamic Loss}} = \frac{1/2f}{RC_{GS}} \gg 1$$

Examples

Pentium III: $n \approx 10^7$ Gates (Excluding Memory)

$f \approx 10^9\,Hz$

$C \approx 10^{-14}\,F$ (Mostly Interconnect)

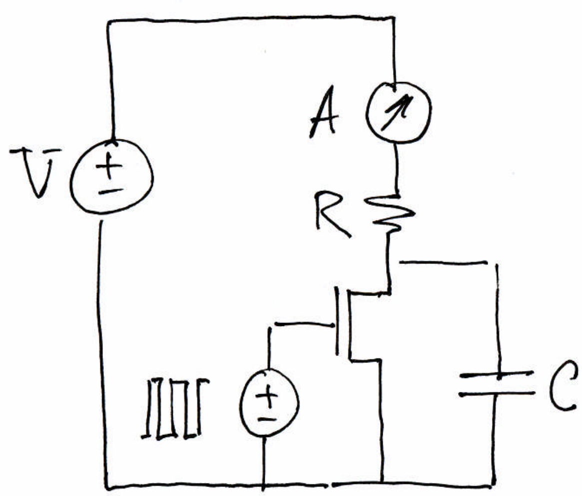
$V \approx 1.8\,V$

Too high since gates often idle $\longrightarrow$ $nCV^2f \approx 324\,W$!!

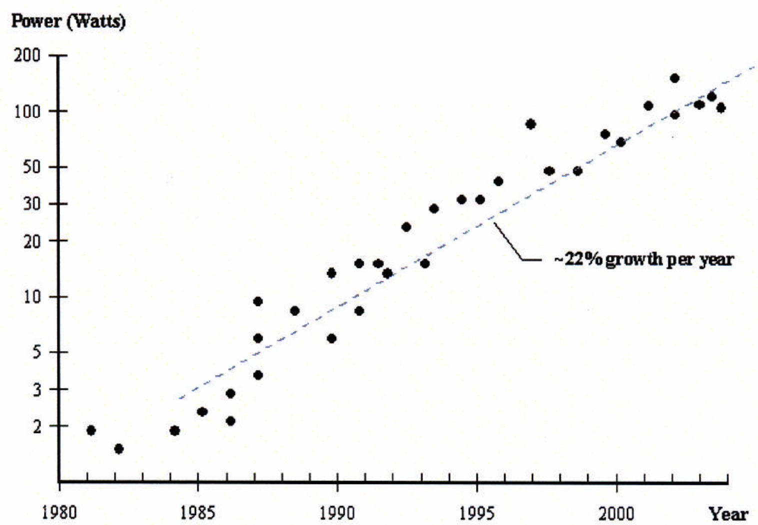
Demo:

$$\text{Avg Dissipation} = V\underbrace{\left[\frac{V}{2R} + CVf\right]}_{}$$

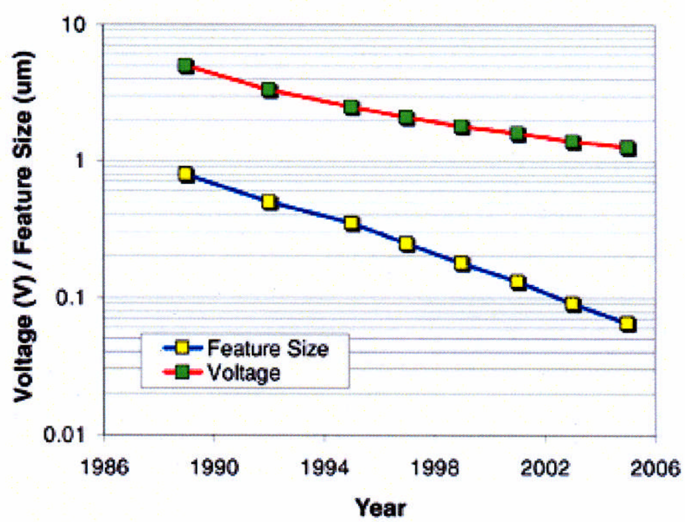
Average current measured by electromechanical ammeter.



Trends

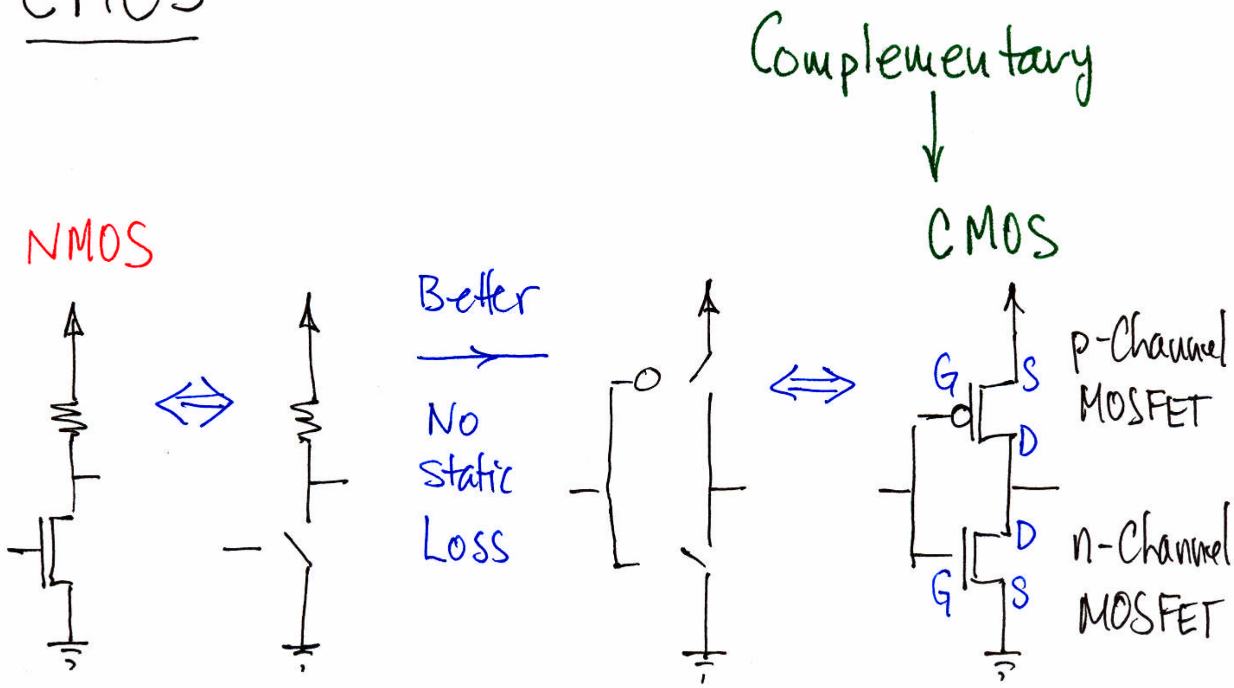


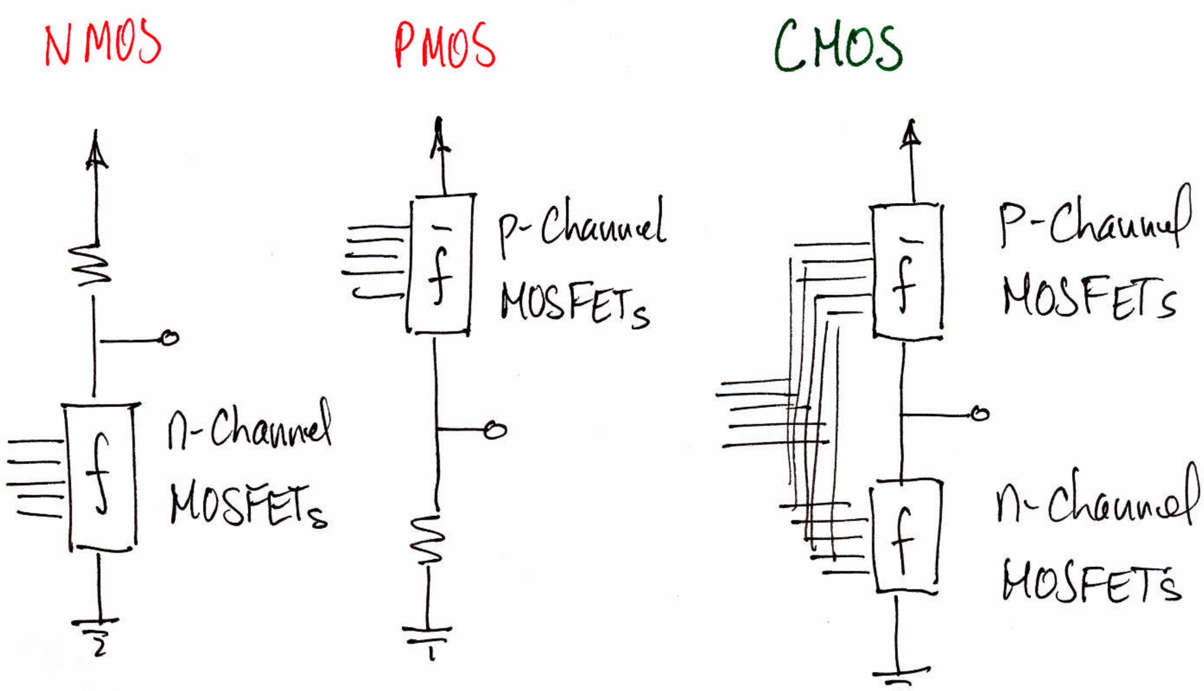
http://www.realworldtech.com/page.cfm?ArticleID=RWT062004172947&p=3



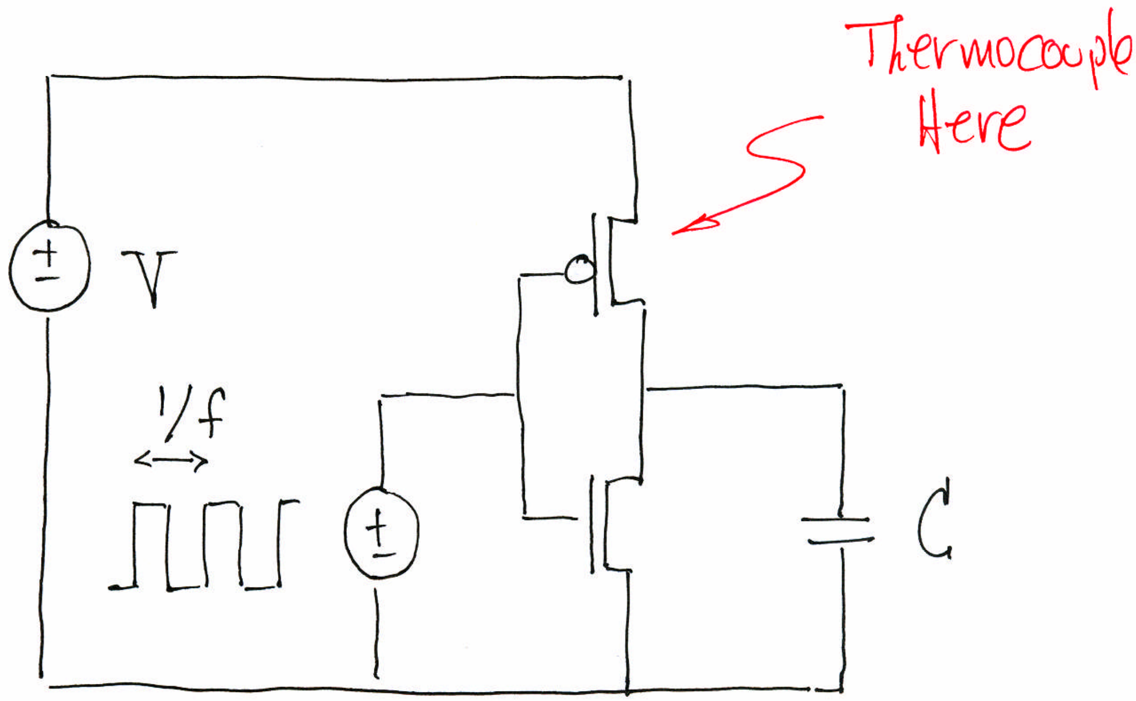
http://www.intel.com/technology/itj/2005/volume09issue04/art02_powerdelivery/figures/figure_3.gif

CMOS


Complementary
CMOS
NMOS
Better
No
Static
Loss
G
S
D
p-Channel
MOSFET
D
G
S
n-Channel
MOSFET

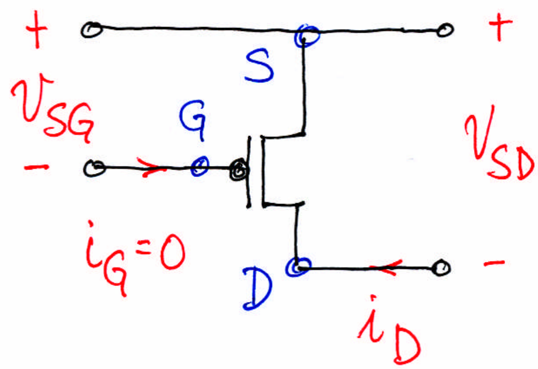

NMOS
n-Channel
MOSFETs
PMOS
p-Channel
MOSFETs
CMOS
P-Channel
MOSFETs
n-Channel
MOSFETs

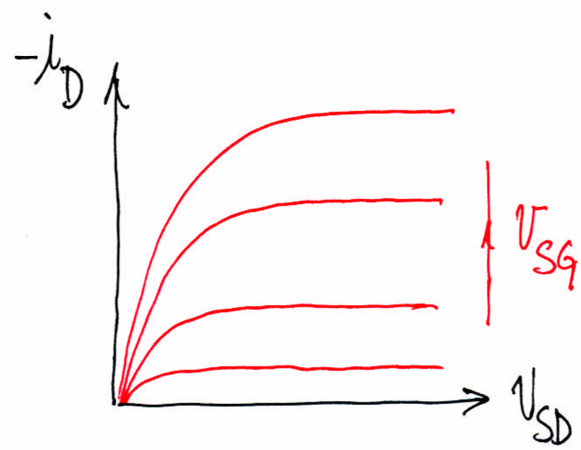
CMOS Dissipation Demo



$$\left.\begin{aligned} V &= 10\,V \\ C &= 1\,\mu F \\ f &= 1\,kHz \end{aligned}\right\} \text{Dissipation} = 0.1\,W$$

p-Channel MOSFET





p-Channel MOSFET permits CMOS logic, and more interesting amplifiers, for example.