Design of a Step-Down DC-DC Controller Integrated Circuit with Adaptive Dead-Time Control

by

Zhipeng Li

S.B. EE, M.I.T., 2009; S.B. Physics, M.I.T., 2009

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Abstract

A constant-frequency peak current mode synchronous step-down DC-DC controller integrated circuit has been designed with adaptive dead-time control. The adaptive dead-time control circuitry is implemented as digital delay-locked loop with digital counters as memory elements. In periodic steady state, the switch is controlled to turn on exactly when the body diode starts to conduct current. The conduction loss through MOSFET switch body diode is minimized. In spice simulation, this scheme increases the overall efficiency in low-voltage applications by up to 3%.

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Chapter 1

Introduction

1.1 Converter Efficiency

DC-DC converters are a category of electronic circuits designed to efficiently convert a source of direct current (DC) from one voltage level to another.

Many electronic devices, such as cellular phones and laptop computers, contain multiple circuit blocks; each circuit block may have its own supply voltage level requirement, different from the one supplied by the battery or an wall adapter. To increase efficiency and extend battery lifetime, we need efficient ways to convert DC voltage sources to different levels. Over the years, technology has moved from linear regulator to switching regulator, from asynchronous converter to synchronous converter. The architectural changes have led to significant increases in converter efficiency.

To push even further, every tiny bit of efficiency loss is targeted for reduction. In this thesis, we look at how to increase efficiency of a synchronous DC-DC converter further by adaptively controlling the dead-times.

The synchronous DC-DC converter has higher efficiency because its lower conduction loss compared to asynchronous converter with free-wheeling diodes. The synchronous converter includes a pair of power MOSFET switches. The switches are repeatedly switched on and off complementarily by a control signal from the controller. Dead-times are the short period of time when both gate drive signals are off. During this period of transition,
the body diode on one of the switches turns on, storing charge during the dead time and requiring a reverse recovery period. If the dead-time is too short or ever goes negative, huge amount of current could flow through the two power MOSFET from the input voltage source to ground. On the other hand, if the dead-time is too long, conduction loss is large. Because of the load variation and the internal timing delays presented both in the control IC and power MOSFETs due to process variation, in previous controllers, the dead times are often made large and fixed internally. The conduction through body diode during the dead time therefore presents a significant efficiency loss. On the proposed controller, an adaptive dead-time control block is integrated to minimize this conduction time through MOSFET switch body diode. We expect this effort to increase efficiency by up to 3% in the low-voltage applications.

1.2 Double Data Rate Memory Termination

One important low-voltage high-current application of a DC-DC converter is termination power supply for the Double Data Rate (DDR) Synchronous Dynamic Random Access Memory. We design this high-efficiency controller to be easily configurable for the DDR memory termination and for the general-purpose applications.

The DDR memory transfers data on both the rising and falling edges of the clock cycle, thus doubling the effective transfer rate of the Single Data Rates Synchronous Dynamic Random Access Memory (SDR SDRAM). However, a typical DDR memory system needs an additional power supply for its termination. The termination power supply \( V_{TT} \) must track the I/O Power supply \( V_{DD} \) with \( V_{TT} = V_{DD}/2 \) to ensure good signal quality. Further, the \( V_{TT} \) power supply must be able to both source and sink current.

There are two basic design schemes for DDR memory power supply termination [4] as shown in Fig. 1-1. In scheme 1, \( V_{TT} \) is directly generated from the \( V_{DD} \) rail. This scheme has been very popular in low power (< 10A) DDR applications. However, for high power application, this scheme has a few disadvantages. The \( V_{DD} \) supply must be able to provide enough current to power both \( V_{TT} \) circuit and the I/O current of the DDR memory. The input capacitors on the \( V_{DD} \) rail must be able to handle high RMS current and have
low impedance to minimize the $V_{DD}$ rail switching noise. These capacitors significantly increase board size and cost. Scheme 2 is preferred for high power applications, where $V_{TT}$ is generated from higher input voltage sources.

The controller designed in this thesis will satisfy these DDR requirements, and it can be used in both schemes. For Scheme 1, the Configuration Selection pin $CSEL$ is shorted to ground, the reference voltage pin $V_{REFIN}$ will be connected to the input source and the applied voltage gets divided by half internally as the error amplifier reference voltage, as shown in Fig. 1-2. For Scheme 2, $V_{REFIN}$ pin is connected to an external precision reference. For a general purpose DC-DC converter, $V_{REFOUT}$, where the internal Bandgap voltage is buffered, is connected to $V_{REFIN}$, and $CSEL$ is shorted to the 5V supply $INTVCC$, the output voltage can be programmed by a resistor divider, as shown in Fig. 1-3.
Figure 1-2: High efficiency DDR memory termination power supply with $V_{TT} = V_{DD}/2$
Figure 1-3: High efficiency DC-DC converter with high step-down conversion from 15V to 1.8V
1.3 Chip Specification

The proposed controller can be configured for DDR memory termination as well as a general-purpose DC-DC converter. An adaptive dead-time control (ADTC) scheme is implemented to reduce the conduction loss due to the power MOSFET body diode turn-on. The proposed controller integrated circuit (IC) will minimize the dead-times to typical 10 nanoseconds. In the application for DDR memory termination, it should be able to drive devices capable to sink and source up to 20 amperes of current. Additionally, its output should be able to go down to 0.3V. These specifications is summarized in Table 1.1. For a complete description of pin functions on this proposed integrated circuit, please refer to Appendix A.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Input Voltage</td>
<td>38</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Input Voltage</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Output Voltage</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Output Voltage</td>
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<td>V</td>
</tr>
<tr>
<td>Maximum Duty Ratio</td>
<td>In Dropout</td>
<td>%</td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>40% inductor current ripple</td>
<td>90</td>
</tr>
<tr>
<td>Maximum Current Sense Threshold ILIM=0V</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>ILIM=FLOAT</td>
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<td>mV</td>
</tr>
<tr>
<td>ILIM=INTVCC</td>
<td>60</td>
<td>mV</td>
</tr>
<tr>
<td>Minimum Current Sense Threshold ILIM=0V</td>
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<td>mV</td>
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<td>ILIM=FLOAT</td>
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<td>ILIM=INTVCC</td>
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<td>Lowest Switching Frequency</td>
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<tr>
<td>Highest Switching Frequency</td>
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<td>kHz</td>
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<tr>
<td>Top Gate Off to Bottom Gate On Delay $C_{LOAD}$=3300pF each driver</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Bottom Gate Off to Top Gate On Delay $C_{LOAD}$=3300pF each driver</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Dead Time Resolution</td>
<td>25°C</td>
<td>ns</td>
</tr>
</tbody>
</table>

Table 1.1: Specification of the proposed step-down controller

1.4 Thesis Overview

Chapter 2 covers the basics of the buck switching regulator operation, control and compensation. The adaptive dead-time control scheme is described in Chapter 3. The design of each sub-circuit of this proposed DC-DC controller is detailed in Chapter 4, and simula-
tion results are described in Chapter 5. Finally, the issues discussed in the thesis will be summarized and future works are suggested in Chapter 6.
Chapter 2

System Overview

This chapter describes the basic operation of the step-down switching regulator IC. It then outlines the control schemes used.

2.1 From Linear Regulator to Switching Regulator

The simplest way to convert a high and varying input DC voltage to a lower but constant output voltage is a dynamically controlled voltage divider circuit - a linear regulator. As shown in Fig. 2-1, by dynamically adjusting the upper resistor of the voltage divider, one can achieve a fixed constant voltage at output despite the disturbances on the input and load.

Figure 2-1: Linear regulator: concept and implementation
The drawback of the linear regulator is its low efficiency. Power is wasted on the variable resistor (the transistor Q1 in Fig2-1). The efficiency of a linear regulator, to the first order, is \( \frac{V_{OUT}}{V_{IN}} \). When \( V_{IN} \) and \( V_{OUT} \) are further apart, a linear regulator is a poor choice if efficiency is a concern.

A Step-down DC-DC Switching Regulator (also known as a buck converter), on the other hand, can be remarkably efficient [13]. In its most simplified form, it uses two switches and an inductor and a capacitor, as shown in Figure 2. Inductors and capacitors are energy storage elements. Current and voltage waveforms are always 90 degrees out of phase; hence, there is no power dissipated in them. For an ideal switch, it either carries current but has zero voltage across it, or has a positive voltage across it but carries zero current; in neither case does it dissipate power. Therefore, ideally the switching DC-DC converter is 100% efficient.

\begin{figure}
\centering
\includegraphics[width=0.5\textwidth]{Figure2-2.png}
\caption{Step-down DC-DC converter}
\end{figure}

The buck converter in Fig. 2-2 operates such that switches SW1 and SW2 are never on at the same time. In each cycle of duration \( T \), SW1 is on and SW2 is off during the first portion of the period of duration \( D \ast T \), and SW2 is on and SW1 is off in the second portion of the period of \( (1 - D) \ast T \). In periodic steady state, the average voltage across the inductor must be zero; otherwise, the inductor current would keep rising. Hence, in periodic steady state, we have \( DT \ast (V_{IN} - V_{OUT}) + (1 - D)T \ast (0 - V_{OUT}) = 0 \) which
reduces to $V_{OUT} = D \cdot V_{IN}$. By controlling the duty ratio of switching, the output voltage could be adjusted to almost any fixed value below the input voltage.

![Buck converter with free-wheeling diode](image)

**Figure 2-3: Buck converter with free-wheeling diode**

### 2.2 Synchronous Step-down Converter

In some applications, SW1 is implemented as a MOS switch and SW2 as a Schottky diode (Fig. 2-3). The freewheeling Schottky diode turns on, on its own, shortly after the switch turns off, as the voltage across it rises. On the other hand, a synchronous step-down controller, where both SW1 and SW2 are implemented as MOS switches, as shown in Fig. 2-4, could be more desirable to reduce the conduction loss of Schottky diode and increase efficiency.

![Synchronous buck converter](image)

**Figure 2-4: Synchronous buck converter**
For many specific applications, the customers prefer to have a stable switching frequency. Facing voltage variation of input source, this constant frequency controller keeps the same switching period, but adjusts the duty ratio of switches M1 and M2 to regulate the output. This switching frequency is determined by the internal programmable clock, and does not shift significantly with load, line, output, temperature, etc.

In this project, we design a general-purpose constant frequency peak current mode synchronous step-down controller IC, which improves on a previous design - the half version of LTC3855 - and implements an adaptive dead-time control scheme.

2.3 Control Scheme

The most important function of a DC-DC converter is to properly regulate the output voltage over a range of input and load conditions. Hence, it is essential to model the control loop dynamics accurately so that its characteristics can be well understood and the control loop can be appropriately compensated to achieve stability and good transient response for all load ranges and any possible load steps.

2.3.1 Voltage Mode Control

In the voltage mode control, the duty cycle is directly determined by the output voltage feedback, as indicated in Fig.2-5.

Two major energy storage elements, output capacitor and power inductor, usually give a voltage mode converter a conjugate pair of high-frequency poles, making it hard to compensate to achieve loop stability.

2.3.2 Current Mode Control

In peak current mode control, the duty ratio is directly determined by the peak inductor current, and the peak inductor current is set by the output of error amplifier. In implementation, at the start of each clock cycle, the M1 Switch is turned on and the inductor current rises; once the inductor current reaches a threshold value [11], the M1 switch is turned off.
when a current mode control scheme is used, the current feedback is required and M2 is turned on. By regulating the inductor current, the inductor sees no AC components and is effectively removed from loop dynamics for all frequencies below the switching frequency. Instead of a pair of complex conjugate poles, the current mode regulator has two real-axis poles that make the loop compensation a much easier task. In fact, for all frequencies way below the switching frequency, we only see an abstract transconductance, $G_{m2}$ in Fig.2-6, which is the conversion ratio from the error amplifier output voltage to the inductor current.

As shown in Fig.2-6, the DC gain is determined mainly by the transconductance of error amplifier (EA), denoted as $G_{m1}$, and the output resistance of EA, denoted as $R_O$. The only
relevant low-frequency pole is determined by the output capacitor $C_{OUT}$ and load resistor $R_{LOAD}$[16][19].

For example, if this regulator is configured to switched at 500kHz for DDR application from 2.4V input to provide 20A at 1.2V output, the load resistance is $R_{LOAD} = 60\,\text{m\Omega}$. If we use an output capacitor of $C_{OUT} = 1500\,\mu\text{F}$, this low-frequency pole is at

$$P_2 = \frac{1}{2\pi R_{LOAD}C_{OUT}} = 1.8\text{kHz}.$$  

Unless the slope compensation is unreasonably large, the high-frequency pole stays way higher than the switch frequency and we do not need to consider it. Hence, without compensation, the loop dynamics will have a crossover frequency close to or higher than the switching frequency.

![Figure 2-7: Block-level schematics of an open-loop current-mode regulator](image)

![Figure 2-8: Simplified block diagram of an compensated current-mode regulator](image)

We compensate the current-mode switching regulator by placing an passive compensation network at the error amplifier output, as shown in Fig.2-7. The modified block diagram
for this compensated regulator is shown in Fig.2-8, compared to the uncompensated version in Fig.2-6. In Fig.2-9, an asymptotical bode plot for the compensated regulator is shown. 

Adding a dominant pole $P_1$ lowers the crossover frequency. Then with two poles $P_1$ and $P_2$ both before crossover, a zero $Z_1$ is added as well to increase the phase margin. Physically this compensation is easily achieved using a compensation capacitor $C_{C1}$ and a resistor $R_{C1}$ in series on the error amplifier output $ITH$, illustrated in Fig.2-7. It is also recommended to add a shunt capacitor $C_{C2}$ to filter as much high-frequency contents. However, the shunt capacitor should be at least ten times larger than the compensation capacitor so that its associated pole $P_3$ is far above the crossover frequency to have minimal effects on loop dynamics.

![Asymptotic bode plot of loop dynamics.](image)

The loop response is given as,

$$L(s) = \frac{G_{m1}R_O(1 + sC_{C1}R_1)}{1 + s(R_OC_{C1} + R_OC_{C2} + R_{C1}C_{C1}) + s^2R_OR_{C1}C_{C1}C_{C2}} \left( \frac{G_{m2}R_{LOAD}}{1 + sR_{LOAD}C_{OUT}} \right)$$

$$\approx G_{m1}R_Om2R_{LOAD} \frac{1}{(1 + sR_OC_{C1})(1 + sR_{C1}C_{C2})} \frac{1}{1 + sR_{LOAD}C_{OUT}}.$$
With the above approximation which is valid if $C_1 \ll C_2$ and $R_1 \ll R_O$, it is easy to see where the additional poles and zero are:

$$
P_1 = \frac{1}{2\pi R_O C_1},
Z_1 = \frac{1}{2\pi C_1 R_C},
P_3 = \frac{1}{2\pi R_C C_2}.
$$

For a numerical example on the compensation of the proposed converter, we could simulate the frequency response on the regulator described in Fig.2-7. For this regulator that has an error amplifier with $G_{m1}=2$ mΩ and $R_O=2$ MΩ and a regulated current mode power stage of 43S and a load of $R_{LOAD}=60$ mΩ with $C_{OUT}=1500 \mu$F, without compensation, the crossover frequency is 1.26MHz with $-8.6^\circ$ phase margin, higher than the switching frequency and unstable. With the compensation network at $ITH$ to add a dominant pole, a zero, and a filter pole, respectively at

$$
p_1 = \frac{1}{2\pi R_O C_1} = 40\text{Hz} ,
Z_1 = \frac{1}{2\pi R_C C_1} = 13.6\text{kHz} ,
P_3 = \frac{1}{2\pi R_C C_2} = 200\text{kHz} ,
$$

the crossover frequency is lowered to 47.8KHz (more than one order of magnitude below the nominal switching frequency 500kHz) with 62.8$^\circ$ phase margin, as shown in Fig.2-10.

This stability does not vary much with load. Assuming the load current is smaller and load resistance is larger, the DC gain is larger but the original low-frequency pole is correspondingly larger. With the compensation network unchanged, the cross-over frequency and phase margin does not change.

It must be mentioned that the described model above is a very simple model. It only describes the system well for frequencies well below the switching frequency. It also does not model sub-harmonic oscillations. For simplicity, it has completely ignored the effect of slope compensation [16].
Figure 2-10: Spice simulated Bode plots of the uncompensated (top) and compensated (bottom) systems.
Chapter 3

Dead Time Control

3.1 Dead-Time Control

The power switches of a synchronous converter, M1 and M2 in Fig.3-1, are repeatedly switched on and off complementarily by a control signal from the controller. As mentioned in Chapter 1, dead-times are the short period of time when both gate drive signals are off. During this period of transition, device output capacitances charge and discharge until either the other switch turns on or the body diode on one of the switches turns on. When the body diode conducts, it stores charge during the dead time, requiring a reverse recovery period.

Figure 3-1: Synchronous buck converter
Because of the load variation and the internal timing delay due to process variation, non-zero dead-time is generally used. If the dead-time is too short or ever goes negative, huge amount of current could flow through the two switches from the input voltage source to ground. This phenomenon is called "shoot-through". On the other hand, if the dead-time is too long, conduction loss on body diode is large. There should be an optimal dead-time. This optimal dead-time varies with load current and external components. Different external switches have different gating delays and output capacitances, and require different dead time to achieve the highest efficiency.

In most previous commercial controllers, the dead time is fixed internally. We implement a smart dead-time control scheme by sensing the switching node SW and giving precisely controlled timing for the power switches. Then our controller is adaptive to achieve higher efficiency.

3.2 Estimation of Efficiency Improvement

With simple calculation on the body diode power dissipation, we could estimate the possible efficiency improvement with adaptive dead time control. For an application in which the buck regulator outputs a load current of $I_{LOAD}$ at a regulator output voltage of $V_{OUT}$, if the dead time control scheme successfully reduces the body diode conduction time by $\Delta T$ for each edge, the energy saving in each clock period is $(V_D - I_{LOAD} R_{DS(ON)}) I_{LOAD} \Delta T$ per edge, where $V_D$ is the forward voltage of the switch’s body diode and $R_{DS(ON)}$ is the on-resistance of the switch. Assuming the efficiency is close to 1, the efficiency improvement is approximately,

$$\Delta eff \approx \frac{2(V_D - I_{LOAD} R_{DS(ON)}) I_{LOAD} \Delta T}{I_{LOAD} V_{OUT}} = \frac{2(V_D - I_{LOAD} R_{DS(ON)}) \Delta T}{V_{OUT}} (3.1)$$

A few simple examples will give us a better intuition of how large this efficiency improvement is.

1. For a regulator to output 5A at 0.6V switched at 700kHz with 5mΩ switches and a 0.7V body diode drop, reducing dead time by 20ns would result in an efficiency
improvement of $2*(0.7V - 5A*5m\Omega *20ns) / (0.6V *(1/700kHz)) = 3.15\%$

2. For a regulator to output 20A at 1.25V switched at 500kHz, reducing dead time by 15ns would result in an efficiency improvement of $2*(0.7V - 20A*5m\Omega *15ns) / (1.25V * (1/500kHz)) = 0.72\%$

3. For a regulator to output 10A at 1.8V switched at 500kHz, reducing dead time by 15ns would result in an efficiency improvement of $2*(0.7V - 20A*5m\Omega *15ns) / (1.8V * (1/500kHz)) = 0.50\%$

This efficiency improvement becomes more significant as the output voltage goes lower and switching frequency goes higher.

With the continuous demand for smaller external components, the controller needs to switch at higher and higher frequency. Because the digital power consumption is a quadratic function of supply voltage, the power supply voltage of microprocessor and memory goes lower and lower to save power. These two trends of converter technology, higher switching frequency and lower output voltage, make an even more promising perspective of efficiency improvement by adaptive dead time control.

### 3.3 Prior Art and Other Control Schemes

To achieve best efficiency and avoid shoot-through, the controller needs to adjust the dead-times to the optimum. The optimum dead-time varies with the process variation in controller integrated circuit, load, duty cycle, switch characteristics, and etc. If the dead-time is too long, there will be additional conduction loss due to conduction and reverse recovery of the body diodes of the switches. If the dead-time is too short, there will possibly result in simultaneous conduction of both switches, causing efficiency loss and possibly device failure.

In most commercially-available DC-DC converter, fixed delays are used to avoid shoot-through, as shown in Fig.3-2. Under this scheme, the bottom gate will turn on only after the top gate turns off, and vice versa. This is a very safe option. However, because of the logic and driver delays, this never creates the optimal solution, in the presence of operating point changes and process variations. This simplest approach leads to low efficiency.
Another method of dead-time control to ensure no shoot-through involves the sensing of the $SW$ node. For the $TG$ low and $BG$ high edge, Texas Instrument’s TPS2833 achieves no shoot-through by sensing the $SW$ node [12]. If $SW$ is down, that means the top switch is fully off. When $SW$ is down, the bottom driver then starts to charge up to turn on the bottom switch. Because of the delay of bottom driver, the actual dead-time could be much longer than is optimal.

Alternatively, some controllers allow dead-time to be programmed externally as in LTC3770 [7]. This is a good option for the user, once a specific application is well characterized, at the cost of an additional pin.

Programmable dead-time is particularly convenient for controllers with a digital pulse-width modulator (PWM). In fact, externally-programmed dead-time control, with resolution down to 1.25 ns, has been reported in digitally-controlled switching DC-DC converters [22], [9]. If a DC-DC converter is digitally controlled entirely and now it allows programmability of dead-time, it is easy to go a step further and implement various efficient algorithms to optimize the dead-time. People have been using the Maximum Efficiency Point Tracking (MEPT) or similar schemes to select the optimal dead-time [2], [1], [17], [18] in digitally-controlled switching regulators. However, this MEPT scheme requires sensing and computation of the input and output powers, which requires significant amount of additional digital logic. It has been pointed out that for a given set of load and output regulation
voltage conditions, the optimum dead-times that lead to highest efficiency result in the minimum switching duty cycle command $D$ [21]. Hence, instead of online maximization of efficiency, online minimization of duty-cycle command could be used instead. Because duty cycle command $D$ is already available in the digital controller, no additional sensing is required. This approach requires relatively small additional digital logic resources and requires no modifications of any gate-drive circuitry [21].

Despite significant effort, fully digital control remains infeasible for our mainstream analog controller IC built on older technologies with minimum gate-length being 0.6 um or larger. In this design, we keep the analog current-mode control.

There have been attempts to use a delay lock loop to align the two gate drive signals in the analog controller, $TG$ and $BG$, to ensure one switch turns on exactly when the other switch turns off. One complication with this prior design is the turn-off delay time of MOSFET switch. When external $TG$ falls below the threshold voltage, the switch might not be off yet. The internal gate voltage may still be above threshold (with the difference owing to distributed gate resistance). Moreover, it takes a few hundred picoseconds to a few nanoseconds to dispel the channel charges. The gate drive signals are not the true signatures of switch-on and switch-off.

On the other hand, the $SW$ node signal gives the true signature of body-diode conduction which directly determines efficiency loss. The longer the body diode turns on, the large the efficiency loss is incurred. By the looking at $SW$, we know exactly when the body-diode of the switch starts to conduct. A delay-locked loop can be used to align two edges of switch-on and switch-off signatures. Charge pump has been a popular method for this delay lock loop [3], [15], [20], but it requires an additional analog servo loop to maintain. Under unforeseen conditions, the loop might go unstable and result in shoot-through or worse, losing regulation. For dead-time control where resolution finer than a nanosecond is not meaningful, digital discretization can be used. Hence, in this design, we use a digital delay-locked loop to achieve precise gate-drive timing, and dead-time resolution is defined by the delay cells used.

In conclusion, because mainstream analog controller ICs are often built on older tech-
nologies with minimum gate-length being 0.6 um or larger, we stay away from full digital control and keep the analog current-mode control. Therefore, it makes sense for us to use the delay-locked loop approach [3], [15], [20] instead of online minimization of duty cycle [21]. However, as done in the digitally-controlled converter with dead-time programmability[22], [9], we use digital counter instead of charge pump as the memory element in the delay-locked loop.

3.4 Control Scheme with Digital Delay-Locked Loop

To achieve the optimum dead-time, the controller has to be able to adjust the dead-time dynamically. The controller has to extract the dead-time information from electrical signals. The best electrical signals to sense are the top MOSFET gate drive signal, $TG$, the bottom MOSFET gate drive signal, $BG$, and the switch node, $SW$. These three signals encompass all the information about the external MOSFET gate voltages, threshold voltages, controller driver strengths, etc. The $SW$ tells the "effective" dead time. If $SW$ is ever one diode voltage above input voltage or one diode voltage below ground, it means the body diode of one of the power switches has turned on; hence, an undesirable conduction loss results. By sensing these three signals, the controller could extract the dead-times, and adjust them accordingly using digital logic circuitry.

Unlike the scheme in Fig.3-2, we use variable delays. For the $TG$ low and $BG$ high edge, the overall system is shown in Fig. 3-3.

To controlling $Delay2$ in Fig. 3-3, we use a digital delay-lock loop which closely resembles an analog phase-lock loop. As shown in Fig. 3-4, $SW$ and $BG$ are sensed through two comparators to produce two edges $SB_{SW}$ and $SB_{BG}$. These two edges race each other to make the counter count up or down on the next clock edge. The state of counter determines the variable delay. In the steady state, $SB_{SW}$ and $SB_{BG}$ are very close to each other in each clock cycle, and they alternate to be first.

The algorithm to optimize dead-time on the $TG$ low and $BG$ high edge, is the following,

1. $SW$ and $BG$ are sensed through two comparators. The first comparator outputs high
Figure 3-3: TG-off to BG-on edge

Figure 3-4: The delay-lock loop to align SB\_SW and SB\_BG signals (parts of this circuitry are shown later in Chapter 4 in more details)
if the SW voltage is higher than input voltage by a fixed threshold voltage or blow
the ground by a fixed threshold voltage. The second comparator outputs high if the
BG is higher than a MOSFET threshold voltage above ground.

2. Two outputs of comparators are racing each other to be latched and then to set the
4-bit counter. The counter memorizes the state of the last switching cycle. If the
BG comparator output is ahead of the SW comparator output, it means that the
dead-time is too little; the counter will count up by one LSB on the next cycle. If
the SW comparator output comes first, it means that the dead-time is too much; the
counter will counter down by one LSB on the next cycle.

3. In steady state, the circuitry will always find one optimal point in the counter and
count up and down alternatively around it.

For the BG low and TG high edge, the overall system is shown in Fig. 3-5. A similar
circuit can be constructed, using sensed SW and TG signals as shown in Fig. 3-6. The
algorithm to control Delay3 in Fig. 3-5 is the following,

1. SW and TG are sensed through two comparators. The first comparator outputs high
if the SW voltage is higher than the input voltage by a fixed threshold voltage or
blow the ground by a fixed threshold voltage. The second comparator outputs high
if the TG is higher than a MOSFET threshold voltage above SW.

2. Two outputs of comparators are racing each other to be latched and then to set the
4-bit counter. The counter memorizes the state of the last switching cycle. If the
TG comparator output is ahead of the SW comparator output, it means that the
dead-time is too little; the counter will count up by one LSB on the next cycle. If
the SW comparator output comes first, it means that the dead-time is too much; the
counter will counter down by one LSB on the next cycle.

3. In steady state, the circuitry will always find one optimal point in the counter and
count up and down alternatively around it.
Figure 3-5: BG-off to TG-on edge

Figure 3-6: The delay-lock loop to align SB_SW and SB_TG signals (parts of this circuitry are shown later in Chapter 4 in more details)
The overall system, considered both edges, is shown in Fig. 3-7. Additional logic is included to minimize interference and have separate controls on Delay2 and Delay3.
Figure 3-7: Both edges
Chapter 4

Chip Design

4.1 Overview

This thesis describes a complete integrated circuit design in a 0.6um BiCMOS process. Accurate evaluation of the efficiency improvement by adaptive dead-time control is only possible through a design fabricated in silicon and eventually measured on well-designed printed circuit board.

This chapter described requirements and trade-offs of each sub-circuit. The LTC3855 was used as a basis for the chip design in this thesis. A block diagram of the designed 24-pin chip is shown in Fig.4-1. For a complete description of pin functions, please refer to Appendix A.

4.2 Internal Supply, Biasing, and Clock

The bandgap reference generates the 1.22V bandgap voltage, and provides a 0.6V reference with resistor dividers for the trimmed buffer to give a precise reference of 0.6V±0.75% at \( V_{REFOUT} \) pin.

An low dropout (LDO) linear regulator with PMOS as pass device is integrated to provide the internal 5V supply with 100mA current capability. With a PMOS transistor as a pass device, the linear regulator is easier to drive than an NMOS LDO, and to achieve
Figure 4-1: Simplified Block Diagram
lower dropout than an NPN LDO. This PMOS LDO is externally compensated by placing a minimum 4.7uF low-ESR tantalum or ceramic capacitor at the INTVCC pin.

This IC also integrates an internal oscillator to provide a clock with frequency configurable from 250kHz to 770kHz. To set an precise frequency using an external precision resistor, a few devices on the chip need to be trimmed sequentially. The clock oscillation time constant is generated by current charging a capacitor.

\[ T = \frac{CV_T}{I} \]  

The charging current is generated by the bandgap voltage and a series of thin film resistors, first scaled with current mirror, and then proportioned by the voltage on FREQ pin. First, the thin-film resistors have to be trimmed for the absolute values of this charging current and the biasing current on FREQ pin to be accurate. Then, the specific current mirror must be trimmed to accommodate the process variations on the absolute value of capacitor.

4.3 Configuration Selection

This circuit block selects between the general-purpose converter configuration and the DDR configuration. In the DDR configuration, the regulated output voltage is shorted to VFB and then divided by half internally. In the general-purpose converter configuration, the regulated output voltage will be divided by an external resistor divider before being applied to VFB pin. In the latter case, the external resistor divider should not be loaded by the internal resistor divider. The easiest way to achieve no loading is using transmission gate, as shown in Fig. 4-2.

The current leakage into the positive input of error amplifier (EA) is on the order of 100nA. For the dividing ratio to be accurate in the DDR configuration, the current running in the divider must be two orders of magnitude higher than 100nA. To have that much current, each resistor must be small. In the general purpose configuration where MN01 is turned off, the 100nA leakage current flows through R01, creating a voltage drop. To reduce this drop, again, the value of R01 must be small. However, such a small resistor would lead
Figure 4-2: If CSELB is high, VREFIN is divided by half before applied to the positive input of error amplifier
to higher quiescent power consumption. Additionally, for this simple design, the size of MN01 must be huge so that its on-resistance will be two order of magnitudes smaller than the already small resistance values of R01 and R02.

A better but slightly more complicated design could be done as in Fig. 4-3. If the configuration selection pin CSEL is shorted to ground, transistors MN1 and MP1 are turned on while MN2 and MP2 are turned off; the voltage applied on the VREFIN pin is divided by half internally before being applied to the positive input of EA. On the other hand, if CSEL pin is shorted to the internal LDO 5V output INTVCC, transistors MN1 and MP1 are turned off while MN2 and MP2 are turned on; VREFIN is then shorted to the positive input of EA.

For the layout of this block, there are two issues to consider. The MOS transmission gate switch comprises MN2 and MP2, which are directly connected to the package pin, and have risks of being damaged by electrostatic discharge (ESD). Hence, in the physical layout of the circuitry, these devices must have ESD spacing. It means that the drain of these devices are drawn longer, and effectively a resistor is placed in series with the transistor to provide current limit protection. Since the input bias current of the EA is tens of nano amperes, the small amount of resistance created by ESD spacing does not generate much
Figure 4-3: If CSEL is grounded, VREFIN is divided by half before applied to the positive input of error amplifier

systematic offset in the regulated output voltage.

The resistor pair R1 and R2 must be precisely matched. In the DDR configuration, the precision of this matching is determines how precise the $V_{TT}$ output is. Any mismatch leads systematic offset of $V_{TT}$ voltage deviated from half of $V_{DD}$. Fortunately, it is not difficult to achieve $\pm0.1\%$ matching for integrated thin film resistors on this process platform, if the following rules are strictly observed:

1. Matched resistors have the same width and are sufficiently wide, in this case, 10 times the minimum feature size of the process technology platform;

2. Matched resistors are orientated in the same direction;

3. Matched resistors are on an iso-therm;

4. Resistor segment taps are on an iso-therm to avoid contact therm-couple effect;

5. Dummies are placed on both end of the resistor array;
6. Matched resistors are placed away from the power devices, specifically, gate drivers and LDO;

7. Each of the matched resistor pair are an array of resistors in parallel. The array resistors is interdigitated to have a common centroid.

### 4.4 Error Amplifier

The basic design of error amplifier is included in Fig. 4-4.

The PNP input stages allow low common-mode inputs. The NPN differential pair gain stage with PTAT current biasing provides constant transconductance over a wide range of temperatures.
To allow soft start, the error amplifier takes an additional positive input, TKSS. This slow rising TKSS voltage is diode AND-ed with $V_{FB}$. After TKSS rises above $V_{FB}$, $V_{FB}$ takes over to become the positive input. At startup, both inputs of the error amplifier, TKSS and $V_{FB}$, are almost near zero voltage. To prevent $V_{ITH}$ floating all the way to the clamp limit and resulting in a few very wide pulses when the regulator starts initial switching, we push asymmetrical currents into the level-shift resistors and get the $V_{ITH}$ driven to ground. As the output ramps up, the common mode of the error amplifier rises; we gradually turn off the asymmetrical level-shift currents. To ensure the accuracy of output voltage, we need to turn off the asymmetrical level-shift current completely before the part settles.

It takes some thought to choose where in the circuit to sense the common mode of the EA. Since the concern is about the biasing current mirror out of saturation, it is natural to choose the drain of the MOSFET. However, this node will have large disturbance and the comparator will need very large hysteresis impossible to design. An alternative node to sense is TKSS. It is relatively steady and the comparator will only need small amounts of hysteresis.

4.5 Current Comparator

4.5.1 Current Threshold

The output voltage of the error amplifier, $V_{ITH}$, determines the current threshold at when the top switch turns off in each clock period. In the circuit block named ITHD, voltage $V_{ITH}$ is converted into a current by a fixed ratio $R_{ITH}$. This current, $V_{ITH}/R_{ITH}$, later gets reduced by 20uA. The resulting current gets scaled by current mirrors, flows through the offset resistor $R_{offset}$ in the current comparator, and generates the current threshold.

Hence, the current comparator threshold offset (without slope compensation) is determined by $V_{ITH}$ with the following formula,

$$\Delta V_{sense} = \left(\frac{V_{ITH}}{R_{ITH}} - I_{offset}\right) \cdot \zeta \cdot R_{offset}. \quad (4.2)$$
For the converter to have almost symmetrical capabilities to sink and source current, $\Delta V_{\text{sense}}$ should be designed to cover a wide range from a negative minimum to a positive maximum, as $V_{ITH}$ ranges from 0V to 1.8V. We must note that when $V_{ITH}$ is below 200mV, the current sink NMOS in the output stage of EA could be out of saturation during which the EA no longer functions properly. Hence, $V_{ITH}$ should never be driven below 200mV in static state operation. The minimum current sense threshold (negative value) should be slightly bigger in absolute value than the maximum current sense threshold.

Assuming that the power stage of converter uses switches with on-resistance of 2$m\Omega$ to sink and source up to 25 amperes of current (with 40% ripple, peak current is 30A), a reasonable current threshold design is maximum of 60mV and minimum of -72mV. From that,

![Figure 4-5: Current sense threshold versus $V_{ITH}$ in this design](image)

we choose in this design, $I_{\text{offset}} = 20uA$, current mirror ratio $\zeta = \frac{25}{60}$ or $\frac{40}{60}$ or $\frac{60}{60}$ depending on whether the $ILIM$ pin is connected to $SGND$, float, or $INTVCC$, and $R_{\text{offset}} = 4k\Omega$.

### 4.5.2 Wide Input-Range Current Comparator

As the output voltage is specified to be between 0.3V and 13V, the current comparator has to accommodate a wide common mode input range. For the low inputs, a PNP input
stage is desired; however, for the high inputs, a NPN input stage is more convenient. An additional voltage comparator was included in this current comparator in order to do both. If the common mode of inputs is below 1.4V, the inputs connect to a pair of PNP transistors and get level-shifted up before fed into the NPN input stages; if the common mode is higher than 1.4V, the inputs connect to the NPN input stages directly. Hysteresis of 300mV is added to avoid oscillation.

4.6 Adaptive Dead-Time Controller

To construct a delay-lock loop (DLL) to align two edges, we use a latch to check which edge comes first, a counter to memorize the state, and a variable delay line. At the front end, we also need to sense the signals. There are in total two delay-locked loops, for the TG low and BG high edge, and for the BG low and TG high edge. Though they are connected differently, the designs are almost the same.

4.6.1 Signal Sensing

Ideally we could use two comparators to determine the times when the power MOSFET body diode starts and stops conducting. Then we could use a delay lock loop to adjust the delay from top gate turn-off logic signal to bottom gate turn-on logic signal until when those two times are very close. In the steady state, the time between the body starts and stops conducting is minimal and perhaps zero.

The SW node, with nanohenry stray inductance and a few nanofarad parasitic capacitance, gives ringing at a few hundred megahertz. Occasionally, the ringing is too large in amplitude and too fast to handle. Hence, the SW node signal must be latched and the sensing output is only allowed to change once every clock period.

The SW node can be as high as one body diode forward voltage above the input voltage and can be as low as one diode voltage below ground. That means, numerically, that the SW node can be anything between -1V and 40V. To sense the SW node, a drain-extended thick-oxide MOSFET is required to block high voltage. Unfortunately, under this process
platform, this high-voltage MOS device is non-isolated, and its body is common with P-substrate. A series resistor has to be added to limit the body diode conduction of the blocking device when SW node falls below ground. The RC time constant of this current limiting resistor and the parasitic capacitance is too large for this sensing circuitry to be fast.
Figure 4-6: OUT is high if SW rises 200mV above TD, or 200mV below SGND
Moreover, the speed of the sensing circuitry depends on the overdrive. If the SW falls from a higher voltage to ground, the overdrive is larger and the circuitry will respond much faster.

Because SW could fall below ground or rise above TD, we have to be very careful in the physical layout of the block to avoid latchup.

4.6.2 Latch

As drawn in Fig.4-7, two falling edges, SB1 and SB2, race against each other to set UP and DOWN. Without loss of generality, we look at the set of latches for events on the TG low and BG high edge. For this edge, SB1 is a logic signal that is 0 if BG is above the power MOSFET threshold, and SB2 is the logical signal that is 0 if SW is more than 200mV above the input voltage or more than 200mV below ground. If the falling edge of SB1 comes first, the UP will go high; it means the bottom power switch turns on too early, and the counter should count up. If the falling edge of SB2 comes first, the DOWN will go high; it means the body diode of one of the power switches has turned on before the bottom switch could turn on, and in this case, the counter should count down.

One important detail is that in each clock cycle, we need to reset the SB1/SB2 racing after top power switch is on so that the circuitry is ready for the next racing. Using the rising edge of CLK1 is too early to avoid the ringing of the rising SW edge, and using the falling edge of CLK1 is too late for low-duty case. The required reset signal must arrive earlier than the event of top gate turn-off, so the latches are correctly reset before the next edge of SW falling and the edge of BG turning on; on the other hand, this clock signal has be arrive later than the clock signal for the counter, so that the counter has enough time to settle to its next state before its inputs change. It turns out that the current comparator output ITRP is perfect for the reset task. The ITRP signal always arrives before the edge of SW falling and the edge of BG turning on. Whichever of SB1/SB2 comes first, the latches reset by ITRP will be ready for the racing. Furthermore, the ITRP signal arrives at least tens of nanoseconds later than the CLK1, which gives ample time for the rising SW signal to settle and avoid false tripping.
Figure 4-7: Latch determines which of two falling edges, SB1 and SB2, comes first after each rising RESET pulse.
Figure 4-8: Timing of Edges. From top to bottom, the signals are: *ITRP*, current comparator output and the reset signal for latches; *DOWN*, logic signal for counter down transition; *UP*, logic signal for counter up transition; *BG*, the gate voltage of bottom power switch; *SB_BG*, logic signal that is low if the gate voltage of bottom switch is higher than the MOSFET threshold voltage (1.6V); *SW*, the SW node voltage; *SB_Sw*, logic signal that is low if the SW node is more than 200mV below ground.
In Fig.4-8, we see an example of the timing of the delay-locked loop, for the $TG$ low and $BG$ high edge. The current comparator trips first, and the latches get reset. Both $UP$ and $DOWN$ go low after the $ITRP$ signal goes high. Then the $SW$ falls, and the body diode of the bottom power switch conducts. The $SW$ signal goes below ground. The bottom gate turns on, and the $BG$ goes high. In Fig.4-8, the $BG$ go above the MOSFET threshold voltage before the $SW$ falls below ground; hence, the counter counts up so that the variable delay in the bottom gate driver will increase slightly in the next clock cycle.

The timing of these signals on the second delay-locked loop, for the $BG$ low and $TG$ high edge, is similar. An example of the timing is described here. First, the positive edge of internal clock signal comes, and the latches get reset. Both $UP$ and $DOWN$ go low after the $CLK$ signal goes high. Then the $SW$ rises, and the body diode of the top power switch conducts. The $SW$ signal goes above input voltage. The top gate turns on, and the $TG$ goes high. If the $TG$ goes one MOSFET threshold voltage above $SW$ before the $SW$ rises above input voltage, the counter counts up so that the variable delay in the top gate driver will increase slightly in the next clock cycle.

4.6.3 Up-Down Counter

The counter is constructed with 4 toggle flip-flops. A typical toggle flip-flop with minimum sizing is shown in Fig.4-9.

The counter design is shown in Fig.4-10. The counter could count up or count down, depending on which of the two inputs, $UP/DOWN$, is high at the rising edge of clock. If both up and down signals are received at the clocking edge, the counter will act as it has only received the up signal (see gates I47 and I60 in Fig.4-10). To prevent overflow, additional logic makes sure that this counter will stay at 1111 if it is already 1111 and receives an up signal (see I24, I40, and I61 in Fig.4-10). Similarly, it will stay at 0000 if it is already 0000 and receives a down signal (see I25, I39, and I62 in Fig.4-10).
Figure 4-9: If $T=0$ at rising edge of CLK, $Q$ does not change after the negative edge of CLK; if $T=1$ at the falling edge of CLK, $Q$ changes to $QB$ after the negative edge of CLK.
Figure 4-10: 4-bit Counter
If the counter starts with the wrong state, shoot-through could occur. To be safe, the counter should always start with 1111 when the regulator starts switching. In our design, the counter counts up as soon as the internal oscillator in the chip starts to produce clock signal. When the regulator has finally started switching (many clock cycles later), the counter has been counting up and already reached 1111.

4.6.4 Delay Line

The delay line produces a copy of input signal with the positive edge delayed by a variable duration, as shown in Fig.4-11. It consists 15 delay elements. Each delay element, with 200fF capacitance to charge, produces a nominal delay of 2.8 nanoseconds on the positive edge, as shown in Fig.4-12. This determines the quantization step in dead-time to be nominally 2.8 nanoseconds, accurate enough for hundred kilohertz switching. The 16-to-1 multiplexer (mux) selects the output from the 16 differently delayed signals, based on the state of counter C[3:0].
Figure 4-12: Each element provides a nominal delay of 2.8ns
Chapter 5

Full-Chip Simulation

Integrated circuits should be designed for test. Because each device is on the micro-scale and because not every circuit node has a pad available for probing, ICs are difficult to test or debug. Hence, efforts must be made to ensure the testability of each IC.

Specifically for DC-DC converters, it is difficult and inefficient for the automated test machine to test the chip, while the switches are switching at hundreds of kilohertz. Thus, for many electrical specifications, we need to test the IC without being in switching operation and indirectly prove that it is working. We call this non-switching mode of operation the test mode. During the design phase, we simulate the fullchip in both the test mode and the switching mode.

5.1 Simulations of Test Mode

To obtain maximum current thresholds without the converter switching, the easiest way is to pull up the \( FB \) down to 500mV, much higher than \( VREFIN \), so that the error amplifier output is clamped high at 1.8V. When error amplifier output \( VITH \) is high, the threshold of current comparator is at maximum. If we fix the current sense comparator negative input \( SENSE- \) at 3.3V and slowly ramp up the current sense comparator positive input \( SENSE+ \) from 3.3V to 3.4V, the \( TG \) will fall and \( BG \) will rise when \( SENSE+ \) is about 63mV higher than \( SENSE- \). Table.5.1 summarizes the current thresholds obtained from spice simulation.
of the circuit. In absolute value, the minimum current thresholds are about the same as the maximum current thresholds. In other words, this DC-DC controller has symmetrical sink/source current limits, suitable for applications on DDR memory termination.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Current Sense Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td></td>
</tr>
<tr>
<td>(VFB=500mV, VREFIN=VREFOUT)</td>
<td>ILIM=0V</td>
</tr>
<tr>
<td></td>
<td>ILIM=FLOAT</td>
</tr>
<tr>
<td></td>
<td>ILIM=INTVCC</td>
</tr>
<tr>
<td>Minimum</td>
<td></td>
</tr>
<tr>
<td>(VFB=640mV, VREFIN=VREFOUT)</td>
<td>ILIM=0V</td>
</tr>
<tr>
<td></td>
<td>ILIM=FLOAT</td>
</tr>
<tr>
<td></td>
<td>ILIM=INTVCC</td>
</tr>
</tbody>
</table>

Table 5.1: Simulated Current Threshold

### 5.2 Simulations of Switching Mode

Simulation of a chip in the switching mode is much more time-consuming than in the test mode. LTspice is a high performance Spice simulator, optimized for simulation of switching DC-DC converters. It has made simulating switching converters very fast compared to that in normal Spice simulators. However, due to the complexity of a full chip, it still takes days to finish a full-chip simulation of switching mode.

To demonstrate the functionality of adaptive dead-time control block in this chip, we run a full-chip simulation in LTspice, as shown in Fig.5-1. It is connected in the DDR configuration. It takes power from a supply of $V_{DD} = 1.5V/2.5V/3.3V$, to produce an output $V_{TT}$ that is half of $V_{DD}$ and sink/source 5A/20A.
Figure 5-1: Full chip simulation for DDR application
We made measurements on this transient simulation, and calculate the efficiency using the product of output voltage and output current divided by the product of input voltage and input current. By connecting FIXDT to INTVCC or SGND, we could disable or enable the ADTC block in the chip. Table 5.2 compares the simulated efficiencies with and without adaptive dead-time control. With a proprietary LTSpice VDMOS model of HAT2166H, switching loss and conduction loss on the power switches are well captured in the simulations. The inductor has been modelled as an $0.3\mu H$ ideal inductor in series with $1.8\,m\Omega$ ideal resistor to capture the conduction loss through the inductor in the simulation.

<table>
<thead>
<tr>
<th>$V_{IN}$ (V)</th>
<th>$V_{OUT}$ (V)</th>
<th>$I_{out}$ (A)</th>
<th>$f_{SW}$ (kHz)</th>
<th>Efficiency with FIXDT=SGND</th>
<th>Efficiency with FIXDT=INTVCC</th>
<th>$\Delta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>1.25</td>
<td>5</td>
<td>500</td>
<td>92.1%</td>
<td>91.2%</td>
<td>0.87%</td>
</tr>
<tr>
<td>2.5</td>
<td>1.25</td>
<td>20</td>
<td>500</td>
<td>87.2%</td>
<td>86.8%</td>
<td>0.41%</td>
</tr>
<tr>
<td>2.5</td>
<td>1.25</td>
<td>-20</td>
<td>500</td>
<td>85.5%</td>
<td>84.7%</td>
<td>0.79%</td>
</tr>
<tr>
<td>1.5</td>
<td>0.75</td>
<td>5</td>
<td>500</td>
<td>91.1%</td>
<td>88.3%</td>
<td>2.81%</td>
</tr>
<tr>
<td>1.5</td>
<td>0.75</td>
<td>20</td>
<td>500</td>
<td>81.1%</td>
<td>80.3%</td>
<td>0.84%</td>
</tr>
<tr>
<td>1.5</td>
<td>0.75</td>
<td>-20</td>
<td>500</td>
<td>76.0%</td>
<td>75.1%</td>
<td>0.92%</td>
</tr>
</tbody>
</table>

Table 5.2: Simulated Efficiency with FIXDT connected to INTVCC or SGND
Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis project, a constant-frequency peak-current mode synchronous step-down DC-DC controller integrated circuit with adaptive dead-time control is designed based on the LTC3855, for both DDR memory termination and general-purpose applications. In periodic steady state, the switch turns on exactly when the body diode starts to conduct current. The conduction loss through MOSFET switch body diode is minimized. In spice simulation, this scheme increases overall efficiency in low-voltage application by up to 3%.

6.2 Known Issues and Discussion

With digital dead-time control, dead-time could only be adjusted by a quantanized amount in each clock cyle. With 4-bit accuracy in the counters, digital lock loop responds to each transient situation within up to 15 clock cycles. For converters switching at 250 kHz to 770 kHz, that corresponds to 60 to 20 microseconds. If transients happen more often than tens of kilohertz, the delay lock loop would not be able to follow and would oscillate. However, this does not usually happen. Because of the large output capacitor, the load transient is never as fast and as sharp.

From the TG, BG and SW waveforms, there is no easy method to extract the informa-
tion of external MOSFET switch’s threshold voltage. By using comparators for TG and BG with 1.6V threshold, the adaptive dead-time controller could be slightly aggressive if the threshold voltage of external switch is 1.2V, and could be conservative if it is 2.5V. However, this is not a real issue. Once the designated application is finalized, the MOSFET switches are no longer changed again. It is simple to provide users with this same IC but with options on the switch threshold voltage.
Appendix A

Pin Functions

Functions of each pin on this controller integrated circuit is described here.

**PLLIN** External Synchronization Input to Phase Detector pin. A clock on the pin will force the controller synchronize the internal oscillator with the clock on this pin. The phase-lock loop compensation network is integrated into the IC.

**FREQ** There is a precision 10μA current flown out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

**TKSS** Output Voltage Tracking and Soft Start Input. A capacitor to ground at this pin sets the ramp rate for the output voltage. Internal soft start current of 1.2μA is charging the pin.

**SENSE+** Current Sense Comparator Input. The (+) input to the current comparator is normally connected to DCR sensing network or current sensing resistor.

**SENSE-** Current Sense Comparator Input. The (-) input to the current comparator is connected to the output.

**VFB** Error Amplifier Feedback Input. If $CSEL=0V$, this pin connects to the output and is applied to the negative input of the error amplifier. If $CSEL=INTVCC$, this pin
receives the remotely sensed feedback voltage from external resistive divider across the output, and the divided output voltage is directly applied to the negative input of the error amplifier.

**VITH** Current Control Threshold and Error Amplifier Compensation Point. The current comparator tripping threshold increases with the VITH control voltage.

**SGND** Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

**FIXDT** Dead-Time Selection Input. Connect this pin to SGND to enable the adaptive dead-time control. Connect this pin to INTVCC to disable the adaptive dead-time control.

**CSEL** Configuration Selection Input. Connect this pin to SGND for the DDR configuration with VOUT=1/2VREFIN. Connect this pin to INTVCC for the general-purpose converter configuration.

**VREFIN** Positive Input of Internal Error Amplifier. If CSEL=0V, this pin connects to an external reference and divides its voltage to 1/2 VREFIN through precision internal resistors before it is applied to the positive input of the error amplifier. Reference voltage for output voltage, power good threshold, and short-circuit hiccup mode threshold. If CSEL=INTVCC, connect this pin to VREFOUT and its voltage is directly applied to the positive input of the error amplifier. If output needs to be below 0.6V, connect this pin to external low output impedance sub-0.6V reference voltage.

**VREFOUT** Precision 0.6V Reference Voltage Output.

**RUN** Run Control Input. A voltage above 1.2V on this pin turns on the IC. However, forcing the pin below 1.2V causes the IC to shut down. There are 1.0uA pull-up currents for the pin. Once the Run pin rises above 1.2V, an additional 4.5uA pull-up current is added to the pin.
**ILIM** Current Comparator Sense Voltage Range Input. This pin is to be programmed to SGND, FLOAT or INTVCC to set the maximum current sense threshold to three different levels for the comparator.

**PGOOD** Power Good Indicator Output. Open drain logic out that is pulled to ground when the output exceeds 10% regulation window, after the internal 20us power bad mask timer expires.

**EXTVCC** External Power Input to an Internal Switch Connected to INTVcc. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever EXTVCC is higher than 4.7V. Do not exceed 6V on this pin.

**VIN** Main Input Supply. Decouple this pin to PGND with a capacitor (0.1uF to 1uF).

**TD** Top FET Drain Input. This pin should be tied to the drain of top power MOSFET.

**INTVCC** Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7uF low ESR tantalum or ceramic capacitor.

**BG** Bottom Gate Driver Output. The pin drives the gate of the bottom N-Channel MOSFET between PGND and INTVCC.

**PGND** Power Ground Pin. Connect this pin closely to the source of the bottom N-channel MOSFET, the (-) terminal of CVCC and the (-) terminal of CIN.

**BOOST** Boosted Floating Driver Supply. The (+) terminal of the boost-strap capacitor connects to the pin. The pin swings from a diode voltage drop below INTVCC up to VIN + INTVCC.

**TG** Top Gate Driver Output. This is the output of floating driver with a voltage swing equal to INTVCC superimposed on the switch nodes voltage.

**SW** Switch Node Connection to Inductor. Voltage swing at the pin is from a Schottky diode (external) voltage drop below ground to a diode voltage above TD.
**Exposed Pad** Signal Ground. Must be soldered to PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.
Bibliography


[7] Linear Technology Corporation. LTC3770 Fast No RSENSE Step-Down Synchronous Controller with Margining, Tracking and PLL.


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