Exercise 3-1: When a particular network having a single port is connected to a 1 kΩ resistor, its port voltage is 2.5 V. When the same network is connected to a 4 kΩ resistor, its port voltage is 4 V. Determine the Thevenin and Norton equivalents of the network.

Exercise 3-2: This exercise applies two different analyses to determine the unknown node voltages in Network (a) shown below. It illustrates that the direct method of analysis is not always the simplest.

(a) Use the node method to find the two unknown node voltages in Network (a).

(b) First, explain why Network (a) may be re-drawn as network (b). Second, combine the left source in Network (b) with the two left-most resistors to form their Thevenin equivalent and redraw the resulting network. Third, combine the right source with the two right-most resistors to form their Thevenin equivalent and again redraw the resulting network. Finally, using superposition, determine the two unknown node voltages in the thrice re-drawn version of Network (a) thereby completing the analysis.

Problem 3-1: This problem studies the fluid flow system shown below, and illustrates how the concepts taught in 6.002 can be applied to the study of systems beyond electronic circuits. The flow system comprises a pump, two sections of pipe and two open fluid reservoirs. Note, however, that the joint between the two pipes leaks.
The pump draws fluid from the first reservoir at ambient pressure and raises the fluid pressure to $p_{\text{PUMP}}$ above ambient. This pressure rise pumps the fluid through the two sections of pipe, delivering the fluid to the second reservoir at ambient pressure. It is assumed here that fluid flow in a pipe obeys the linear law $p = Raf$ where $p$ is the pressure drop across the pipe (N/m²), $f$ is the fluid flow through the pipe (m³/s), and $R$ is the flow resistance of the pipe (Ns/m⁵). Note that the pipe sections in the system shown below have flows $f_1$ and $f_2$, and flow resistances $R_1$ and $R_2$. In contrast to pipe flow, fluid flow through the leak obeys the nonlinear law $f_{\text{LEAK}} = \frac{F_{\text{LEAK}}}{\sqrt{p_{\text{LEAK}}}}$ where $p_{\text{LEAK}}$ is the pressure rise at the leak, $f_{\text{LEAK}}$ is the fluid flow through the leak, and and $F_{\text{LEAK}}$ and $P_{\text{LEAK}}$ are a reference flow rate and pressure, respectively.

(a) Adopt the following analogy: pressure $\leftrightarrow$ voltage, fluid flow rate $\leftrightarrow$ current and flow resistance $\leftrightarrow$ resistance. Draw the electric-network analog to the fluid flow system, but label its node voltages and branch currents with the flow system variables. Additionally, state the fluid flow equivalents to KCL and KVL.

(b) Derive a Thevenin equivalent for the pump and the two sections of pipe, and redraw the analog to the flow system accordingly. The terminal variables for the Thevenin equivalent should be $-f_{\text{LEAK}}$ and $p_{\text{LEAK}}$. Use the Thevenin equivalent to simplify the remaining parts of this problem.

(c) In terms of $f_{\text{LEAK}}$ and $p_{\text{LEAK}}$, graph the flow-pressure relation of the Thevenin equivalent network and the leak on the same graph, and indicate the operating point of the flow system.

(d) Analytically determine $f_{\text{LEAK}}$ and $p_{\text{LEAK}}$, and then $f_1$ and $f_2$.

(e) Determine the power delivered by the pump as it pumps the fluid. Hint: consider the electrical analog of power, and check units.
Problem 3-2: This problem studies Boolean algebra and the implementation of logic functions with gates.

(a) For the functions \( F(A, B, C) \) and \( G(A, B, C) \) specified in the following truth table, write a corresponding logic expression.

<table>
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<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>( F(A, B, C) )</th>
<th>( G(A, B, C) )</th>
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(b) Implement \( F(A, B, C) \) with 2-input NAND gates. Hint: Use DeMorgan’s laws.

(c) Give an implementation using gates for each of the logic expressions below. Also, write the truth table for expression 1.

\[
\begin{align*}
1. & \quad (A + \overline{B})(A \cdot \overline{B} + C) + \overline{C} \cdot D \\
2. & \quad (A \cdot \overline{C} + B \cdot \overline{D})(D + B + A) \\
3. & \quad A + \overline{B} \cdot D + A \cdot C \cdot D \\
4. & \quad ((A + \overline{C}) + B + \overline{D}) + A \cdot \overline{C} \cdot D
\end{align*}
\]

Problem 3-3: Consider a family of logic gates which operate under the static discipline with the following voltage thresholds: \( V_{OL} = 0.5 \) V, \( V_{IL} = 1.6 \) V, \( V_{OH} = 4.4 \) V and \( V_{IH} = 3.2 \) V.

(a) Graph an input-output voltage transfer function of a buffer satisfying the voltage thresholds given above.

(b) When transmitting information over a noisy wire, buffers can be used to minimize transmission errors by restoring signal values. Consider the transmission of data over a noisy wire which picks up a maximum of 80 mV symmetric peak-to-peak noise per centimeter. How many buffers are needed to transmit a signal over a distance of 2 meters in this noisy environment?

(c) How large are the 0 and 1 noise margins? Now consider three buffers connected in series and behaving as a single buffer. What are the noise margins for this new buffer?

(d) Using the switch-resistor MOSFET model, design an inverter satisfying the static discipline for the above voltage thresholds using an n-channel MOSFET with \( R_n = 1 \) k\( \Omega \) and \( V_T = 1.8 \) V. Recall, \( R_{on} = R_n(L/W) \). Assume \( V_S = 5 \) V and \( R_{\Omega} \) for a resistor is 500 \( \Omega \). Further assume that the area of the inverter is given by the sum of the areas of the MOSFET and the resistor. Assume that the area of a device is approximately \( L \times W \). The inverter should take as little area as possible with minimum size for \( L \) or \( W \) being 0.5 \( \mu \)m. Graph the input-output transfer function of the inverter. What is the total area of the inverter? What is its maximum static power dissipation?
Problem 3-4:

(a) Give a resistor-MOSFET implementation of the following two logic functions.

1. \( \overline{A} \cdot \overline{B} \cdot C \cdot D \)
2. \( (\overline{Y} \cdot \overline{W})(\overline{X} \cdot \overline{W})(\overline{X} \cdot \overline{Y} \cdot \overline{W}) \)

(b) Remember that a NAND gate can be implemented as a circuit with two n-channel MOSFETs and a pull-up resistor \( R_L \). Let us call it the NAND circuit shown below. These NAND circuits are used by Penny-Wise Computer Corporation in their computer boards. In one ill-fated shipment of computer boards, the outputs of a pair of NAND circuits get shorted accidentally resulting in the effective Circuit X shown below. What logic function does Circuit X implement? Construct its truth table.

![NAND Circuit](image)

![Circuit X](image)

(c) If we connect \( n \) identical NAND circuits together in parallel forming Circuit Y as shown in the figure below, what is the general form of the logic function it implements? If for each MOSFET, \( R_{\text{on}} = 500 \, \Omega \), \( R_L = 100 \, k\Omega \), and \( V_T = 1.8 \, V \), how many NAND circuits can we connect in parallel and still satisfy the static discipline for the voltage thresholds given in Problem 3-3?

![Circuit Y](image)

(d) We now connect 10 identical NAND circuits together and have the resulting Circuit Y satisfy the static discipline for the voltage thresholds in Problem 3-3 with \( R_L = 500 \, \Omega \). Give specifications on the dimensions of the MOSFETs such that total MOSFET area is minimized. As before, assume that the area of a device is \( L \times W \). Assume that \( R_n = 1 \, k\Omega \) and no resistor dimension or MOSFET gate dimension should be smaller than 0.5 \( \mu \text{m} \). For what inputs does Circuit Y dissipate maximum static power, and what is that power?